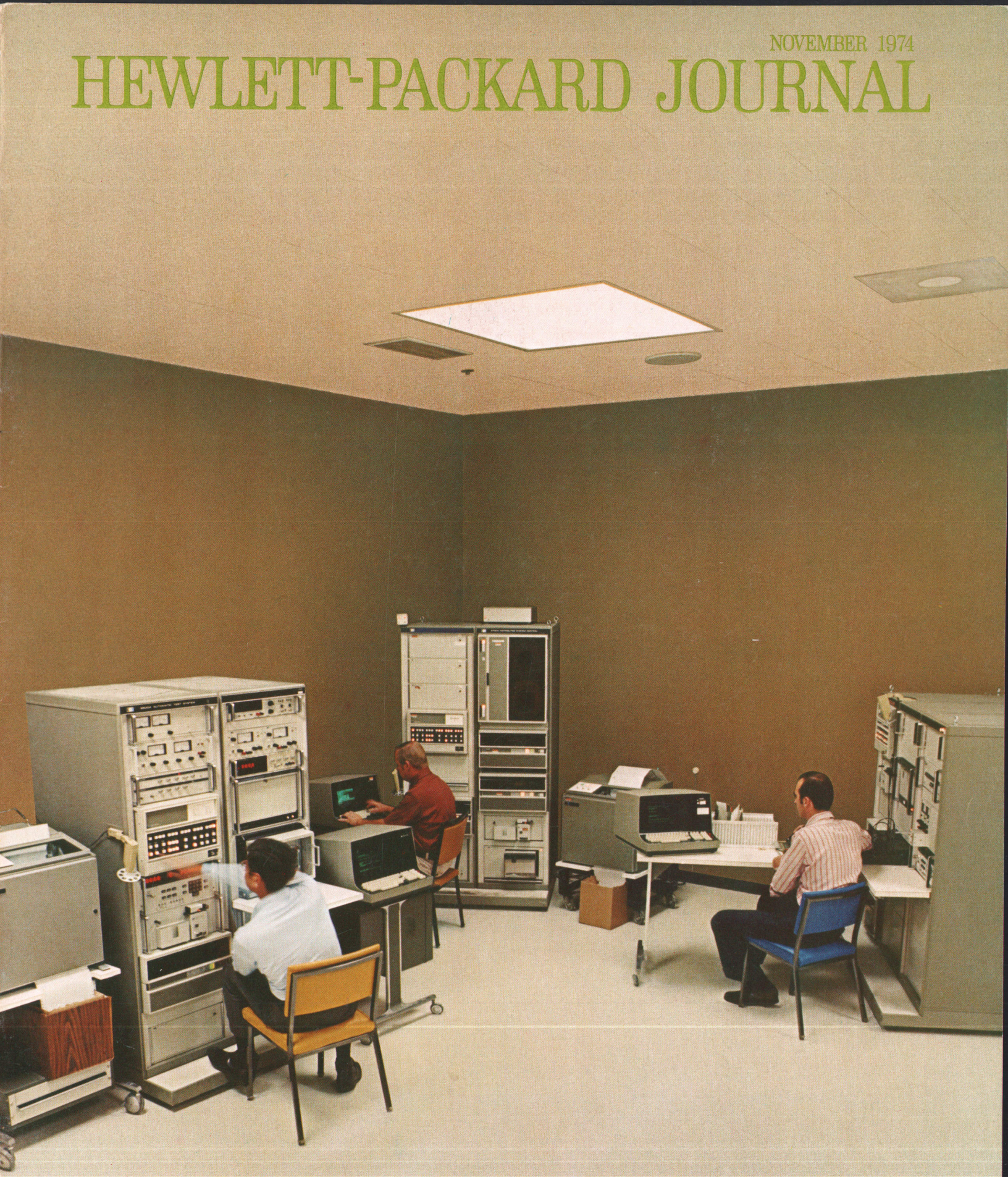
NOVEMBER 1974

HEWLETT-PACKARD JOURNAL



Distributed Computer Systems

As multiple minicomputers collect data, control processes, and run tests, a central computer system supports them all, gathering data, generating management reports, and performing other tasks at the same time.

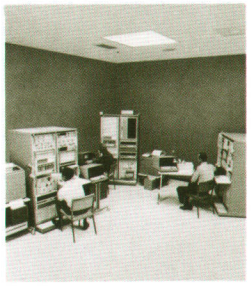
by Shane Dickey

A SINGLE LARGE-SCALE COMPUTER or a network of smaller, less costly computers? In this era of multiplying minicomputer applications and increasing minicomputer efficiency, the answers to this question are changing. There are, of course, computer applications for which the network solution is clearly not appropriate, and there are others in which a decision must be based upon a detailed comparison of the alternatives. But there are more and more applications that can benefit greatly from a network solution.

A not-uncommon situation that typifies problems amenable to solution by a computer network, or a "distributed" computer system, is that of a manufacturer producing and testing a product in several discrete steps. Each step in the process takes place in a different area of the manufacturer's facility, and several could be completed better, faster, and more economically if they were automated (examples might be incoming parts inspection, subassembly manufacturing, subassembly testing, and final testing). However, funds for computer automation are limited. Also, any computer solution must provide for a large, unified data base to coordinate all the manufacturing and testing areas and to provide management information.

Hewlett-Packard 9700-Series Distributed Systems represent a new approach to solving these problems and many others. These systems give the user a powerful minicomputer-based central system and one or more smaller satellite minicomputer systems, each dedicated to a specific task such as data collection, laboratory automation, process control, production monitoring, or automatic testing (see Fig. 1). Special distributed system software makes the systems much more than simple interconnections of computers.

Programs for the satellites are developed and stored at the central system and loaded into the proper satellite on request via a communications link. This assures centralized quality control for applications programs and affects considerable savings through centralization of major peripherals and programming manpower. Upon execution, the satellite programs can manipulate the central station's mass storage devices to build a centralized data base. User programs in different computers can communicate directly with each other via a transparent communi-



Cover: *In this distributed computer system, a 9700A Distributed System Central Station collects data from two satellite automatic test systems dedicated to measurement tasks. Test programs for the satellites are developed at the central station as a background activity. Communication is over hard-wired cable when the systems are as close as these or as much as two miles apart. Common-carrier facilities are used for more widespread networks.*

In this Issue:

Printed in U.S.A.

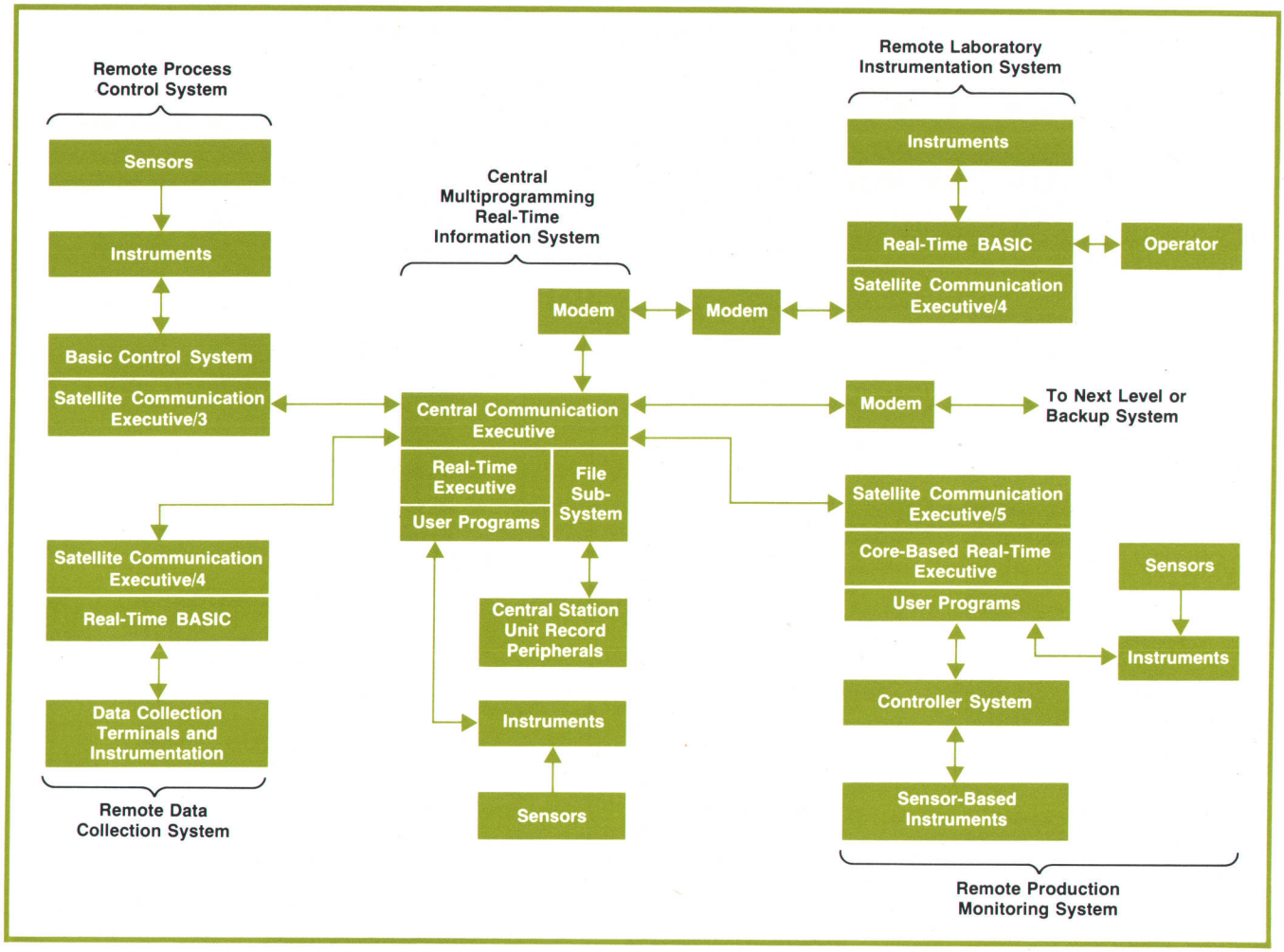


Fig. 1. *HP 9700 Series Distributed Systems are hardware/software systems that allow a central real-time executive (RTE) system to communicate with multiple satellite computer systems. Three satellite operating systems are available: basic control system (BCS), real-time BASIC (RTE-B), and core-based real-time executive (RTE-C).*

cations interface. Because the systems are modular, a user who has limited resources can begin with a minimum system and later expand as much as desired.

A companion package, the Remote Data Transmission Subsystem (RDTS), provides for communication between the central station and the IBM 360/370 series of computers. Thus a direct link can be established between working automatic test systems and a management-level information system. Central station communication with the HP 3000 is also possible via an HP 30300A Programmable Controller.

Integrated Hardware/Software Systems

An HP 9700-Series Distributed System is an integrated hardware/software system. Fig. 1 illustrates a four-satellite arrangement. At the central station is an HP 2100-Series Computer with 24K or 32K words of core memory and various peripherals, including one or more disc drives, a paper tape reader, and a system console. To these may be added one or more magnetic tape drives, a line printer, a card reader, a paper tape punch, a digital plotter, and various measurement instruments. Central station software consists of the multiprogramming real-time executive (RTE), a file management package, and the central station communication executive (CCE).

Each satellite consists of an HP 2100 Computer with 4K or more of core memory and whatever peripherals and console are required. For simple applications a 64-word remote communications loader provides for down-link loading of user-written applications programs from the central station. However, most applications will probably require some form of satellite operating system. The three satellite operating systems available are the basic control system (BCS), the core-based real-time executive (RTE-C), and the real-time BASIC system (RTE-B). Fig. 2 compares their features and capabilities. The operating system is combined with a satellite communication

A Working Distributed System

At HP's Advanced Products Division in Cupertino, California, a 9700 Distributed System helps produce the HP-35, HP-45, HP-70, HP-80, and HP-65 Pocket Calculators.

RTE Central System is a 32K distributed system central station. It has two swapping partitions and a full complement of peripherals including disc drive, card reader, magnetic tape, line printer, and paper tape reader and punch. It is used as the central file system as well as for program preparation, data analysis, and report generation. Applications programs for the satellites are stored here and loaded into the satellites as needed—for example, when changing from HP-80 testing to HP-65 testing.

RTE-C Manufacturing Support Satellite supports all of the automatic equipment on the manufacturing line: four logic board welders, three logic board testers, and a battery charger/tester.

RTE-C Incoming Inspection Support Satellite has a 16K computer controlling a ROM tester, a continuity tester, a component tester, and a data entry station. This satellite is on a Bell 103 modem link to its location in a warehouse five miles from the main facility.

BCS Magnetic Card Recorder Satellite does all of the program recording for the library of prerecorded HP-65 program cards.

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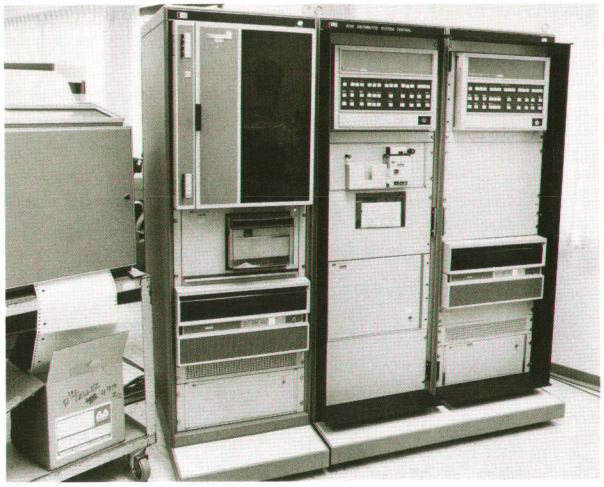
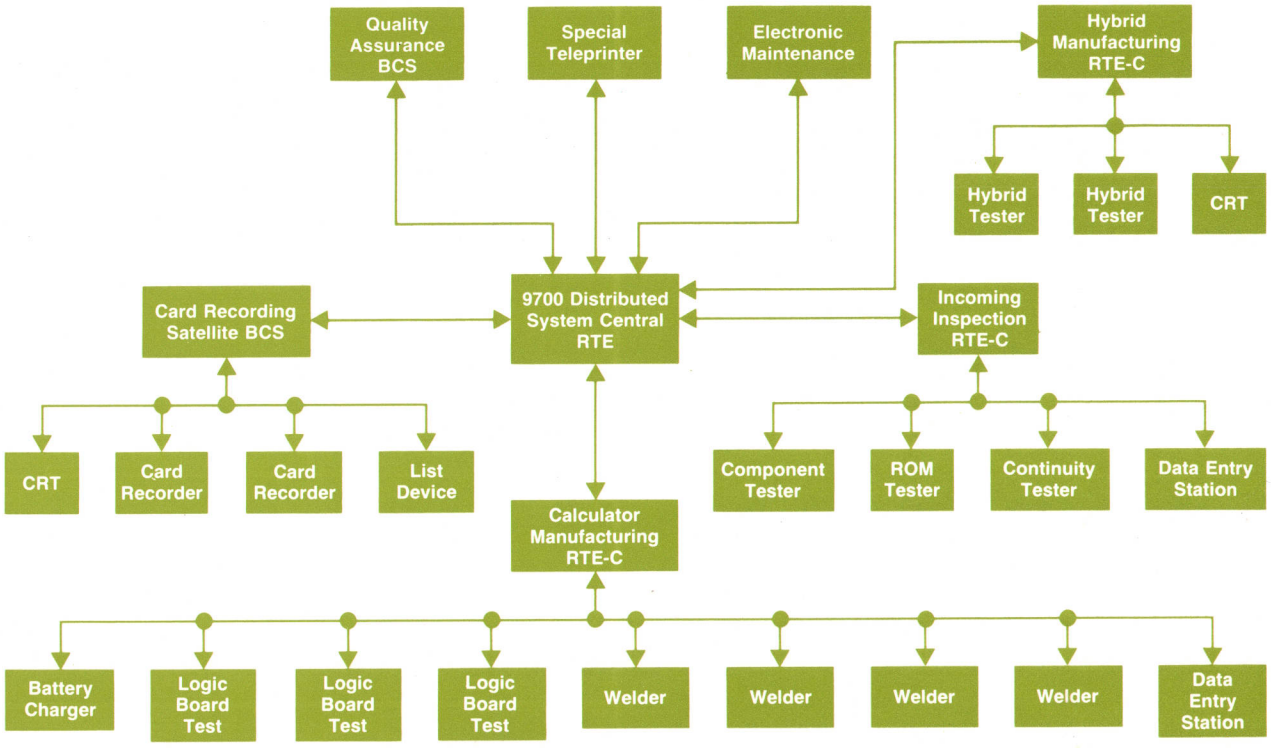
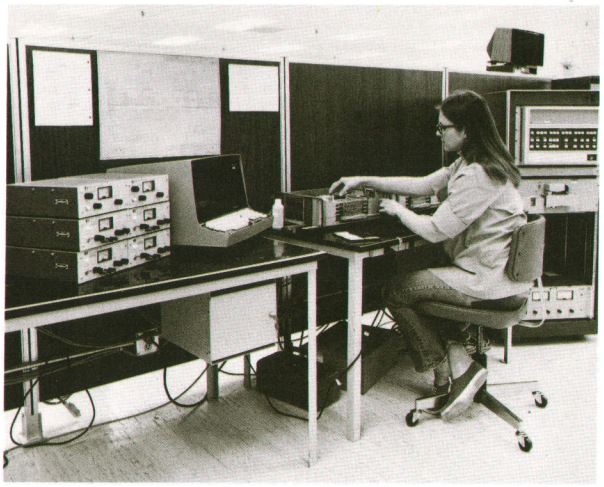


Distributed System Central

Card Recording Satellite



BCS Quality Assurance Satellite may be used as a calculator simulator with access to the central file system.
RTE-C Hybrid Manufacturing Support Satellite is a 16K computer supporting two hybrid testers and a data entry station.



Hybrid Manufacturing Satellite

Electronic Maintenance Satellite is used for peripheral testing. It has access to various diagnostic programs stored in the central file system.
Special Teleprinter has an HP-65 card reader installed. It is used to generate program listings for the HP-65 user's library.

executive (SCE) to complete the link to the CCE.

Connecting the central station with the satellites are serial communication interface cards and either twisted-pair cables for hardwired interconnections or user-supplied modems for communication over common-carrier facilities. Distributed system packages consisting of just the communication hardware and software are available as separate entities for users who already have the computer systems.

The BCS Satellite

The basic control system (BCS) is the least complex of the three satellite operating systems. It provides a starter-set capability to the measurement satellite programmer. Satellite communication executive SCE/3 connects BCS with the central station.

BCS handles execution and input/output interrupt processing of FORTRAN, ALGOL, and assembly-language test programs by means of a complete set of measurement-instrument I/O drivers and library subroutines. Because of its simplicity, BCS has the fastest I/O interrupt service time of all the satellite types, and it is well suited to the dedicated high-speed collection, concentration, and remote storage of test data.

BCS satellites are usually dedicated to their measurement tasks and therefore are not available for preparation of the measurement software that they execute. For this reason all satellite software for these terminals is compiled or assembled as a background activity at the central system while the satellites' ongoing distributed-system needs are being serviced by the foreground distributed-system modules of CCE. The object code thus produced is relocated by a system cross loader and stored on the central station disc to be sent to the satellite on request (see Fig. 3). The BCS satellite operating systems and programs can be generated from files in a batch mode or interactively from the central station console.

Distributed System Capabilities	RTE-C	RTE-B	BCS
Satellite System Generation at Central	•	•	•
Program Development at Central	•		•
Remote Program Test (Satellite program test-executed at Central).	•		
Program Storage on Central Disc	•	•	•
Shared Peripherals	•	•	•
Remote Access to Data Files	•	•	•
Remote Task Scheduling (Satellite-to-Central)	•	•	•
Remote Task Scheduling (Central-to-Satellite)	•	•	
Cooperative Real-Time Multi-processing	•	•	
Dynamic Master-Slave Switching	•	•	
Remote Program Loading	•	•	•
Linking of Program Segments	•	•	•
Forced Program Loading	•		

Fig. 2. *Capabilities of the three types of satellite operating systems and the central real-time executive system.*

Remote File Access and Remote System Services

Once the test program has been loaded into the satellite and begins acquiring measurement data, remote file access (Fig. 4) makes available to the satellite programmer all of the power of the central station's file management package (see box, page 10).

When a request for remote file access is issued by a satellite user program, control is transferred to a remote file access interface subroutine, which assembles all calling parameters and data, if any, into a transmission buffer. This buffer is shipped to the central computer by SCE/3 via a serial-communication I/O driver. Upon arrival at the central station, the request is queued up by CCE for execution. Upon execution, the processing of the request is a two-step procedure. The initial step is accomplished by a remote file access monitor, which determines whether the request is for a new or existing file. If the request is for a new file, a data control block (DCB) is created for use by the file. If the request is for an existing file, the previously created control block is used.

The central station distributed software maintains a data control block for each file currently open in a

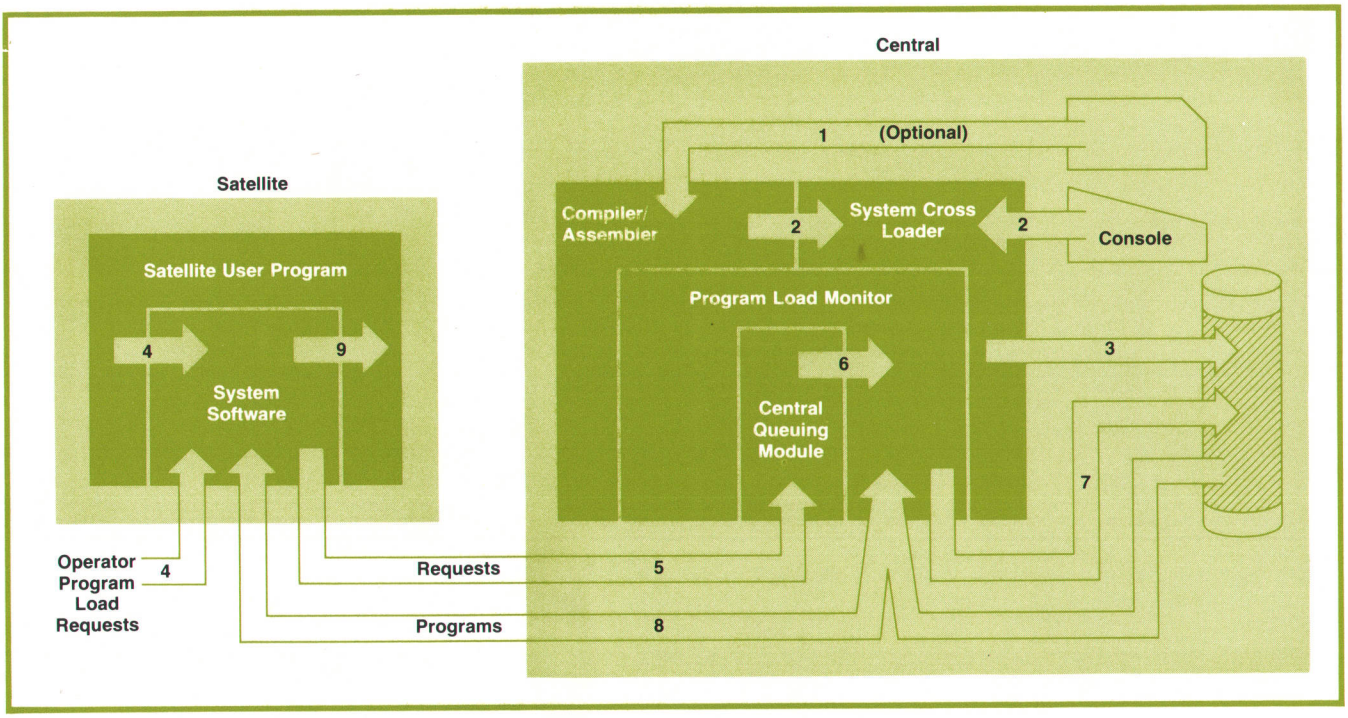


Fig. 3. *Satellite systems are freed from program development and storage problems by central program preparation and automatic down link loading: 1. Satellite applications source program is compiled or assembled (optional) 2. System cross loader builds satellite operating system from operator interaction or file input and relocates the object program for the target satellite 3. Relocated program or system is stored on central disc. Then: 4. Program or system is requested by satellite user program or operator (not shown: central station operator or programmer may issue request for RTE-C satellite, which may be unattended) 5. Satellite system sends request to central queuing module 6. Request is passed to program load monitor 7. Program or system is recalled from disc 8. Program or system is loaded into satellite 9. Completion reply is returned to requester.*

satellite. The data control block is required by the file management package for file-specific information and for a packing buffer. The system will allow up to 256 of these data control blocks concurrently, one for each of the maximum number of satellite files.

System access time to these data control blocks will be minimized if they are maintained in a core-resident table. However, the core consumed in an active system can be excessive. Core can be conserved if the data control blocks are maintained on disc, but this slows down control-block access. 9700 Distributed Systems solve this dilemma by dynamically maintaining only data control blocks for recently referenced files in core. If a file goes unused for an extended period of time, its data control block is "aged" as new requests are received. When a data control block is older than all other core-resident data control blocks, the next request for a new file will cause it to be transferred to an overflow disc file for later recall. The user can control the relative sizes of the core- and disc-resident portions of the data control block table at system generation time.

After the data control block has been assigned and all pre-execution conditions have been satisfied by the monitor, control is passed to the execution module. This module reassembles the original request and data from the transmission buffer, performs preliminary error checking, and executes the request under file subsystem control. The success or failure of the transaction is then transmitted back to the satellite system and then to the user program, thus completing the service of the request.

Besides the remote file access calls, the BCS satellite programmer has access to many of the requests for central system services (RTE EXEC calls) that are available to the central station programmer. The service requests are designed to aid in the synchronization of network times, events, and program control, and include a clock-time request, a program schedule request, and unit-record and instrument I/O requests.

The clock-time request returns the contents of the central station real-time clock to the satellite. The schedule request causes a central station program to be scheduled for immediate or time-delayed execution. Thus, for example, a central data reduction program can be scheduled to process data gathered by the satellite and stored at central. The unit record

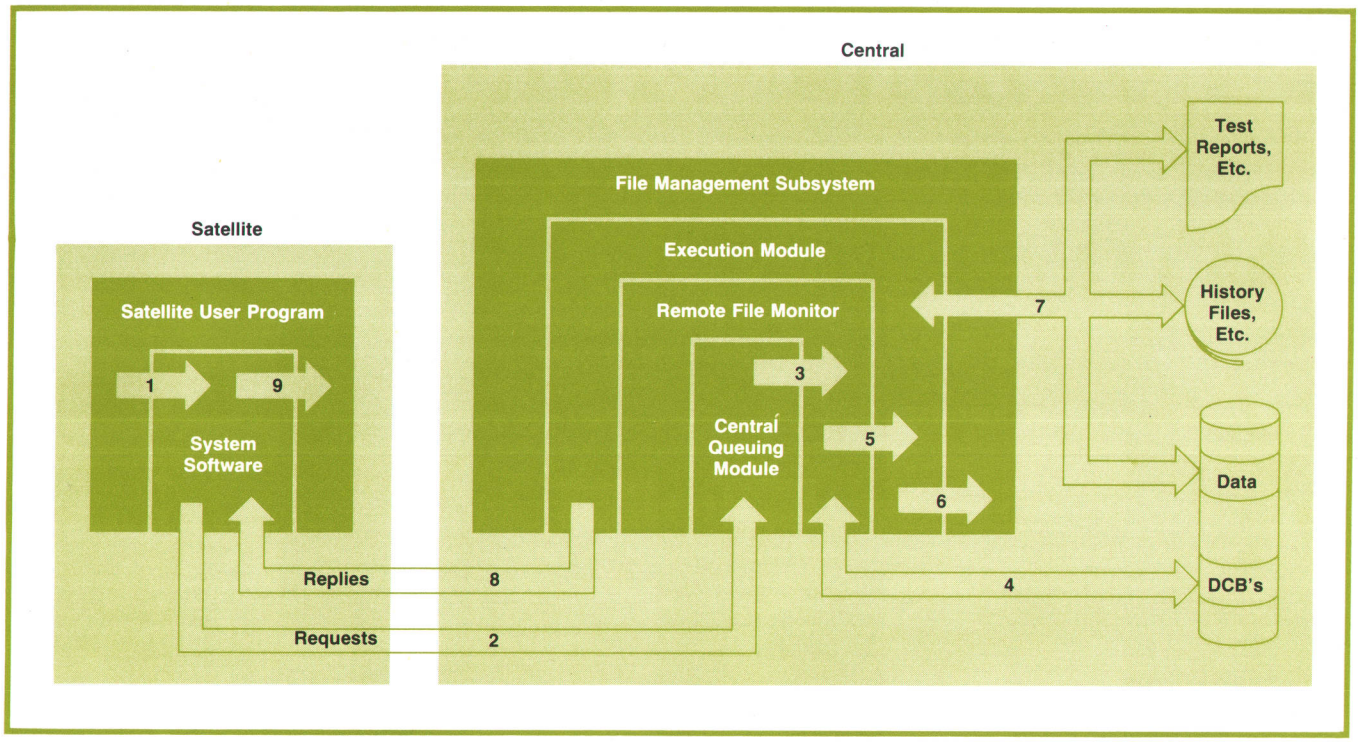


Fig. 4. *Central station data storage and file management capabilities are made available to the satellite programmer by remote file access: 1. Satellite user issues request to satellite system 2. Request is sent to central queuing module 3. Request is passed to remote file monitor 4. Monitor sets up "aged" data control block (DCB) 5. Monitor passes request to execution module to be formatted 6. Formatted request is passed to file management subsystem for execution 7. Data is read (written) from (to) the desired central peripheral 8. Request status and data are returned to satellite system 9. Status and data are returned to the requester.*

requests cause I/O control, status and read/write commands to be issued to central station devices or instruments. These requests are handled by the system in a manner analogous to that of the remote file access calls, except that data control blocks are not needed.

System Operator Interaction

Interactive operator commands provide file control and further enhance network program control. Satellite operator control of central files is accomplished by implementation of an operator interface for the commands to create, close, purge, and rename files. Program control is enhanced by providing an operator interface to the central station service requests already discussed. Also, the satellite operator can at any time cause the executing satellite test program to be terminated and, optionally, cause a new test program to be loaded into the satellite and executed.

Besides these interactive operator commands the software includes utility calls to allow the transmission of system messages from the satellite operator console to the central station console, to cause the central station real-time clock setting to be printed on the satellite console, and to list directories of program and data files on the satellite console.

The directory list feature is an operator utility request of particular interest. The satellite operator can request a local listing of all program and data files currently being maintained by the central station file manager. A partial listing may also be obtained.

A complete listing is obtained by entering the command "DLIST" on the SCE/3 satellite console. If the command is followed by a "filter" word of up to six ASCII characters, only those files whose names contain characters that match the filter characters are listed. Any number of characters up to six may be input; character positions to be ignored are specified by an asterisk. For example,

:DL[IST]	List all programs stored by the central system for the requesting terminal.
:DL[IST], *AB***	List only programs stored by the central system that contain "AB" in the specified position (e.g., CAB, IABLE, etc.).

While simple in concept, this feature provides broad flexibility when used with user-defined file naming conventions.

Satellites for Specific Applications

Distributed systems are a logical extension of computer-based measurement equipment designed for specific applications. HP offers such systems for a variety of applications. Those for automatic instrument testing and microwave network and spectrum analysis, now available as stand-alone systems, will soon be available as distributed system satellites. As satellites, 9500-Series and 8500-Series systems facilitate the preparation and coordination of programs and data for quality control, test and calibration histories, and related activities.

9500 Systems as Satellites

The 9500-Series Test Oriented Disc Systems (TODS) are designed for a variety of automatic test environments. As stand-alone systems, 9500 systems provide FORTRAN and Assembly Language programming capability in addition to the ATS-BASIC programming language and a flexible disc file management scheme. As satellites in a distributed system, 9500 systems attain even greater flexibility by gaining access to the RTE central's file structure, peripherals, and real-time operating system. Programs running in TODS share central station peripherals, schedule programs in the real-time environment of the central, transfer files between the file managers of the two operating systems, and create files on either disc from the measurement data obtained at the satellite. An interactive operator command package provides the satellite operator with capabilities similar to those offered to the satellite user program. In addition, message transactions between the operators at the RTE central and the TODS operator allow a manual hierarchy to be established in operator-governed distributed systems.

8500 Systems as Satellites

These microwave network analysis and spectrum analysis systems have been optimized for specific tests and are furnished with test programs that minimize user programming. Operated as stand-alone systems, their application programs use only the local computer peripherals. Data interchange between stations is possible, but only by transferring information on magnetic tape. In a distributed system, both of these limitations are removed. The central system disc file is now available for convenient loading of program and calibration data into the satellite. Measurement data can be stored on the central disc so that a summary of test results from several test stations is easily prepared.

RTE-C and RTE-B Satellites

Distributed system software has also been designed and implemented to couple satellites using the core-based real-time executive (RTE-C) and the real-time BASIC system (RTE-B) to a central RTE system. A major feature is a powerful capability for direct inter-computer program-to-program communication, which allows coordination of distributed processes without the need to rely on a file system. The satellite communication executives for the RTE-C and RTE-B satellites are SCE/5 and SCE/4, respectively.

Two different hardware systems support either the RTE-C or the RTE-B software. The 9601 is an integrated measurement and control system consisting of an HP 2100 Computer, unit record peripherals, and analog and digital input/output subsystems. This system is especially useful in laboratories, research and development environments, and similar smaller-scale applications. The 9610 is a larger industrial measurement and control system that provides expanded I/O capabilities and standard termination panels for data acquisition and alarming, data logging, manufacturing testing, and supervisory control applications.

Under the RTE-C operating system, FORTRAN, ALGOL, and assembly language user test programs can be executed. The ISA FORTRAN extensions for simplified digital and analog I/O and system scheduling functions are also supported.

The RTE-C operating system is a core-based subset of the powerful disc based real-time executive operating system used at the central station. RTE-C handles multiple user tasks in a multiprogramming and hardware-protected environment. With its incorporation into the distributed system network these features are retained and a host of others are offered. The SCE/5 satellite has remote file access to source programs stored on the central computer disc. An interactive command package is available to the satellite operator.

Equipped with the RTE-B operating system, stand-alone 9601 and 9610 systems provide the BASIC programmer with analog measurement, digital I/O, bit manipulation, plotting, and magnetic tape I/O. Incorporated into a distributed system, they gain many significant new features.

The SCE/4 satellite is unique in that BASIC test programs are prepared at the satellite and the results of the interactive sessions are stored by satellite operator command on the central station disc for later retrieval. These source files can be purged from the system, merged with additional BASIC program statements and loaded into the satellite for interpretation and execution, all by satellite operator commands that have been added to the real-time BASIC system. Once completed, the satellite programs can use the remote file access and program-to-program features of the system.

The SCE/5 and SCE/4 satellites retain all of the operator capabilities provided for the SCE/3 satellite. In addition, the central station operator has been given the ability to send a message to SCE/5 and SCE/4 satellite operator consoles, request the current real-time clock setting from RTE-C satellites, and schedule RTE-C programs for down-link loading and immediate or time-delayed execution. The central station can also invoke control and read/write operations on RTE-C and RTE-B satellite peripherals and request status information on these devices.

A feature of particular interest for factory automa-

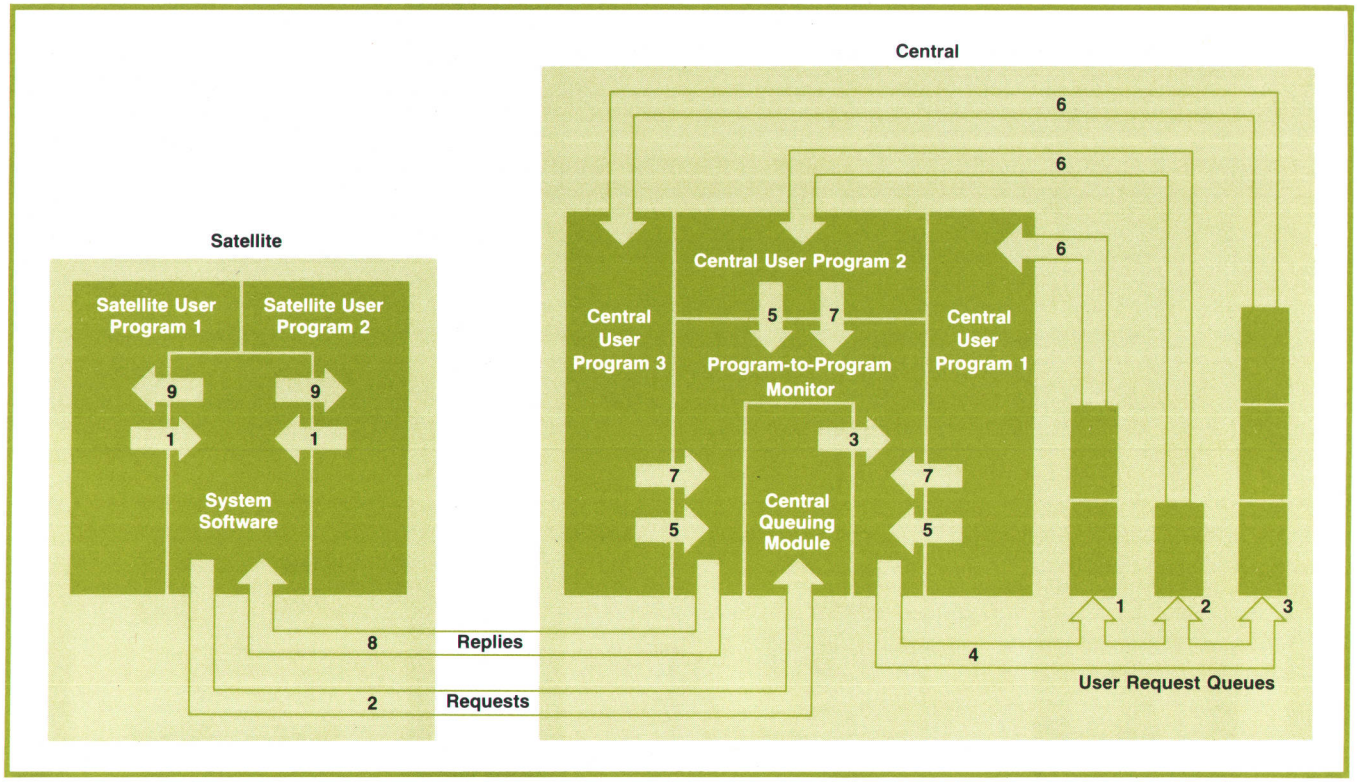


Fig. 5. *High-level-language programs in different computers communicate interactively via a transparent program-to-program communication interface: 1. Master satellite user issues request to satellite system 2. Request is sent to central queuing module 3. Request is passed to program-to-program communication monitor 4. Monitor schedules the receiving central user program if not active and queues requests for the specified central user program (three are shown) 5. Central user asks for its next request 6. Monitor passes next request to user for acceptance or rejection 7. Central user accepts or rejects requests 8. Monitor concludes request and sends reply to satellite system 9. Satellite system returns reply to user.*

tion and other applications that call for unattended satellites is forced down-link loading, offered with the SCE/5 satellite. This feature allows the central station operator or programmer to cause an application program to be sent to an unattended SCE/5 satellite and executed.

Program-to-Program Communication and Transportability

The remote file access capabilities previously described, expanded to include the RTE-C and RTE-B satellite types, manage a centralized data base quite well. However, to pass data from one executing program to another using remote file access, an intermediate file structure is required. The direct program-to-program communication capability, Fig. 5, eliminates this intermediate step and also allows the coordination of many programs executing in various network computers simultaneously.

A feature of primary importance in both remote file access and program-to-program communication is that of transportability. Our goal here was the standardization of the user/system interface so that central station user programs could be executed without modification in a satellite environment (that is, transported) and vice versa, when dictated by network needs.

The program-to-program facility was designed to permit the FORTRAN, ALGOL, and BASIC programmer to send and receive data to or from another program executing in another computer by means of simple library subroutines. All coordination of program execution and data transfer is handled by the system, leaving the application programmer free to concentrate on the design of the data collection and measurement tasks specific to his installation. The system is designed so a program executing in the central computer can communicate with several programs executing under RTE-C and RTE-B satellite operating systems simultaneously.

To further ease the burden on the application programmer the system provides a "tag field" as part of each system call. This tag field is constructed by the request originator and shipped by the system to the receiver, who may interrogate and modify it before it is returned to the originator as part of the request-completion information. The decision to use the tag field as well as its specific contents remains with

RTE File Management Package

The remote file access commands provide the satellite programmer with the facilities of the real-time executive file management package. The highlights of this powerful package are as follows.

Multiprogramming and File Integrity

Of key importance in a distributed multiprogramming RTE system is avoidance of file conflicts. The RTE file manager provides a variety of options that permit file access and file security to be optimized file-by-file to satisfy requirements. Up to seven different programs can have the same file open simultaneously, or a file may be opened exclusively to just one program. Simple, easy-to-use security codes restrict files to designated programs and users and control the nature of their access (read only or read and write). It is also possible to leave access to files unrestricted.

Often the security of the filing system is just as important as its integrity. Data in certain files may be of a confidential nature, making it necessary to restrict read as well as write access. It may be necessary to assure that data in other files comes from only one source, so only that source can be given write access to those files. The same security codes that can be used to safeguard file integrity also form the basis of a file security scheme that can be as comprehensive as desired.

The file manager provides for calling programs and data files by name. This spares the programmer the inconvenience and time required for detailed track and sector addressing.

File Manager Calls

Remote Program Calls		Purpose
remote file	create	Creates a central station file; does not store data.
remote file	absolute position	Positions a central station file to a known record address.
remote file	open	Opens a desired central station file.
remote file	control	Sends RTE control request to central station file.
remote file	read	Transfers one record from central station file to satellite user buffer.
remote file	write	Transfers one record from satellite user buffer to central station file.
remote file	position	Directs next read write to a specified record.
remote file	rewind	Resets central station file to first record.
remote file	rename	Renames specified central station file.
remote file	disc directory access	Returns 125 words of central disc directory.
remote file	status	Returns central station file status, including position of record pointer.
remote file	close	Closes a central station file.
remote file	purge	Purges central station file and directory entry.

All requests are callable from FORTRAN, ALGOL, BASIC, or HP Assembly Language.

Peripheral Device Control

An optional feature of the file manager, one offering real convenience to the user, is peripheral device control by means of file manager commands. This is established by a file directory entry for the magnetic tape unit, photoreader, punch, line printer, or other peripheral device that is to be controlled. After this directory entry has been established, the device can be controlled by the file commands. One important benefit of peripheral control via the file manager is that a program can obtain undivided access to a peripheral in the multiprogramming environment. For example, a satellite program can issue an exclusive open to a file that is designated as a line printer, locking out other network programs until a needed listing is completed.

the application programmer using the system.

The program-to-program facility also provides for communication between CCEs (central communication executives) in different central computers. This makes it possible to interconnect several distributed system networks to form a "supernetwork."

Using Program-to-Program Communication

Program-to-program communication is implemented by means of eight subroutine calls. These are divided into two types. The first type, the master requests, consists of the calls: POPEN, PREAD, PWRIT, and PCONT (program-to-program open, read, write, and control). These calls treat the other program as a slave input/output device and have logical counterparts in the RTE file system. The second type of call, the slave request, includes the calls: GET, ACEPT, REJCT, and FINIS (get next request, accept last request, reject last request, terminate communication). These calls are used to receive the master calls from the system and, after examination of the tag field, to instruct the system to return the tag field to the requester and to complete or terminate any pending data transfer. The FINIS call removes the slave program from active communication with its master requesters.

When a master program-to-program communication request is issued by a satellite user program, control is passed to an interface subroutine that assembles calling parameters, system information, the user's tag field, and optional data into a transmission buffer. The system then causes the buffer to be shipped to the central station via the communication driver.

A master POPEN request received at the central station causes the system to schedule the required central station program (if not already scheduled) and to pass the POPEN request to that program upon execution. If after examination of the tag field the pro-

gram accepts the POPEN request, a queue is created by the system for the PREAD, PWRIT and PCONT requests to follow, and the updated tag field is returned to the originator. Subsequent POPEN requests for this same program will be passed through to the executing program and the existing queue used.

The ensuing PREAD/PWRIT requests received at the central station cause the tag field to be passed to the executing program. If the request is accepted by the central program, the system causes the associated data field to be written to or read from the queue previously created for the program in question. At completion the updated tag field is returned to the requester. Rejected PREAD/PWRIT requests cause the data to be purged from the system. PCONT requests are passed through the system to the executing program for tag examination. Thus the PCONT request allows the exchange of small data fields without the overhead required to process PREAD and PWRIT requests.

Acknowledgments

I am indebted to project engineer Larry Pomatto for his help in evolving many of the concepts discussed here, for programming support on the RTE-B and central software, and for his consistent willingness to "go the extra mile." I would also like to thank project engineer Jim Hartsell for the BCS and RTE-C satellite software, which he thoughtfully prepared and executed; project engineers Prem Kapoor and Barbara Packard for 9500 and 8500 satellite software; George Anzinger, group leader for operating systems, for his many system tools that helped make the project possible; Andy Danver and Dave Borton, for product marketing support; Joe Bailey, Bob Shatzer, and Hal Sindler, for encouragement, enthusiasm, and project, field, and training support; and finally, many allied project members.

SPECIFICATIONS
Distributed Systems

These specifications are for distributed system hardware and software only. Specifications for central and satellite systems available on request.

91700A
Central-to-Satellite Distributed System

CENTRAL COMMUNICATES WITH: BCS, RTE-B, and RTE-C satellite systems

SOFTWARE: Central Communications Executive, including data communications driver

HARDWARE: Serial Data Communications Interface, hardwired or modem version

HARDWIRED CABLE:

LENGTHS (feet)	1 to 600	601 to 1200	1201 to 2000	2001 to 3000	3001 to 4000	4001 to 5400	5401 to 7300	7301 to 10,000
LINE SPEED (kbps)	1000	500	250	125	250	125	62.5	31.25

MODEM CONNECTION: Distance is limited only by telephone network; line speed is determined by choice of line and modem and can range up to 20,000 bits per second.

MEMORY REQUIRED:

CPU-RESIDENT: 500 words plus user-defined system buffer area for use by all RTE central modules and the system.

DISC-RESIDENT: 3300 words of real-time disc-resident area and 6080 words of background disc-resident area.

MINIMUM CENTRAL SYSTEM MEMORY: 24K words.

Satellite Systems

	BCS Satellite			RTE-B Satellite		RTE-C Satellite	
Uses Satellite Communication Executive	SCE1	SCE2	SCE3	SCE1	SCE4	SCE1	SCE5
Memory Required (words) for Operating System (including BASIC interpreter in RTE-B system), SCE, and Data Communication and System Console Drivers	2150	2,860	4,590	11,620	14,890	6,710	10,000
Additional Memory (words) for REMAC (RTE-C Operator Communications Interface)							1,660
Minimum Recommended System Memory Size	4K	4K	8K	16K	16K	8K	16K
I/O Channels Used for Data Communication Interface	1			1		1	
Languages: FORTRAN, ALGOL, HP Assembly	×					×	
Real-Time BASIC				×			

91703A

SOFTWARE: Satellite Communications Executives 1, 2, and 3 including data communication driver for use on BCS based computer systems.

HARDWARE: Two Serial Data Communications Interfaces, Hardwired or Modem.

91704A

SOFTWARE: Satellite Communications Executives 1 and 4 including data communications driver for use on RTE-B based computer systems.

HARDWARE: Two Serial Data Communications Interfaces, Hardwired or Modem.

91705A

SOFTWARE: Satellite Communications Executives 1 and 5 including data communications driver for use on RTE-C based computer systems.

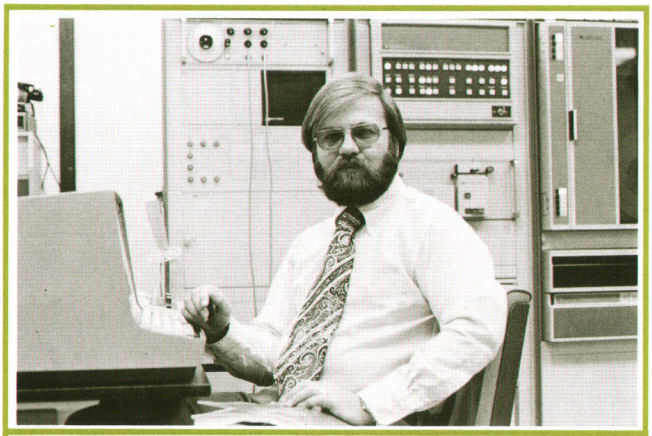
HARDWARE: Two Serial Data Communications Interfaces, Hardwired or Modem.

PRICES IN U.S.A.:

91700A, $3500.

91703A, 91704A, 91705A, $4000 each.

MANUFACTURING DIVISION: AUTOMATIC MEASUREMENTS DIVISION
974 East Arques Avenue
Sunnyvale, California 94086 U.S.A.



Shane Dickey

Before coming to HP in 1972, Nebraskan Shane Dickey specialized for five years in real-time minicomputer systems design and implementation for process and supervisory control. As project manager for HP 9700 Distributed Systems, he has guided that project from inception to production. He's a member of ACM and author of a pair of professional papers on distributed systems. A 1966 graduate of California State University at Long Beach, Shane holds a BA degree in mathematics. He lives in Sunnyvale, California, but is building a new house in the nearby Santa Cruz mountains with a solar heating system that he designed. Other interests include sailing, woodcarving, scrimshaw, and stained glass. Shane and his wife, a systems programmer, have just welcomed their first child, a boy.

A Quality Course in Digital Electronics

This practical approach to the teaching of digital integrated circuit principles includes hardware, a textbook, and a 26-experiment laboratory workbook.

by James A. Marrocco and Barry Bronson

ADVANCES IN DIGITAL TECHNOLOGY and a resultant decline in IC prices have spurred tremendous growth in both the use and complexity of digital integrated circuits. This rapid change has created training problems for educational institutions, military schools, and companies that train their own personnel. Needed are new teaching tools that are comprehensive and efficient, yet adaptable to changing technology.

The Hewlett-Packard Model 5035T Logic Lab, Fig. 1, was developed to meet this need by providing a complete, quality course in practical digital electronics. The logic lab is an educational training package consisting of hardware, textbook, laboratory workbook, and all required parts and troubleshooting tools; in short, everything needed to train newcomers to digital circuitry.

About the Lab

We felt the lab should be easy to use, even for a complete novice, and that it should provide hands-on experience with current digital circuits. At the same time, the goals for the lab were such that it had to be designed to full Hewlett-Packard quality standards. Outside consultants—an educator and a journalist—were contacted to help work out any bugs in the course. We also felt strongly that the mainframe should meet environmental tests to insure that it would be rugged and dependable over many years of rough use. Also, to acquaint the student with digital troubleshooting techniques, we included the 10525T Logic Probe, the 10526T Logic Pulser, and the 10528A Logic Clip, and we made them an integral part of many of the 26 experiments contained in the course.

Beyond educational needs, we felt that the lab would be used as a breadboarding tool, much as we have used it to help design new digital devices here in our own plant. So, the lab power supply was designed to provide enough power to supply several fully loaded breadboards—a handy feature when complicated circuits are being designed.

The Hardware

Logic lab hardware consists of the mainframe, an assortment of 32 integrated circuits, pre-stripped

Fig. 1. *Model 5035T Logic Lab includes everything needed to train newcomers to digital integrated circuits: hardware, textbook, laboratory workbook, and all parts and troubleshooting tools.*

wires for circuit interconnection, four fully decoded LED numeric indicators, an IC extractor, the removable breadboard, and the three IC troubleshooters—probe, pulser, and clip.

The mainframe is made of polycarbonate foam with rounded corners and a 15° canted front panel for ease of use. The cover is attached to the mainframe underbody with just four screws, and when the cover is removed all circuit components are easily accessible for checkout and servicing.

The breadboard is held in place by two magnetic strips, making it easily removable by pressing on the bottom edge. Thus several students can use the same mainframe, or a single user can build several circuits simultaneously using the same mainframe.

Integrated circuits and interconnecting wires are pushed into the breadboard connection points: no soldering is necessary.

Four buffered light-emitting diodes (LED's) are located on the front panel above the breadboard. These act as indicators for circuits installed in the breadboard. Also, six "bounceless" switches provide clean steps without false switching caused by contact bounce.

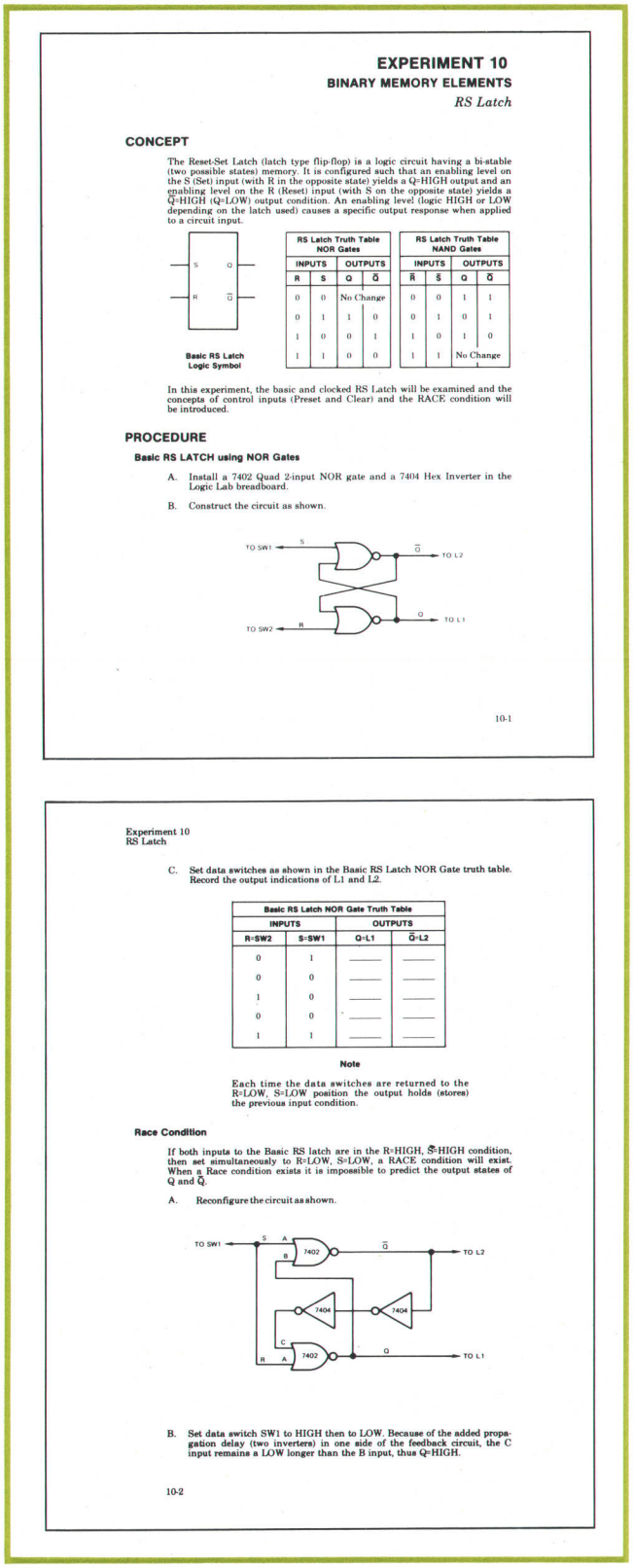
Inside, the mainframe contains a five-volt, one-ampere power supply and clock generators at two frequencies: 1 Hz and 100 kHz. The TTL compatible circuits in the mainframe are all fully short-circuit protected.

Two rear-panel connectors provide five-volt power for the logic probe and the logic pulser. The logic probe's indicator lamp shows the instantaneous logic state of any point in a circuit: it is off for logic lows, bright for logic highs, and dim for bad levels. Fast pulses are stretched and displayed at 10 Hz. The logic pulser drives any circuit node to its opposite state when the button on its body is pressed. Together the pulser and probe provide a stimulus-response test capability that is helpful in building circuits, troubleshooting, and learning how digital circuits work. The logic clip lets a student see the logic states of all pins of 14-pin or 16-pin TTL circuits at the same time, a valuable aid to comprehension.

The Books

While the logic lab hardware was being designed, a search was begun for software to go with it. It quickly became apparent that there were no textbooks or laboratory workbooks that met the project's objectives for quality, completeness, conciseness, practicality, and ease of learning. Therefore, the software was made a part of the logic lab development project. The result was two new books, an introductory text in practical digital electronics, and an accompanying 26-experiment laboratory workbook.

The text is aimed at digital novices. It takes the student from a discussion of 1's and 0's up through the most important TTL circuit elements in current use. Chapter titles are:



EXPERIMENT 10
BINARY MEMORY ELEMENTS
RS Latch

CONCEPT

The Reset-Set Latch (latch type flip-flop) is a logic circuit having a bi-stable (two possible states) memory. It is configured such that an enabling level on the S (Set) input (with R in the opposite state) yields a Q=HIGH output and an enabling level on the R (Reset) input (with S on the opposite state) yields a Q=HIGH (Q=LOW) output condition. An enabling level (logic HIGH or LOW depending on the latch used) causes a specific output response when applied to a circuit input.

Basic RS Latch Logic Symbol

RS Latch Truth Table NOR Gates

INPUTS		OUTPUTS	
R	S	Q	$\overline{Q}$
0	0	No Change	
0	1	1	0
1	0	0	1
1	1	0	0

RS Latch Truth Table NAND Gates

INPUTS		OUTPUTS	
$\overline{R}$	$\overline{S}$	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	No Change	

In this experiment, the basic and clocked RS Latch will be examined and the concepts of control inputs (Preset and Clear) and the RACE condition will be introduced.

PROCEDURE

Basic RS LATCH using NOR Gates

A. Install a 7402 Quad 2-input NOR gate and a 7404 Hex Inverter in the Logic Lab breadboard.

B. Construct the circuit as shown.

10-1

Experiment 10
RS Latch

C. Set data switches as shown in the Basic RS Latch NOR Gate truth table. Record the output indications of L1 and L2.

Basic RS Latch NOR Gate Truth Table

INPUTS		OUTPUTS	
R=SW2	S=SW1	Q=L1	$\overline{Q}$=L2
0	1	____	____
0	0	____	____
1	0	____	____
0	0	____	____
1	1	____	____

Note

Each time the data switches are returned to the R=LOW, S=LOW position the output holds (stores) the previous input condition.

Race Condition

If both inputs to the Basic RS latch are in the R=HIGH, S=HIGH condition, then set simultaneously to R=LOW, S=LOW, a RACE condition will exist. When a Race condition exists it is impossible to predict the output states of Q and $\overline{Q}$.

A. Reconfigure the circuit as shown.

B. Set data switch SW1 to HIGH then to LOW. Because of the added propagation delay (two inverters) in one side of the feedback circuit, the C input remains a LOW longer than the B input, thus Q=HIGH.

10-2

Fig. 2. *Typical pages from the laboratory workbook.*

The Nature of Digital Logic
Decision-Making Elements
Memory Elements
Data and Data Communication
Integrated Circuits and Logic Families
Shift Registers, Counters, and Combinational Logic Circuits
Arithmetic Elements
Memories

Three appendixes cover numbering systems, data communication codes, and Boolean algebra.

The laboratory workbook gives the student experience working with the devices covered in the textbook and with the logic lab hardware. The 26 experiments are divided into nine groups:

Logic Lab Familiarization (2 experiments)
Individual Logic Gates (7 experiments)
Binary Memory Elements (3 experiments)
Sequential Logic (4 experiments)
Data Handling Circuits (2 experiments)
Arithmetic Elements (4 experiments)
Memories (2 experiments)
Signal Conditioning Devices (1 experiment)
Simplification of a Logic Design (1 experiment)

Each experiment concludes with self-test questions to check the student's comprehension. Fig. 2 shows portions of a typical experiment from the laboratory workbook.

Acknowledgments

The authors wish to thank everyone who contributed to the evolution of the Logic Lab, especially the following. Initial electrical design: Chuck Taubman. Textbook author and editor: Mark Baker and Juris Blukis. Workbook author and editor: Roy Schmidt and Maurice Bird. Manufacturing coordination: Roy Ingham. Manufacturing plastic development: Bill Hassel. Marketing coordination: Jesse Pipkin. Service coordination: Jack Nilsson. Production introduction: Roy Criswell. Production line assembly leaders: Walt Johnson and Larry Ligon.

Barry Bronson

Barry Bronson came to HP in 1971. Since then, he's developed automatic test systems for HP VHF integrated circuits and for the 5000A Logic Analyzer, and completed the electrical design of the 5035T Logic Lab. Born in Los Angeles, Barry received his BS degree in engineering from the University of California there in 1970, and is now nearing completion of his work for the MSEE degree at Stanford University. He's also involved in a videotape equipment business venture, and spends a good deal of his spare time tinkering (his wife's word) on several projects. The Bronsons live in Campbell, California and enjoy bicycling and traveling.

SPECIFICATIONS
HP Model 5035T Logic Lab

POWER SUPPLY
VOLTAGE: +5 ±5% over load range
LOAD RANGE: 0—1 ampere
RIPPLE: 10 mV rms max
SHORT-CIRCUIT PROTECTION: continuous

SWITCHES: (6, bounce-free operation)
OUTPUT: TTL logic levels
FAN-OUT: 10 TTL loads (will sink >16 mA)

CLOCKS: (2)
FREQUENCY: 1 Hz ±30%, 100 kHz ±30%, nominal squarewave
OUTPUT: TTL logic levels
FAN-OUT: 10 TTL loads (will sink >16 mA)

INDICATORS: (4)
INPUT: indicators on above +0.6 volts
INPUT IMPEDANCE: >40kΩ(<1 TTL load fan-in)

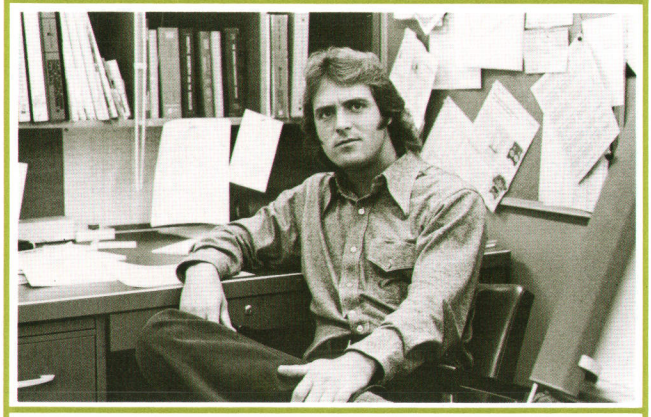
POWER REQUIREMENTS
VOLTAGE: 100, 120, 220, 240 volts +5%,−10% 48—440 Hz
POWER DISSIPATION: 30 Watts max
TEMPERATURE RANGE: 0—55°C

WEIGHTS
NET: Lab only, 5 lbs, 10 oz. (2.55 kg); with case and documentation 13 lbs (5.9 kg)
SHIPPING: Lab only, 7 lbs, 12 oz. (3.5 kg); with case and documentation 15 lbs, 2 oz. (6.86 kg)

DIMENSIONS
Lab only: Height 3 1/2" (89 mm), Width 12 1/4" (311 mm), and Depth: 10 1/2" (267 mm)

PRICE IN U.S.A.: $695.

MANUFACTURING DIVISION: SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.



James A. Marrocco

Jim Marrocco was project leader and did the mechanical engineering for the 5035T Logic Lab. With HP since 1970, he's also contributed to the design of the 5510A Compensator and the 5000A Logic Analyzer. A 1970 graduate of California State Polytechnic College at Pomona, he holds a BS degree in mechanical engineering, and is now working on his MS degree in cybernetic systems at San Jose State University. He's married and lives in San Jose.

Simplified Data-Transmission Channel Measurements

Synthesized signal generation and a dual time-interval measurement simplify evaluation of group delay and attenuation distortion in voice-grade telephone lines used for transmitting digital data.

by David H. Guest.

INCREASING WORLD-WIDE DEMAND for data transmission facilities is resulting in ever-higher bit rates being pressed on to voice communications channels—channels that were never intended for digital communications. The transmission quality of these lines thus becomes of concern to a growing number of users.

Two important characteristics a transmission channel needs for data transmission are constant group delay and constant attenuation across the frequency spectrum of the modem's transmitted signal. Serious deviations from this ideal cause signal distortions that result in misinterpretation of the digital symbols by the receiving modem, particularly at high bit rates. The group delay characteristic, which is of no importance in voice communications, therefore becomes significant in circuits to be used for the transmission of high-speed data.

Recently described in these pages was the Model 4940A Transmission Impairment Measuring Set,[1] an instrument that, among several other measurements, determines group delay according to standards established for North American telephone networks. The new Model 3770A Amplitude/Delay Distortion Analyzer (Fig. 1) to be described here measures group delay according to CCITT standards which prevail in

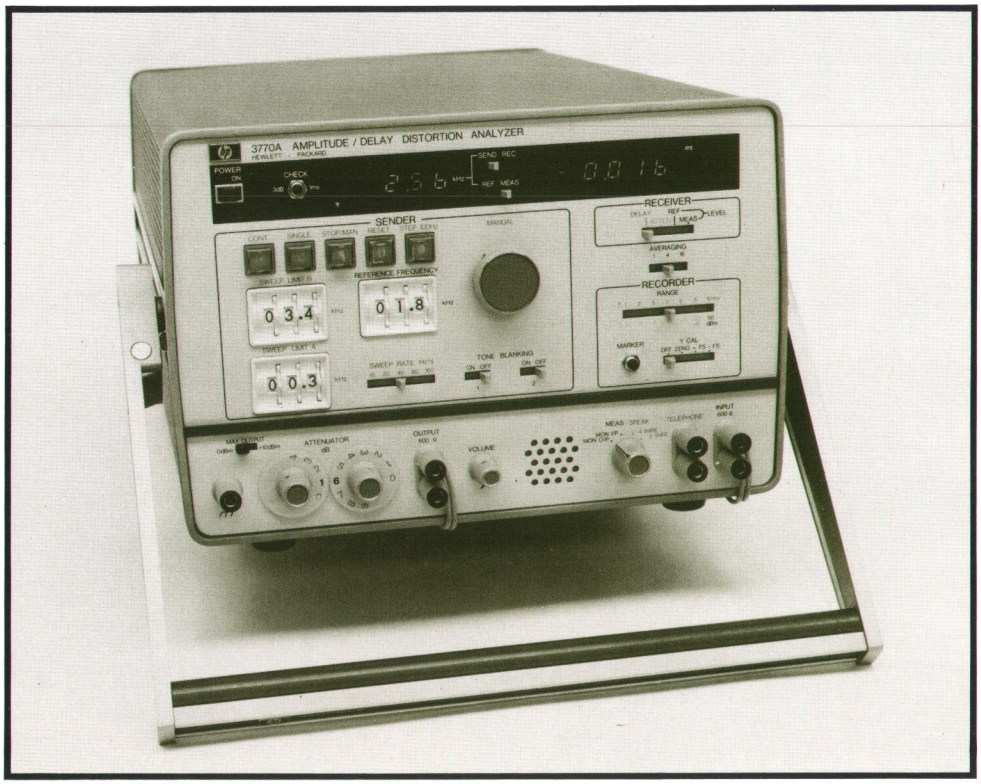


Fig. 1. *Model 3770A Amplitude/Delay Distortion Analyzer measures the quality of voice channels used for transmitting digital data. Both the sender and receiver are combined in a single portable unit.*

most of the rest of the Western world and on international circuits. However, it is expected that data channel users in all parts of the world will want this instrument to check out the quality of their circuits, particularly because of its compactness and unprecedented ease of use.*

To ensure compatibility between countries and manufacturers, CCITT has specified standards for the operation and performance of audio group delay and attenuation distortion measuring equipment (see box). Not only does the Model 3770A meet these compatibility requirements, but it also incorporates principles that give significantly improved accuracies over those recommended. At the same time, operation has been simplified so that relatively untrained personnel can achieve accuracies hitherto possible only in the laboratory.

In addition to measuring relative group delay and attenuation, the Model 3770A also fills the role presently occupied by traditional level-measuring equipment since the receiver can measure absolute levels, and the output level of the sender is calibrated.

Basic Operation

A simplified block diagram of the new Model 3770A Amplitude/Delay Distortion Analyzer is shown in Fig. 2. The instrument combines sender and receiver in one unit. Although they share the same power supply and frequency display, sender and receiver are essentially independent and operate simultaneously. With two analyzers, a pair of channels can be evaluated in both directions at the same time. Otherwise, only the sender or receiver section is used at either end for single-path measurements. The analyzer may also be used either as a sender or as a receiver with other equipment that conforms to CCITT standards.

The Model 3770A operates as follows:

- The reference frequency is set by a thumbwheel switch. 1.8 kHz is generally used but any other frequency from 0.4 to 19.9 kHz is selectable in 100-Hz steps.
- For swept-frequency measurements, the sweep limits of the measurement frequency are selected by two thumbwheel switches in a range from 0.2 to 19.9 kHz in 100-Hz steps, a range that allows measurement of special purpose audio channels as well as voice channels. Sweeps can be single or repetitive.
- The output level is selected. The output range is 0 to −49 dB (600Ω) in 1-dB steps.
- The operator then commands the instrument to sweep once, or to sweep repetitively.
- The operator at the receiving end merely selects the type of measurement to be made (delay or attenuation) and the instrument then displays frequency and delay over a range of −10 to +10 ms (or attenuation in a ±40 dB range or level in a −50 to +10

*The Model 1645A Data Error Analyzer,[2] also for checking digital transmission channels, measures overall digital-to-digital performance but does not directly characterize the analog channel itself.

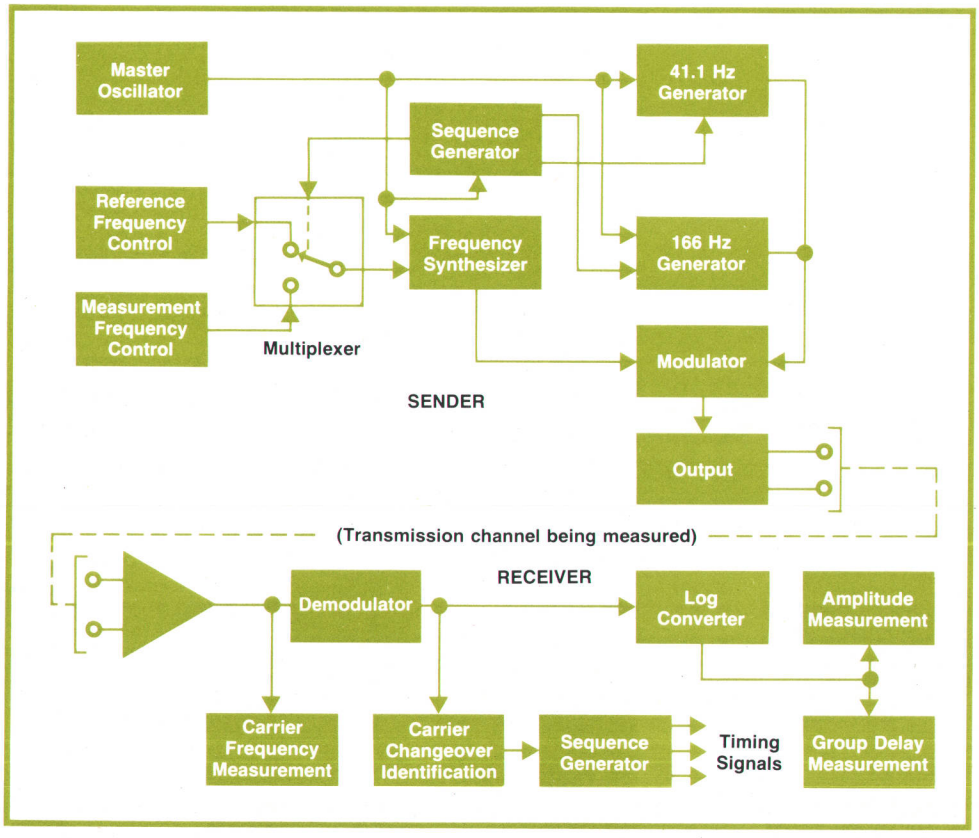


Fig. 2. *Block diagram of the Model 3770A Amplitude/Delay Distortion Analyzer. Sender and Receiver sections share the same power supply and frequency display but operate independently.*

Measurement of Amplitude and Delay Distortion

Group delay, often referred to as envelope delay, is the delay in transmission of information modulated on a carrier. In general, it is not the same as the phase delay of the carrier itself.

In a group delay measurement, the modulating frequency remains constant while the carrier frequency is stepped or swept across the frequency band of interest. Phase delay in the *modulating* envelope as the *carrier* frequency varies is a measure of group delay.

It is not possible to measure absolute group delay in an end-to-end measurement but neither is this of any special interest. The important characteristic is relative group delay. This must be constant over the band of frequencies of interest, else it will introduce distortion in a complex waveform.

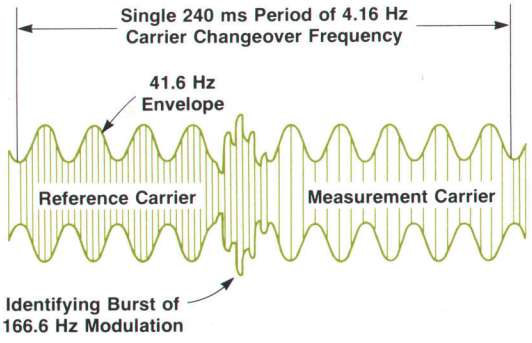
Two techniques for measuring group delay have been in common use. One requires an auxiliary channel either for transmitting a reference signal for phase comparison with the test signal at the receiving site, or for returning the test signal envelope on a fixed carrier to the transmitting site for comparison there. The other technique, applicable to short-term measurements, uses a stable crystal-controlled oscillator to recreate the envelope as a reference at the receiving site.

The technique specified by CCITT (International Telegraph and Telephone Consultative Committee) in Recommendation O.81 supplies the reference envelope to the remote receiver on the same channel as the test signal. The two carriers are transmitted sequentially in alternate time slots, as shown in the diagram. Differing group delays in the channel at the measuring and reference carrier frequencies result in a phase difference between the envelopes of the two modulated carriers at the receiving end. A measurement of this phase difference, expressed as a time interval, is the measure of group delay.

Differing channel attenuations at the two carrier frequencies lead to differing received carrier levels, giving a measure of attenuation-vs-frequency distortion. Clearly, this and the group-delay measurement must be accompanied by frequency information, so the receiver must be able to determine the measuring frequency in use at any moment.

The envelope frequency and the rate of carrier changeover are included in the CCITT recommendation. To synchronize the receiver operation to the carrier changeover, the recommendation includes a 4-cycle burst of identifying modulation inserted at the end of each reference carrier period.

Also included is a specification of the instants that the signal is sampled for measurement information. To allow time for switching transients to die down, measurements are made within a 24-ms window just prior to the carrier changeover.



CCITT standard group delay and attenuation test signal.

dBm range). No range setting is required.

The instrument also has X-Y recorder outputs for obtaining graphs of delay and/or attenuation vs frequency (Fig. 3).

For single-frequency measurements, the measuring frequency is selectable manually in 10-Hz steps. Spot checking a channel is facilitated by a front-panel pushbutton that steps the frequency in precise 100-Hz increments.

A rear-panel switch converts the instrument to an unmodulated level measurement mode for absolute level measurements. Modulation is removed and carrier changeover is inhibited so that a pure tone at the measurement frequency is transmitted. All of the measurement frequency controls are effective in this mode.

Optional features allow for loopholding and for tone blanking. With the latter option, selected frequency bands are skipped during a sweep so the test will not activate signalling-tone equipment.

Group Delay Measurement

In the past, group-delay measurements commonly relied on a measurement of envelope *phase* shift. Knowing the envelope frequency, ω_e, it is possible to scale the phase shift $\Delta\theta$ to arrive at group delay, $\Delta\theta/\omega_e$. However, any deviation in the envelope frequency from its nominal value results in an error. Although the CCITT recommendation allows up to 1% envelope frequency error, an early design objective of the 3770A was to eliminate this source of errors by eliminating envelope frequency as a parameter in the measurement. This was done by using a dual time-interval measurement to derive group delay directly without the need for phase scaling.

Group delay is the time interval t_g indicated in Fig. 4, which shows the demodulated waveform at the receiving end when the channel being measured suffers both relative group delay and relative attenuation between measurement and reference frequencies. A non-delayed waveform would appear as the dashed line in the measurement interval.

The dashed line would not exist in reality, however, so the measurement must be made with respect to the adjacent reference frequency periods. In the Model 3770A, the reference points are the first zero-axis crossings (points A and A′) after the beginning of the 24-ms acceptance "window". The instrument then measures t_1, or A to B, and t_2, or B to A′. Since $t_1 - t_g = t_2 + t_g$:

$$t_g = \frac{t_1 - t_2}{2}$$

Using this technique, total reading errors in group delay measurement with the 3770A are less than 5 μs ±1% of reading from 0.6 to 20 kHz (see specifications, page 24). No adjustments are required on the

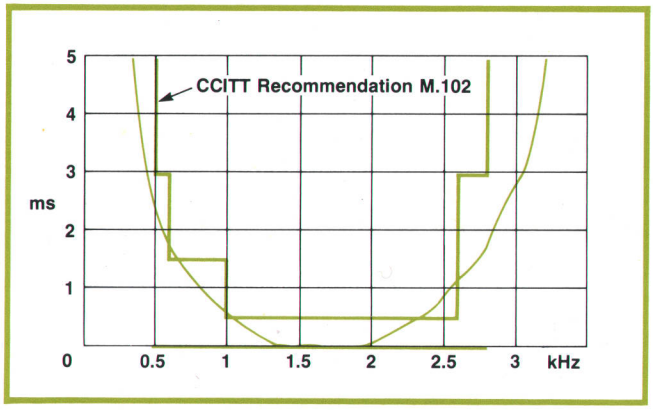


Fig. 3. *Recording of a typical group delay measurement, this one being made over an international data circuit that included two satellite hops. The recording shows that the channel does not quite meet the requirements of CCITT performance recommendation M.102 and thus needs suitable equalization near the band edges.*

part of the operator to obtain this accuracy.

Precision Carrier Frequency Control

The test waveform recommended by CCITT for group delay measurements demands unusual agility on the part of the sender carrier frequency. To implement this with accuracy but without requiring awkward adjustments on the part of the operator, digital waveform synthesis is used.[3]

A diagram of the synthesizer is shown in Fig. 5. Within a read-only-memory (ROM) the equivalent of some 2^{15} words are stored, corresponding to equispaced samples of a sine wave taken over exactly one waveform cycle. The ROM is addressed by an accumulator whose 15-bit contents at any instant correspond to a sinewave angle. On each clock pulse, the accumulator is incremented by an amount proportional to the desired output frequency. This is accomplished by adding the increment to the previous word and storing the result.

The output of the ROM is applied to a digital-to-analog converter, generating a sampled-and-held stepped sinewave as the accumulator steps the ROM through the indicated addresses. Because the stepping frequency is many times higher than the sinewave frequency, low-pass filtering easily removes the steps to give a clean sine wave. Fig. 6 shows the output spectrum while the synthesizer is generating a 1-kHz tone. Except for harmonics of 1 kHz, spectral components are more than 80 dB below the fundamental.

Clearly, the output frequency is proportional to the speed with which the addressing advances through the sample table stored in the ROM. Higher frequencies thus have fewer samples per cycle. To simplify the filtering, the clock rate was made high enough (327,680 Hz) to generate about 16 samples per cycle at the highest output frequency (20 kHz). The clock rate is exactly 10× the number of stored samples (2^{15}) so the lowest output frequency would be 10 Hz and all other frequencies are multiples of 10 Hz. The low end of the instrument's range, however, is restricted to 0.2 kHz.

Several advantages accrue from use of this synthesis technique. First of all, the output frequency is controlled by the clock frequency, which is derived from a crystal-controlled oscillator. The accuracy of any output frequency is within ±0.1%.

Second, digital control gives flexibility and general ease in frequency control. Frequency is set precisely, and the sweep limits are accurate.

Third, switching between reference and measurement frequencies causes no transients in the output. A change in frequency is effected simply by incrementing the ROM address by a new value. Hence, there is no jump in phase when the frequency is changed.

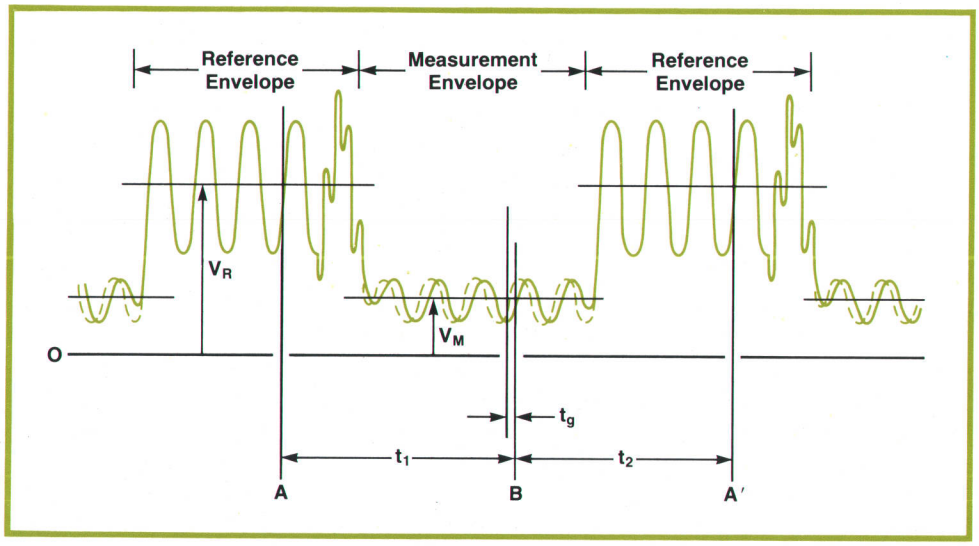


Fig. 4. *Demodulated envelope of received waveform that was subject to relative group delay (t_g) and relative attenuation (V_R/V_M).*

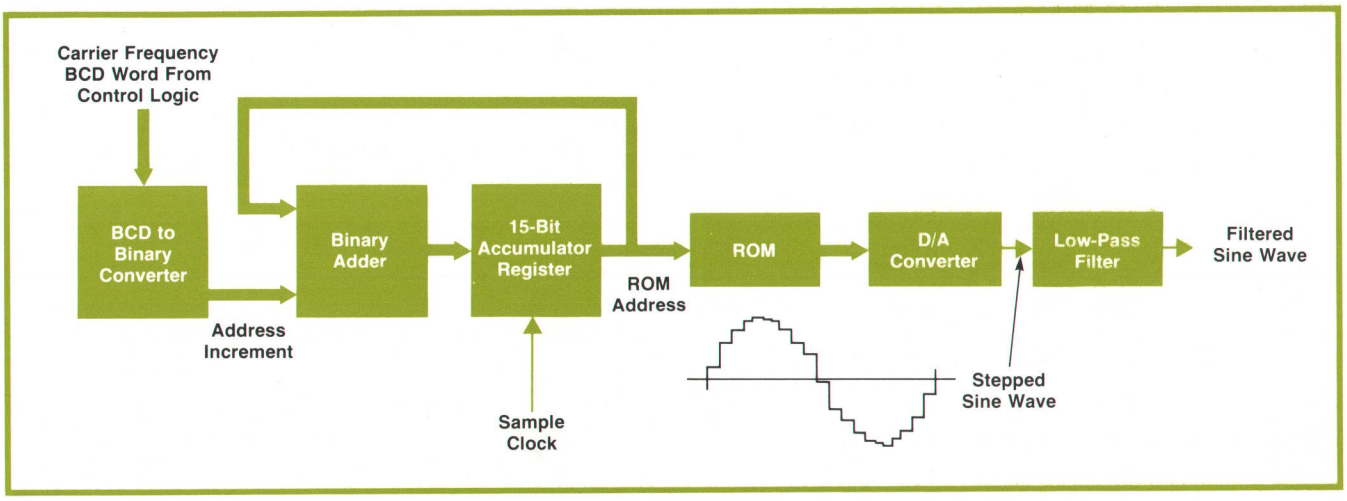


Fig. 5. *Synthesizer output frequency is determined by the clock frequency (crystal-controlled in the Model 3770A) and by the magnitude of the address increment.*

ROM Reduction

In practice, storage of 32,768 (2^{15}) sinewave samples would have been economically impractical. An immediate four-fold reduction is achieved by storing samples for one quadrant only, and reusing the data appropriately to derive the other quadrants.

A further reduction of significant proportions was achieved by use of the relationship (valid for small B):

$$\sin (A+B) = \sin A + \cos A \cdot \sin B$$

A relatively few values of A may then be used to give coarse angular resolution and small values of B can increment the angles between values of A. The ROM stores 64 magnitude values of sin A equispaced throughout a quadrant which, of course, also gives 64 magnitude values for cos A. Then the ROM has 64 values for sin B magnitude but since negative values of B can be used, these only have to have a range sufficient to interpolate half-way between the values for A. Sign information is supplied by the accumulator register.

Thus, the real-time calculation of each sample value from reduced sine function information enables a ROM of only 1024 bits to be used. Without this reduction, the technique would not have been economically practical.

Digital Control System

Operation of the carrier digital control system is shown in Fig. 7. Its purpose is to present to the synthesizer a digital word, i.e., the accumulator increment, that corresponds to the carrier frequency required at any instant. In response to the carrier changeover signal, a multiplexer switches the source of this word at a 4.166-Hz rate between the front-panel reference frequency thumbwheel switch and a register containing the measurement frequency.

The measurement-frequency register is incremented or decremented by clock pulses from an algorithmic state machine. When the operator selects CONTINUOUS SWEEP, the register initially is incremented towards the value set on SWEEP LIMIT B, thereafter continuously reversing direction on reaching either A or B (the sweep limits were named A and B rather than upper and lower because it is quite permissible to reverse their roles). Sweep incrementing is synchronized to the carrier changeover so there is no change in carrier frequency during each measurement-frequency period.

In SINGLE SWEEP, the frequency moves toward SWEEP LIMIT B and then stops automatically. Control thereupon reverts to the MANUAL tuner. Rotating the MANUAL tuner knob turns an optically-fringed disk that interrupts a light path, generating up-count or down-count pulses. The absolute position of the knob has no relationship to frequency—it merely acts as a direction-sensitive pulse generator.

Pressing the RESET button loads SWEEP LIMIT A into the register, immediately returning the measurement frequency to A. The STEP-100 Hz button issues a burst of 10 incrementing pulses to the register, achieving an apparently instantaneous jump in frequency. These two buttons are effective only in the manual mode.

Tone Blanking

For tests on systems that may have signalling-tone receivers, the Model 3770A is available with a tone blanking option that prevents the instrument from transmitting in small frequency ranges (one or two) centered about the signalling tone(s). The ranges are factory programmed by jumpers on the printed-circuit board included as part of the option.

The range limits programmed on the card are continuously compared to the carrier frequency word. If the measurement frequency is swept or tuned into this range, the algorithmic state machine issues clock pulses rapidly until the other extremity of the range is reached, giving an apparently instantaneous jump

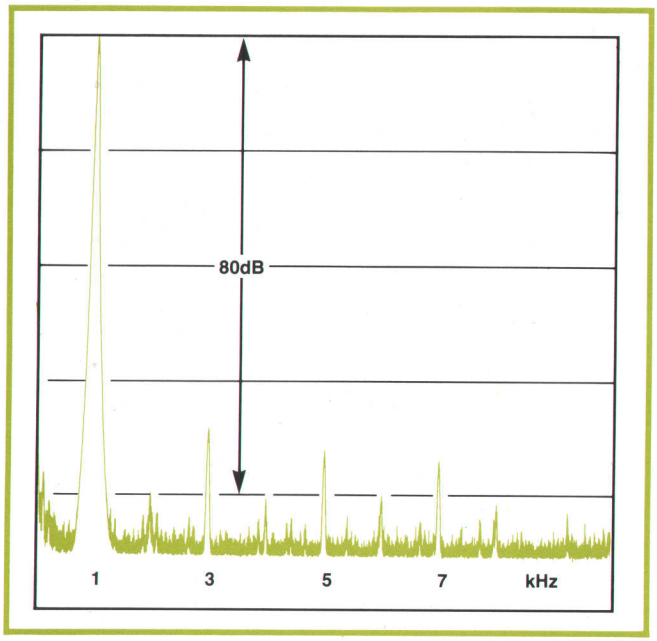


Fig. 6. *Frequency spectrum of the synthesizer output (before modulation) when generating 1 kHz.*

across the range.

The reference frequency is also monitored. If this should be set within a signalling-tone range, the multiplexer is inhibited and the measurement frequency is then sent continuously.

Receiver Overview

A more detailed block diagram of the receiver circuits is shown in Fig. 8. The receiver demodulates the signal and normalizes the envelope amplitude for operation of the group-delay measurement circuits. In a second channel, it measures the average dc level of the demodulated signal for determination of attenuation and absolute level. The 166.6-Hz identifying burst, used to synchronize the measurements, is separated from the demodulated waveform in a third channel. A fourth channel measures the carrier frequency.

After demodulation, the envelope signal undergoes logarithmic conversion. This serves a dual purpose. The dc components of the demodulated signal represent the carrier levels and, when converted logarithmically, they are suitable for expression in dB and dBm. It is merely necessary to measure the two carrier levels digitally and subtract the results to obtain a reading of relative attenuation in dB.

The other purpose is to equalize the peak-to-peak swing of the two envelopes, which simplifies filtering and limiting. Equal peak-to-peak swings occur regardless of the incoming levels of the two carriers because the incremental gain of the log converter is inversely proportional to the dc level.

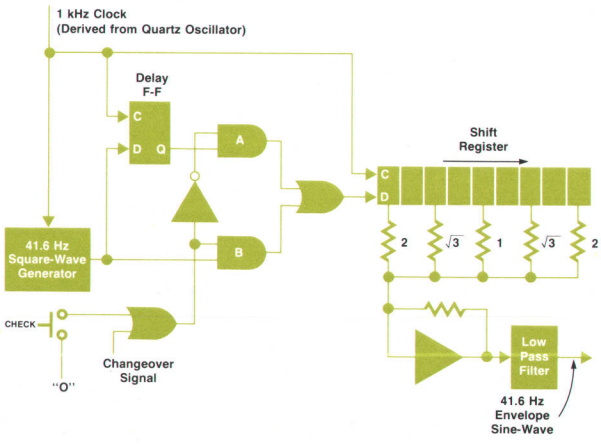
A Group Delay Standard

Although the Model 3770A's direct technique for measuring group delay requires no calibration adjustments, a group delay standard is included in the sender. This is used to give a quick, overall verification of system operation.

When the front-panel CHECK button is pressed, the 41.6-Hz modulation envelope alternates between its normal phase and a phase delayed by precisely 1 ms. Since this gives the carriers a corresponding relative envelope delay, a receiver interprets the signal as though a transmission network with 1-ms relative group delay were being measured. As a further aid, the CHECK button also introduces 3-dB of relative attenuation at the sender output.

A highly accurate means for introducing a phase delay for this test was easily incorporated into the circuits that generate the 41.6-Hz modulation signal. As shown in the diagram, 41.6-Hz squarewave is derived from a 1-kHz clock by digital techniques. The squarewave is filtered by a discrete-delay transversal filter, consisting of a shift register with weighted taps, that removes harmonics up to the 10th. A simple low-pass filter attenuates higher harmonics. This filtering arrangement ensures that the phase of the 41.6-Hz sine wave is maintained in accurate relationship to the carrier changeover, as specified by CCITT. Although of no consequence to the operation of the 3770A receiver, this precise relationship would be required by some other receivers.

The 1-ms phase delay is introduced by a flip-flop clocked by the 1-kHz signal. When the front-panel CHECK button is pressed, the low period of the changeover signal closes gate B and opens gate A, inserting the flip-flop in the signal path. This in effect introduces a 1-ms delay into the 41.6-Hz squarewave, and thus into the modulation envelope. The accuracy of the phase delay is equivalent to that of the master quartz oscillator, higher than that ordinarily obtainable from a delay network, particularly for longer delays (delays up to 10 ms generated this way have shown agreement with 3770A receivers typically to 0.03%). In back-to-back connection of two 3770's, the delay measured by the receiver is typically within 0.1%, some 10 times better than quoted specification.



The converter operates over a 60-dB input range so no range changing is required at the input. The converter does introduce distortion into the envelope but this is of no consequence to the measurements.

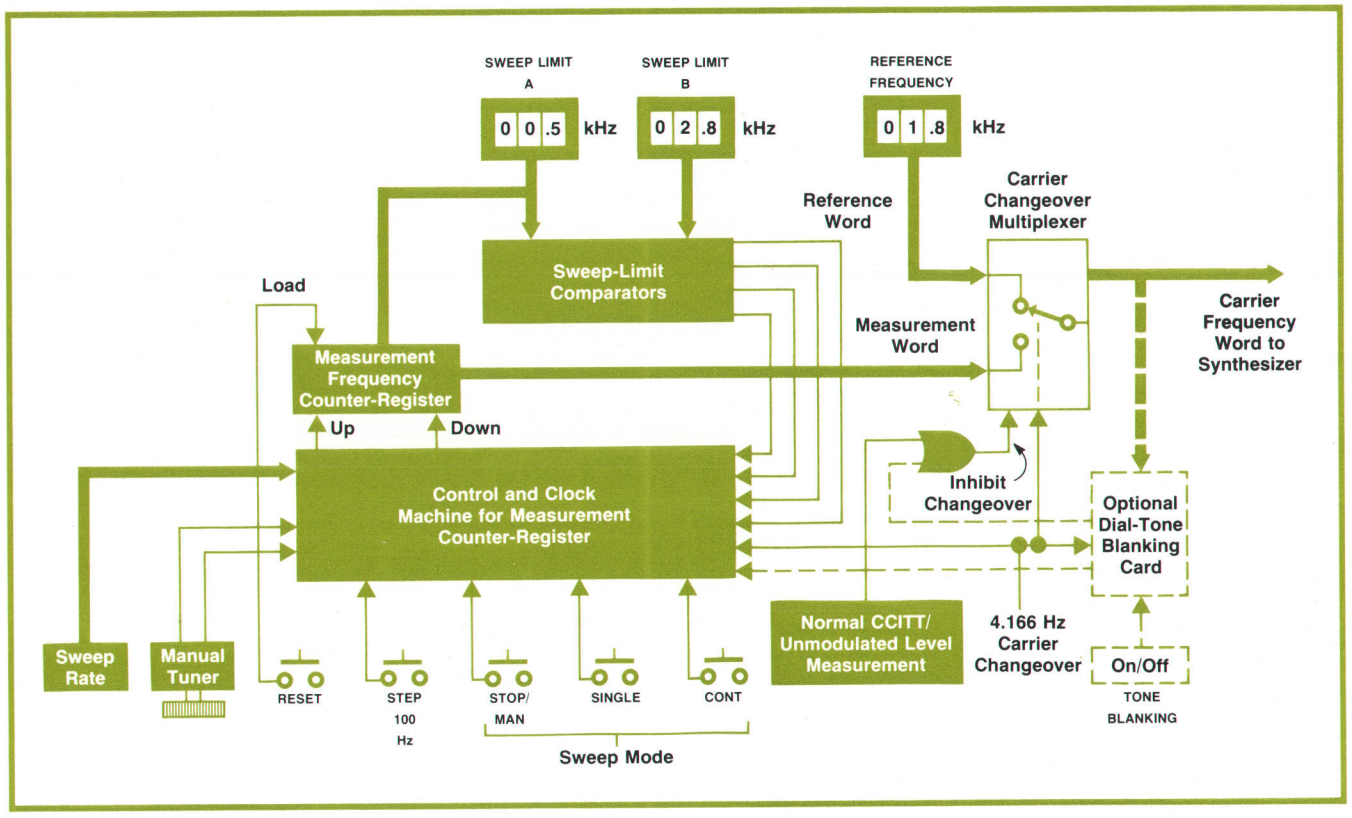


Fig. 7. *Carrier frequency control logic generates a digital word corresponding to the synthesizer output frequency desired.*

Counting Group Delay

Group delay is measured with a bi-directional counter. As shown by waveform "d" in the diagram of Fig. 9, the counter counts up during the interval G_M (t_1) and down during G_R (t_2). The residue in the counter is proportional to group delay.

If the incoming signal is noisy, readings can be averaged by continuing the up-down sequence for 4 or 16 consecutive measurement cycles and dividing the result by appropriate register shifts.

To obtain a clean waveform for accurate group delay measurements, a narrowband 41.6-Hz filter is needed, but the time required for a narrowband filter to settle down after a shift in envelope phase could introduce errors. The use of a blanked filter solves the settling problem. About 40 ms prior to a measurement window, the blanking logic is enabled. It unblanks the filter on the next waveform zero crossing (waveform 9c). The envelope signal then develops from this zero crossing without the transients that otherwise would occur. It is blanked again when the timing window has passed. A narrower filter than otherwise would be possible may thus be used.

Counting Attenuation

Attenuation measurements are made by the dual-slope technique commonly used in digital voltmeters.[4] As shown by waveform 9e, an integrator charges at a rate proportional to the measurement carrier level for the duration of the 24-ms acceptance window (by making the integrator charging interval exactly 24 ms, the 41.6-Hz envelope is averaged out of the measurement). The counts accumulated while the integrator subsequently discharges to zero under control of a fixed reference voltage (period A_M in waveform "e" of Fig. 9) becomes an indicator of the measurement carrier level (Fig. 9f). This is compared to the reference carrier level by counting down for the reference carrier measurement (A_R). In the case shown in Fig. 9, the reference carrier level is less than the measurement carrier so the count reverses when it arrives at zero and the negative sign is set.

For absolute level measurements of either carrier, a fixed reference corresponding to 0 dBm is substituted for the carrier level not being measured.

Since attenuation, absolute level, and group delay measurements use similar counting techniques, the same up-down counter and control logic are used for all three. Attenuation and absolute level measurements, as well as group delay measurements, may be averaged.

Measurement results are presented digitally in the right-hand part of the display, a front-panel switch selecting attenuation, level, or group delay for display. Measurement results are also applied to a digital-to-analog converter for use by an X-Y recorder.

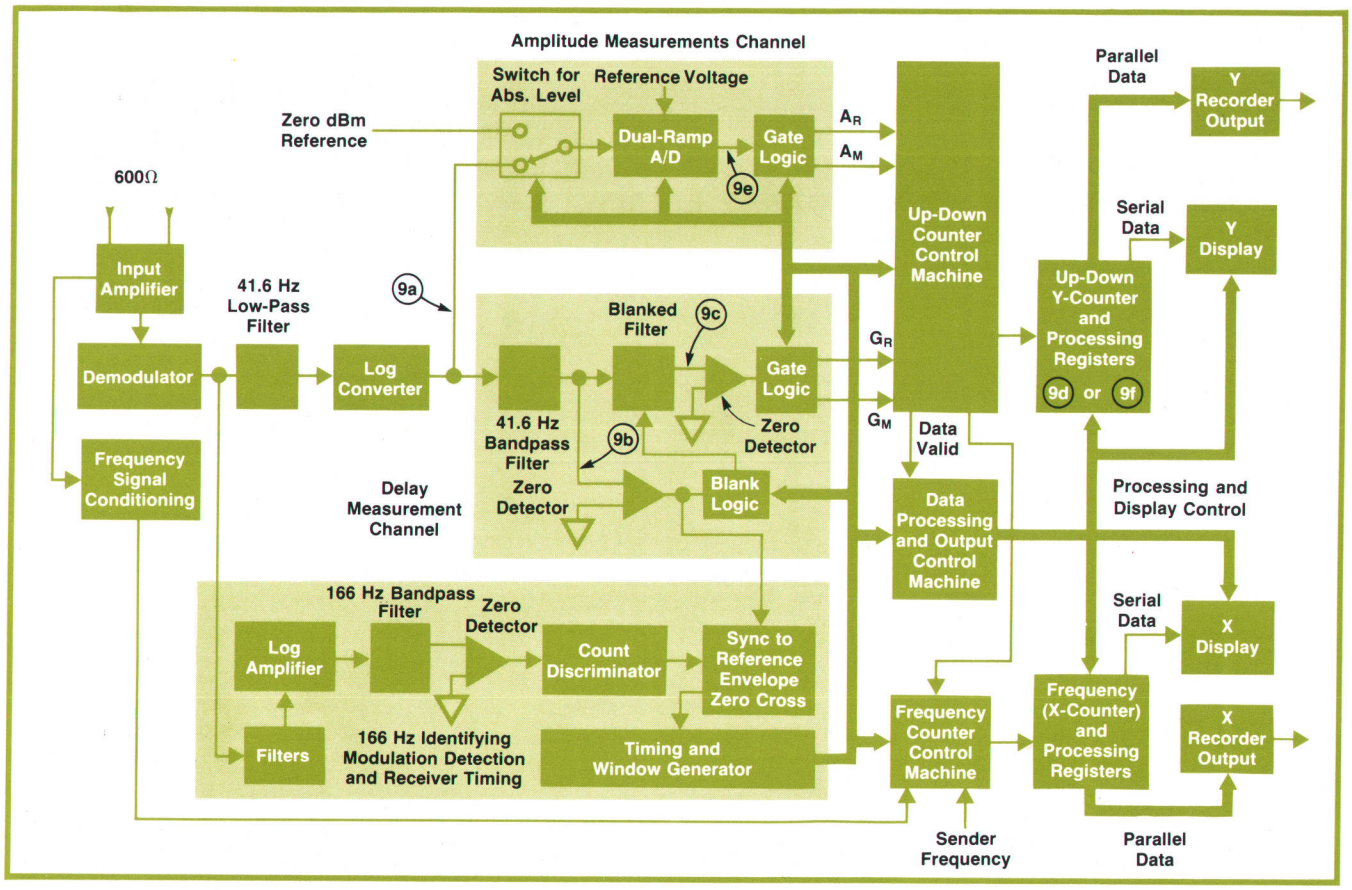


Fig. 8. *Block diagram of receiver. Circled numbers refer to the waveforms in Fig. 9.*

Frequency Measurement

The frequency conditioning circuit enables the carrier frequency to be measured over the full input amplitude range of the instrument (−50 to +10 dBm) without operator attention and with good noise immunity. It uses a non-linear amplifier that gives high gain for low-level signals and a gain of about one for high-level signals. A self-biasing comparator triggers on the positive peak of the signal and another triggers on the negative peak. These alternately set and reset a flip-flop to generate a square wave at the same frequency as the input.

The 100-ms counter gating interval is synchronized to a zero crossing of the measured signal. This removes a ±1 count ambiguity, equivalent to ±10 Hz, which would occur if the gating period and the signal were uncorrelated. As a further refinement, both positive and negative waveform transitions are counted and an additional count is then added before dividing by 2 with a one-place shift. This has the effect of rounding the answer *up* or *down*, depending on which 10-Hz step is nearest. The instrument thus has a basic ±5-Hz accuracy in frequency measurements.

The results of a frequency measurement are presented digitally in the left-hand part of the display and are applied to a D-to-A converter for an X-Y recorder. A front-panel switch selects the receiver or the sender frequency (reference or measurement) for display.

Efficient Packaging

Complex as this instrument may seem to be internally, servicing is simplified by the use of plug-in circuit boards to provide quick access to component assemblies. The front panel tilts down to give access to front-panel components, otherwise often difficult to reach, without need for electrical disconnections (Fig.10).

The instrument is housed within a compact, easy-to-carry cabinet. A major contributor to the instrument's compactness is the highly efficient switching-regulated power supply that sharply reduces the size and weight of the power transformer. Though obtaining an efficiency of 75%, this power supply has a dc regulation better than 0.01% at a full 40W load with wide ±20% variations in line voltage.

Acknowledgments

Many innovative contributions from a spirited design team led the 3770A project to a satisfying conclusion. The best ideas often resulted from the persistence and interaction of several team members but

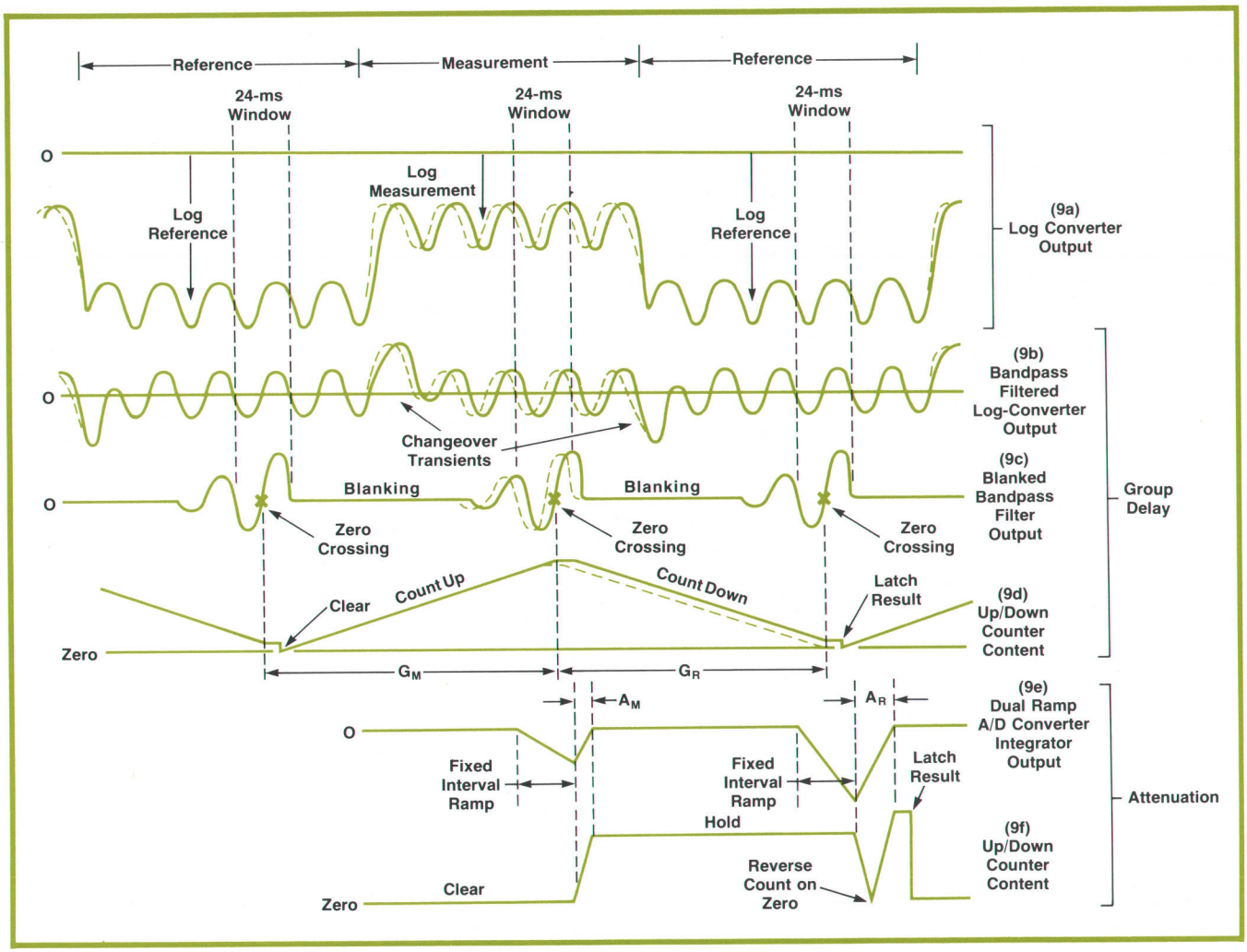


Fig. 9. *Waveforms illustrate processing of the signal to determine group delay and attenuation.*

particular mention must be made of Ralph Hodgson whose particularly thorough, systematic and painstaking approach to the complex measurement logic

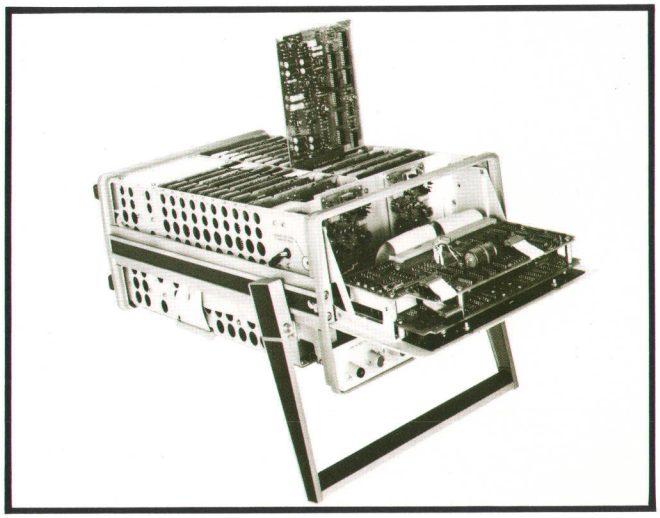
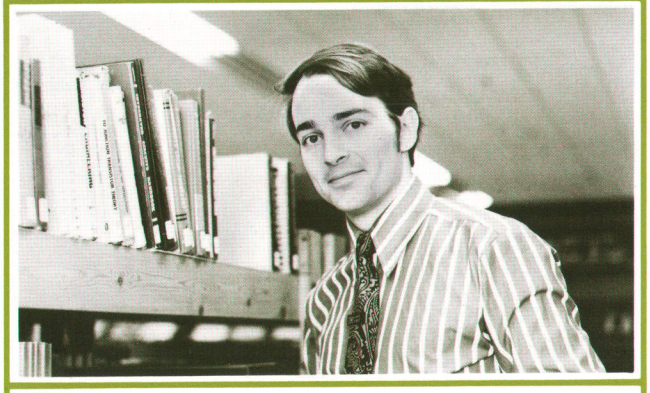


Fig. 10. *Circuits are readily accessible for service.*



David H. Guest

David Guest's early interest in amateur radio eventually led to a B.Sc. degree at Heriot-Watt University. On graduating in 1970, he joined Hewlett-Packard, working initially on some investigative products and working part-time on an M.Sc. degree. He subsequently contributed to the 3761A Bit Error Detector then joined the 3770A project, becoming project leader in 1973. Davids' spare time activities are pure relaxation—enjoying the wildlife and open spaces of his native Scotland.

ABRIDGED SPECIFICATIONS

Hp Model 3770A Amplitude/Delay Distortion Analyzer

(Complete specifications available on request)

Sender

REFERENCE CARRIER
FREQUENCY RANGE: 0.4 to 19.9kHz in 100Hz steps
FREQUENCY ACCURACY: ±0.1%
MEASURING CARRIER
FREQUENCY RANGE: 0.20 to 20.00kHz in 10Hz steps
FREQUENCY ACCURACY: ±0.1%
MODULATION
ENVELOPE FREQUENCY: 41.66Hz, ±0.1%
Modulation Index: 0.40, ±0.05
IDENTIFICATION-BURST-FREQUENCY: 166.6Hz, locked to envelope frequency
Modulation Index: 0.20, ±0.05
CARRIER CHANGEOVER FREQUENCY: 4.166Hz, locked to envelope frequency. The changeover maintains both envelope and carrier phase continuity. Deviation between changeover point and envelope minimum: <0.2ms.
SWEEP
MEASURING FREQUENCY SWEEP RATES: 10, 20, 40, 80, 160Hz/s nominal. Frequency is maintained constant during measurement frequency transmission interval.
SWEEP LIMITS: Panel presettable in the range 0.2 to 19.9kHz, in 100 Hz steps.
SENDER GROUP DELAY ERROR: 0.2 to 0.4kHz <5μs
0.4 to 0.6kHz <2μs
0.6 to 20kHz <1μs
OUTPUT
IMPEDANCE: 600Ω balanced
RETURN LOSS: >40dB
DEGREE OF BALANCE: >50dB
CARRIER LEVEL: 0 to −49dBm in 1dB steps
CARRIER HARMONIC DISTORTION: <1% (40dB) total
CARRIER SPURIOUS DISTORTION: <0.03% (70dB) per 100Hz bandwidth
SPURIOUS SIDEBAND POWER RELATIVE TO WANTED SIDEBAND POWER (Modulation distortion factor): <1% (40dB)

Receiver

INPUT
OPERATING LEVEL RANGE: <−50dBm to >+10dBm
IMPEDANCE: 600Ω, balanced
RETURN LOSS: >40dB
DEGREE OF BALANCE: 200Hz to 6kHz: >60dB; 200Hz to 20kHz: >50dB

GROUP DELAY ERROR
DELAY ACCURACY (rms) (5 to 40°C):
0.2 to 0.4kHz: <10μs ±1% of reading
0.4 to 0.6kHz: <6μs ±1% of reading
0.6 to 20kHz: <4μs ±1% of reading
For 0 to 50°C, ±1% of reading becomes ±2% of reading.
ADDITIONAL DELAY ERRORS: (See "Combined Sender/Receiver Specification").
FREQUENCY
When used with any sender other than an HP 3770A, frequency measurement accuracy is: 0.1% ±5Hz.
RECORDER
X-AXIS OUTPUT: 0 to +5V corresponds to 0 to 20kHz or 0 to 5kHz.
Y-AXIS: ±5V corresponds to ±FS of recorder range selected. There is only one range in LEVEL, where +1 to −5V corresponds to +10 to −50dBm.
RECORDER OUTPUT ACCURACY: As display, ±1% of range selected.

Combined Sender/Receiver

FREQUENCY
RANGE: 0.2 to 20kHz in 10Hz steps
ACCURACY: 0.1% (send and receive)
GROUP DELAY DISTORTION
DELAY RANGE: 0 to ±10ms
DELAY ACCURACY (rms) (5 to 40°C):
0.2 to 0.4kHz: <15μs ±1% of reading
0.4 to 0.6kHz: <8μs ±1% of reading
0.6 to 20kHz: <5μs ±1% of reading
For 0 to 50°C ±1% becomes ±2% of reading.
ADDITIONAL DELAY ERRORS: Further delay errors are allowed at below −40dBm, with large attenuation distortion, and with interfering noise and tones.
ATTENUATION DISTORTION

Receive level range within which both Measurement and Reference carrier levels are contained	Receiver Maximum Error of Attenuation in the range 0 to ±40dB		Sender Max Error
	5 to 40°C	0 to 50°C	
+5 to −5dBm	0.15dB ±1%	0.15dB ±1%	0.1dB
+5 to −20dBm	0.15dB ±1%	0.15dB ±1.5%	0.1dB
+10 to −30dBm	0.2dB ±1%	0.2dB ±2%	0.1dB
+10 to −40dBm	0.2dB ±1.5%	0.3dB ±2.5%	0.1dB
+10 to −50dBm	0.6dB ±2.5%	0.7dB ±3%	0.1dB

LEVEL MEASUREMENT (absolute) without changeover and unmodulated:
Rear panel Function Switch of both Send and Receive instruments (if different) must be in "Unmodulated Level Measurement" position.
RECEIVE RANGE: +10 to −50dBm
ACCURACY:

	5 to 40°C		0 to 50°C	
	Sender	Receiver	Sender	Receiver
+10 to −20dBm:	±0.2dB	±0.2dB	±0.3dB	±0.3dB
−20 to −30dBm:	±0.2dB	±0.4dB	±0.3dB	±0.5dB
−30 to −40dBm:	±0.3dB	±0.7dB	±0.4dB	±0.8dB
−40 to −50dBm:	±0.5dB	±1.2dB	±0.5dB	±1.6dB

LEVEL MEASUREMENT (absolute) with changeover
Either the Measurement or Reference received levels may be measured. Send levels are as above.

Options

OUTPUT LEVEL (OPTION 001): Send level range extended to −49 to +10dBm.
LOOP HOLDING (OPTION 002): Loop holding is provided for both sender output and receiver input.
MAXIMUM DC LOOP HOLDING CURRENT: 100mA
VOLTAGE DROP AT MAX. CURRENT: Approximately 12V
DYNAMIC OUTPUT IMPEDANCE: Approximately 50kΩ
TONE BLANKING
RANGE: Up to two bands in the range 0.2 to 9.9kHz
RANGE LIMITS: Any multiple of 100Hz

General

DIMENSIONS: 560×200×290mm (22×7.8×11.3in)
WEIGHT: 12kg (26.5lbs)
OPERATING TEMPERATURE RANGE: 0 to 50°C unless otherwise specified.
POWER: 90 to 126Vac or 195 to 253Vac (45 to 65Hz), 50W
PRICE IN U.S.A.: Model 3770A, $6500.
MANUFACTURING DIVISION: HEWLETT-PACKARD LIMITED
South Queensferry
West Lothian, Scotland

and analog circuits resulted in a much finer product, of Peter Rigby for ideas and much of the design of the delay and frequency measuring circuits, of Aileen Appleyard for her persistence in the design of the identification detection and timing circuits midst ever-changing requirements, of Mike Ramsay for development of the sender control logic, of Rajni Patel for painstaking development of the efficient switching-regulated power supply, of David Leahy who initiated the mechanical design and Tony Cowlin whose design details added refinement to the concept, of Stuart Ross who ably guided the instrument into production, and of Mario Pazzini, who provided broad technical experience as project leader during the earlier design phase before returning to his native Italy.

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HEWLETT-PACKARD JOURNAL

NOVEMBER 1974 Volume 26 • Number 3

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