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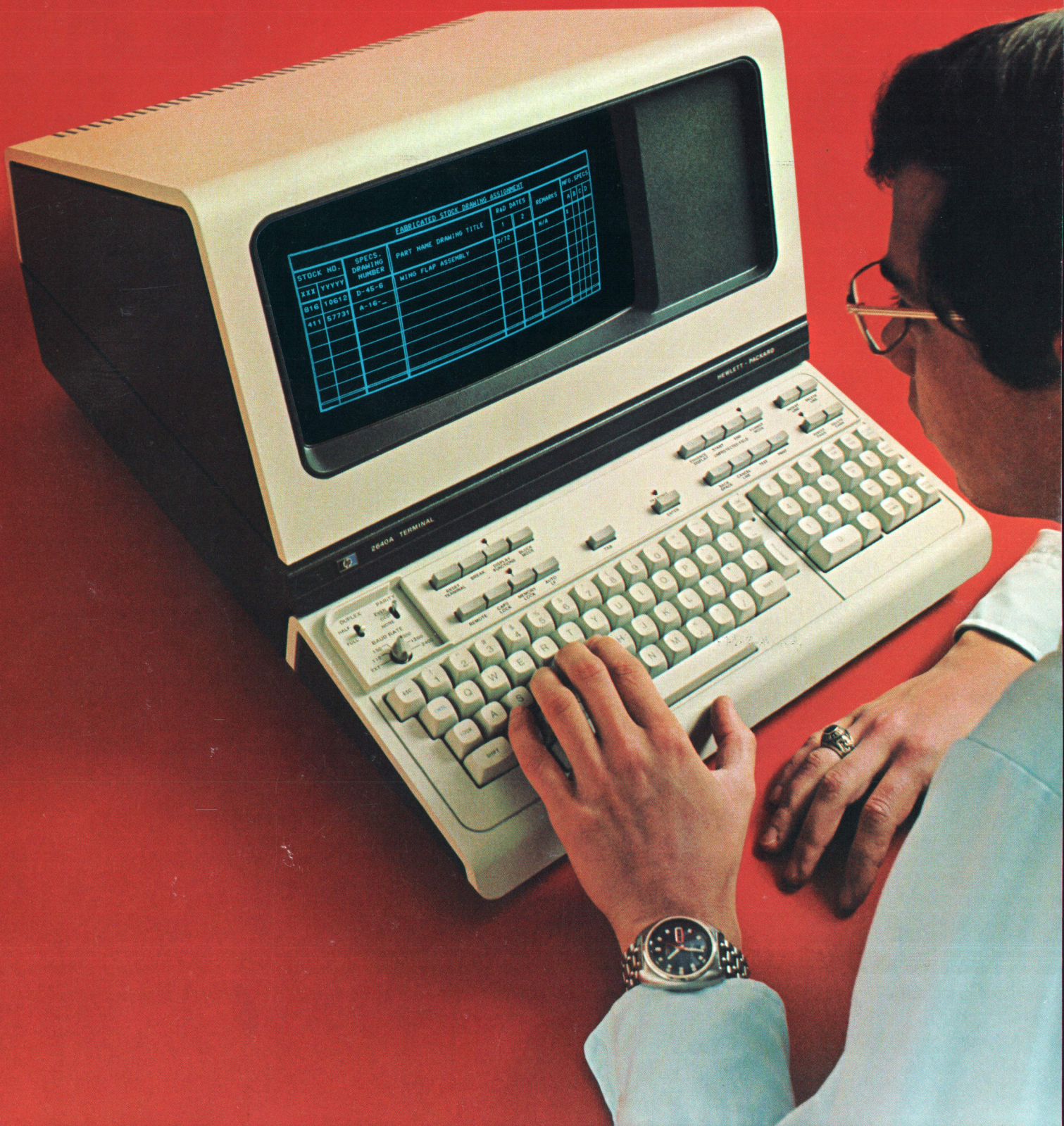

Cost-Effective, Reliable CRT Terminal Is First of a Family

Microprocessor control and modular design result in a computer terminal that is powerful and flexible, yet low in cost. Jim Doub, engineering section manager, discusses the family concept and the philosophy behind the design.

by James A. Doub

ALTHOUGH HEWLETT-PACKARD has been in the minicomputer and computer systems business for almost ten years, the Model 2640A Interactive Display Terminal (Fig. 1) is its first HP-manufactured terminal. Before the 2640A, Hewlett-Packard had relied upon other manufacturers for this key component in its terminal-based systems.

HP's terminal needs called for a wide range of capability at the lowest possible cost. The flexibility that comes from physical and functional modularity and from microprocessor-based organization was mandatory to allow the terminal to adapt to new applications, changing user requirements, and new technologies. To meet these requirements, a family of terminals was conceived. The 2640A is the first member of this family.

2640A Features

An easy-to-read display generates characters using a high-resolution dot matrix. The display has a capacity of twenty-four 80-character lines. Besides the standard Roman font, mathematics and line-drawing character sets, including subscripts, superscripts, and Greek characters are available. Additional character sets such as Japanese Katakana are planned. Inverse video (black on white), blinking, half-bright, and underlining in all combinations are possible. Control codes for character sets, display enhancements, and protected fields do not occupy positions

Fig. 1. *Model 2640A Interactive Display Terminal operates in either character or page mode. Data transmission is compatible with EIA RS 232C and with Bell type 103 and 202 modems. Data rates from 110 to 2400 baud are selectable. Character code for data transmission is ASCII.*

Cover: *Model 2640A Interactive display terminal uses its optional line-drawing character set to display a form to be filled in by the operator. Microprocessor control gives this new terminal a high degree of flexibility at a relatively low cost.*

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on the screen and are transparent to the user.

The dynamically allocated memory is designed for efficient storage. Spaces to the right of the end of a line are not stored in memory. Lines that have rolled off the screen remain in memory and are available to the user via roll and page keys. Over 400 lines can be stored in the terminal. Memory is expandable to 8192 characters in 2K or 4K blocks. All memory allocation is automatic and transparent to the user.

Full off-line editing capability allows the user to verify and correct data before transmission to the computer. The terminal transmits one character, a line, or a page of characters at a time. Data transmission is RS-232C compatible, full or half duplex. Connection with the computer can be hardwired or by Bell type 103 or 202 modems.

Easy to expand, Model 2640A is equipped with seven powered slots for options, memory, or peripheral interfaces. An HP Model 9866A Line Printer is available as a terminal option. Hard copy is printed at 240 lines per minute.

The self-test feature makes it possible for an untrained operator to determine whether a service call is required. If a failure occurs during the self-test, the test yields information to allow a service person to isolate the defective module without additional diagnostics or special test instruments. The defective module can be quickly replaced without tools.

Design Overview

The 2640A is shown in block diagram form in Fig. 2. The product has three major and mechanically independent sections: keyboard, CRT monitor, and mainframe. The heart of the system is the mainframe, which can be considered a microcomputer system. In the mainframe is the power supply and a bus-oriented logic system containing the microprocessor, program and data memory, video display subsystem, keyboard interface, and data communications interface. The basic system contains slots for two options, and an optional extender adds five more slots. All mainframe modules are functionally, mechanically, and electrically independent, giving a high degree of flexibility and reducing manufacturing and service time.

The CRT monitor section contains sweep and high voltage circuits, the high-resolution, low-profile cathode-ray tube, and the fan when the mainframe

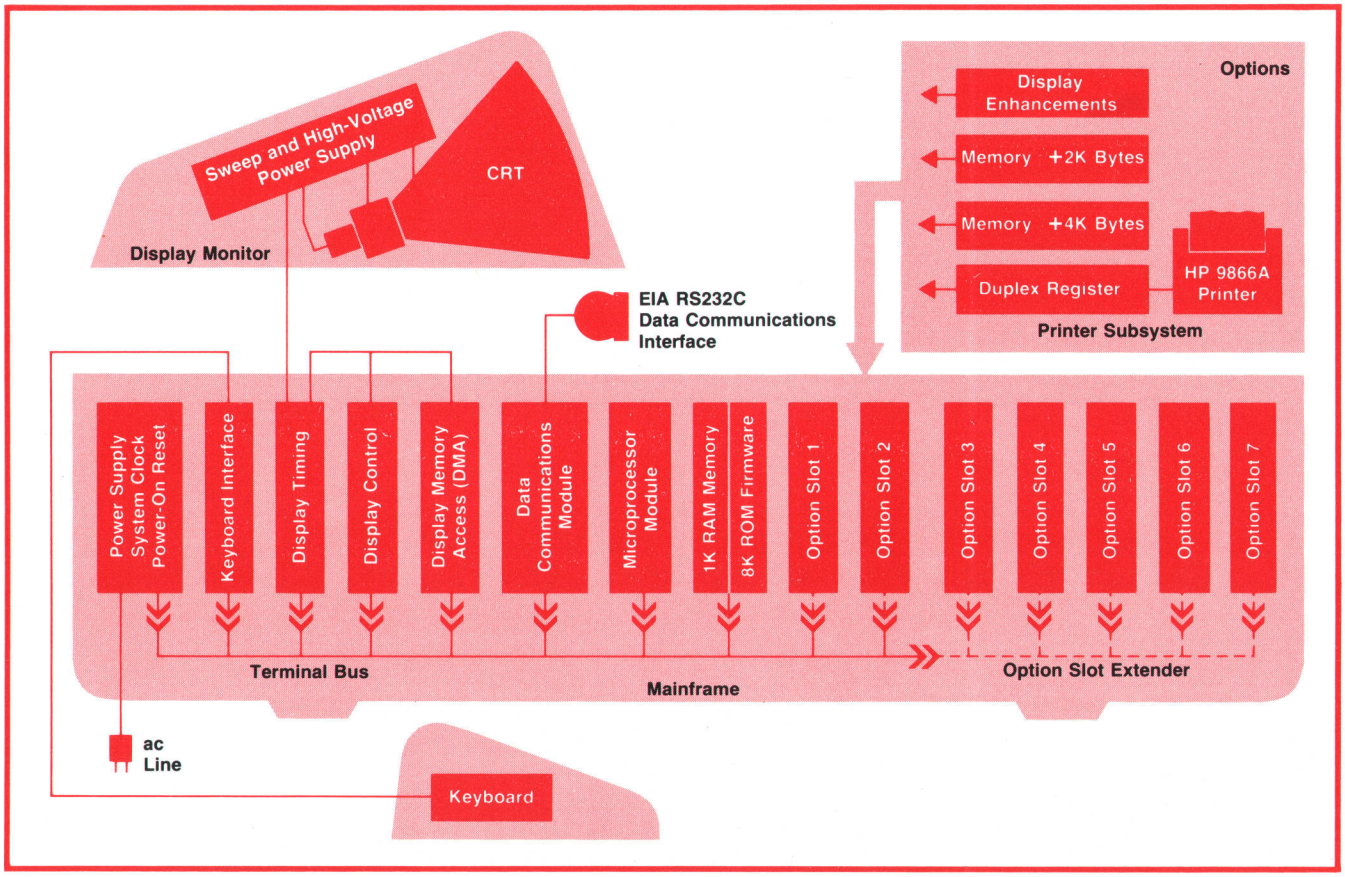


Fig. 2. *CRT monitor, mainframe, and keyboard form three mechanically independent sections. Mainframe contains slots for standard and optional modules. Any module, including the power supply, can be replaced quickly without tools.*

option slot extender is included.

The keyboard section comes in two versions depending on the application, a general-purpose version and a simplified one with fewer keys for less sophisticated uses.

The specific functional properties of the terminal are determined by firmware programs resident in ROM (read-only-memory). It is these programs, occupying 8K bytes of ROM, that make it possible for the terminal to have many powerful features such as self-test, dynamic memory allocation, transparent control codes, and off-screen storage.

The articles that follow describe the important design contributions of the 2640A. Common to all of these designs is an effort to guarantee product quality. Here is the story behind designing quality into the 2640A.

Product Quality

All users want "inexpensive quality". All design engineers want to include this property in their designs. All too often, however, this desire is not realized. To ensure that inexpensive quality became a reality in the HP 2640A, this concept had to be converted into a tangible concept that could be dealt with in the design. We decided to measure it by the annual cost of maintenance expressed as a percent of the selling price. Inexpensive quality, then, meant designing for a low maintenance cost with little or no increase in the selling price. This produced a double benefit, since a product that is easy to maintain is also easy and less costly to manufacture.

Annual maintenance cost is the sum of hardware failure rate times the cost of repairs, operator error rate times the cost of operator errors, and miscellaneous costs. Designing in quality simply meant establishing specific design goals and practices aimed at reducing each component of the maintenance cost.

At the outset, a hardware failure rate goal of less than one failure per operating year was established as the minimum acceptable limit. An operating year, defined in terms of the average application of the product, was taken to include 3640 hours of power-on operation and 260 power on/off cycles. This corresponds to 14-hour days, five days per week, 52 weeks per year, with power turned on and off each day.

In addition to the normal HP Class B environmental testing, a major reliability program was established to predict and verify compliance with the failure rate goal. The predicted failure rate based upon the design was 7000 hours mean time between failures (MTBF). Actual measured MTBF, based upon over 175,000 unit-hours of field operation, is in excess of 4100 hours.

How were these results achieved in the design?

Designing for Quality

All designers submitted their modules to a design review by a group of peers at each prototype phase. This practice was aimed at disseminating design understanding throughout the team, justifying costs versus benefits, justifying component selection, detecting gross errors in design, and most important,

The HP 2640A At Work as a Data Entry Terminal

The HP 2640A CRT terminal is now being integrated into Hewlett-Packard's internal data entry and data communications system called COMSYS. A worldwide distributed network of minicomputer systems, COMSYS uses dial-up telephone lines to link 76 HP locations for the transfer of data. Currently over 150 CRT terminals of various types are being used to enter approximately three million characters of data per day. Total COMSYS traffic averages 40 million characters of data per day with peaks of over 100 million characters per day. The 2640A is being used as an operator-to-program interface with its primary COMSYS use being for data entry.

Sales orders, shipping papers, payroll information, statistics and general messages are only a few of the kinds of data being entered into COMSYS via 2640A terminals. Each data entry transaction may require several forms or formats to be displayed sequentially on the CRT screen. As each format is displayed, the operator transposes coded data from a source document into special data fields on the screen. Each data field is appropriately titled and delimited by brackets. The operator uses a TAB key to skip from data field to data field. A convenient data entry feature of the 2640A is a "beep" that occurs when a data field is filled by the operator and the cursor skips automatically to the next field. This allows the operator to hear his or her place on the screen and not have to look up from the source document.

When the operator presses the ENTER key on the 2640A, the computer reads the data typed into the format, checks for typing or coding errors and displays the next format. If any errors are detected by the computer, the fields in error are underlined and blinked. Each error must be corrected before the operator can continue with that transaction. Error correction at the point and time of original entry has greatly reduced error rates and time delays and hence order processing costs.

Each 2640A is operated in a page or forms display mode and currently interfaces to an HP 2100A Computer through a separate interface card. COMSYS supports a maximum of four 2640A's per system with capabilities for up to 16 per system planned for 1976. By parallel I/O, the computer can simultaneously display formats or read data on all four 2640A's. This reduces the wait time of any one operator to almost nothing. Each terminal operates independently of the other terminals and can be used to enter any type of transaction that has been programmed. In addition, the computer is multiprogrammed to allow other tasks such as printing or transmission to occur simultaneously with data entry.

Combining HP computers and CRT terminals is proving to be the fastest, least expensive and most reliable way to accomplish data entry. Response to the 2640A has been such that an all-2640A data entry system is almost certainly in Hewlett-Packard's future.

Terry Eastham
COMSYS Systems Analyst

SPECIFICATIONS
HP Model 2640A Interactive Display Terminal

Features

ENHANCED HIGH-RESOLUTION DISPLAY
PLUG-IN CHARACTER SETS
DYNAMICALLY ALLOCATED MEMORY
POP-IN MODULARITY AND EXPANDABILITY
MICROPROCESSOR CONTROLLED
CHARACTER/BLOCK MODE
SELF-TEST
FULL EDITING CAPABILITY
MULTI-TASK KEYBOARD
OFF-SCREEN STORAGE WITH SCROLLING CAPABILITY
PROGRAMMABLE PROTECTED FIELDS
INVERSE VIDEO FOR HIGHLIGHTING. OPTIONAL BLINKING, UNDERLINE, HALF-BRIGHT
CURSOR ADDRESSABILITY AND POSITIONING CONTROL. TABULATION
MOS CIRCUITRY, ROM/RAM
HARD-COPY INTERFACE
SINGLE BUS ARCHITECTURE

General

SCREEN SIZE: 5 inches (127 mm) × 10 inches (254 mm)
SCREEN CAPACITY: 24 lines × 80 columns (1,920 characters)
CHARACTER GENERATION: 7 × 9 enhanced dot matrix; 9 × 15 dot character cell; non-interlaced raster scan
CHARACTER SIZE: .097 inches (2.46 mm) × .125 inches (3.175 mm)
CHARACTER SET: 64 upper-case Roman
CURSOR: blinking-underline
DISPLAY MODES: white on black; black on white (inverse video)
REFRESH RATE: 60 Hz (50 Hz optional)
TUBE PHOSPHOR: P4
IMPLOSION PROTECTION: bonded implosion panel
MEMORY: MOS; ROM: 8K bytes (program); RAM: std. 1024 bytes; 8192 bytes max
KEYBOARD: full ASCII code keyboard, 8 special function keys, and 12 additional control and editing keys; ten-key numeric pad; cursor pad; multi-speed auto-repeat; n-key roll-over; stand-alone, 4-foot cable.

Data Communications

DATA RATE: 110, 150, 300, 1200, 2400 baud, and external—switch selectable (110 selects two stop bits)
COMMUNICATIONS INTERFACE: EIA standard RS232C; 103 and 202 modem compatible
TRANSMISSION MODES: full or half duplex, asynchronous
OPERATING MODES: on-line; off-line; character, block
PARITY: Switch selectable; even, odd, none

Power Requirements

INPUT VOLTAGE: 115 (+10%, −23%) at 60 Hz (50 Hz optional)
230 (+10%, −23%) at 60 Hz (50 Hz optional)
POWER CONSUMPTION: 75W

Environmental Conditions

TEMPERATURE, FREE SPACE AMBIENT:
NON-OPERATING: −40 to +75°C (−40 to +167°F)
OPERATING: 0 to +55°C (+32 to +131°F)
HUMIDITY: 5 to 95% (non-condensing)
HEAT DISSIPATION: 426 BTU/hour
ALTITUDE:
NON-OPERATING: sea level to 25,000 feet (7620 meters)
OPERATING: sea level to 15,000 feet (4572 meters)
VIBRATION AND SHOCK:
VIBRATION: 30 mm (0.012") pp, 10 to 55 Hz, 3 axes
SHOCK: 30G, 11 ms, 1/2 sine
Type tested to qualify for normal shipping and handling

Physical Specifications

DISPLAY MONITOR WEIGHT: 37 pounds (16.8 kg)
KEYBOARD WEIGHT: 7 pounds (3.2 kg)
DISPLAY MONITOR DIMENSIONS: 17.5 in W × 18 in D × 13.5 in H (444.5 mm W × 457.2 mm D × 342.9 mm H) (25.5 in D (647.7 mm D) including keyboard)
KEYBOARD DIMENSIONS: 17.5 in W × 8.5 in D × 3.5 in H (444.5 mm W × 215.9 mm D × 88.9 mm H)
PRICES IN U.S.A.:
2640A CRT Terminal, $3000.
Option 001 128-Character Set, $100.
Option 005 Modem Cable, $50.
Option 006 RS 232C Cable, $50.
Option 010 Simplified Keyboard, −$100.
Option 012 9866A Printer Subsystem, $3295.
Option 015 50 Hz, N/C.
13231A Display Enhancement Board, $250.
Option 201 Math Symbol Set, $100.
Option 202 Line Drawing Set, $100.
13233A +2K Memory Module, $250.
13234A +4K Memory Module, $375.
13240A Option Slot Extender, $150.
MANUFACTURING DIVISION: DATA SYSTEMS DIVISION
11000 Wolfe Road
Cupertino, California 95014 U.S.A.

encouraging the designer to have an exhaustive understanding of his design.

All components used in the 2640A ultimately were reliability qualified. Component types and values were consolidated by almost 50% to reduce the number of potential component-related reliability problems and reduce the materials handling costs both in the factory and the field. In some cases more expensive components were used if they reduced the total product cost (selling price plus maintenance cost). The contactless magnetic keyswitch used on the keyboard is an example.

The cost of operator errors is reduced by localizing and solving these problems at the user's site by the operator. The built-in self-test feature tells the user quickly whether the hardware is the offending element. An easy-to-read manual aids the user in resolving any application issues.

Repair costs break down into several components: problem verification, fault isolation, fault repair, and performance re-verification. The majority of 2640A problems can be quickly verified and isolated to the modular level simply by using the self-test feature. More exotic problems are diagnosed using the microdiagnostic supplied with the service kit. Repair in the field is done rapidly to the modular level and is aided by the no-tools pop-in/pop-out packaging system. Performance verification is again quickly done using self-test. Repair of modules is done quickly and economically on computer-based automatic test systems at the repair depots.

Acknowledgments

The performance of the 2640A is the direct result of the outstanding team of designers we were fortunate to have on the program. Key contributors who served the team in general were: Bob O'Keefe, who managed the project logistics and documentation; John DiVittorio, who managed to get all of our modules integrated into our in-house computer-based component-level test systems; Lee Wiese, our project technician who is now our lead production test technician; and George Crow, who designed our outstanding power supply. Special credit is due Bill Toney, production engineering manager, and Tom Anderson, product marketing manager, for their contribution to the definition and producibility of the 2640A. In addition to those acknowledged in the articles that follow, special note is due Rick Lyman, who did much of the system design and is now at Stanford University pursuing an MBA degree, Ole Eskedal, who did the initial memory and system bus design, and Karl Helness, who did the early keyboard design. Ole and Karl have now returned to their native Scandanavia.

James A. Doub

Jim Doub is section manager for CRT terminal products at HP's Data Systems Division. With HP since 1965, he's served as a design engineer and project manager for nuclear analyzers, product and project manager for the 5407A Scintigraphic Data Analyzer, and laboratory manager for digital signal analyzers. He assumed his present position in 1972. Jim earned his BSEE degree at the University of California at Berkeley in 1963 and his MSEE degree at Rutgers University in 1965. Born in Glendale, California, he's married, has two sons, and now lives in Sunnyvale, California. He spends much of his spare time with his family—camping, skiing, sailing, participating in the Indian Guides program, and serving as a Sunday School superintendent. His principal hobby is woodworking "for fun and profit."

A Functionally Modular Logic System for a CRT Terminal

by Arthur B. Lane

CONTROLLING THE FUNCTIONS of the 2640A CRT Terminal is an internal microcomputer system. This system does almost everything in the terminal except generate the character dot patterns and drive the CRT. The basic elements of the system are a single chip microcomputer (often called a microprocessor) and a terminal bus.

The logic system design objectives of flexibility, adaptability, and cost effectiveness led to a modular microprocessor-controlled approach (Fig. 1). The major subsystems of the terminal were partitioned into individual printed circuit cards, all of which plug into the terminal bus. This provides many benefits, such as ease of maintenance and convenient addition of options. Also, since the 2640A is the first in a family of terminals, modules can be common to several products, thereby easing manufacturing and service. A major benefit to the designer and ultimately to the user is the ease of upgrading individual modules or adding new ones when new technology makes cost or performance improvements possible.

The benefits of microprocessor control are, for the user, advanced features at low cost, and for the factory, flexibility as a result of the ease of reprogramming. For these reasons, microprocessor control was selected over hardware wherever possible. The bus and logic modules were designed to be processor-independent so other microprocessors could be added later without major system redesign.

Terminal Bus

A major element of the logic system is the terminal bus, a printed circuit board with connectors, which is attached to the bottom of the terminal mainframe and to the power supply. The terminal bus distributes power to the individual modules and provides data,

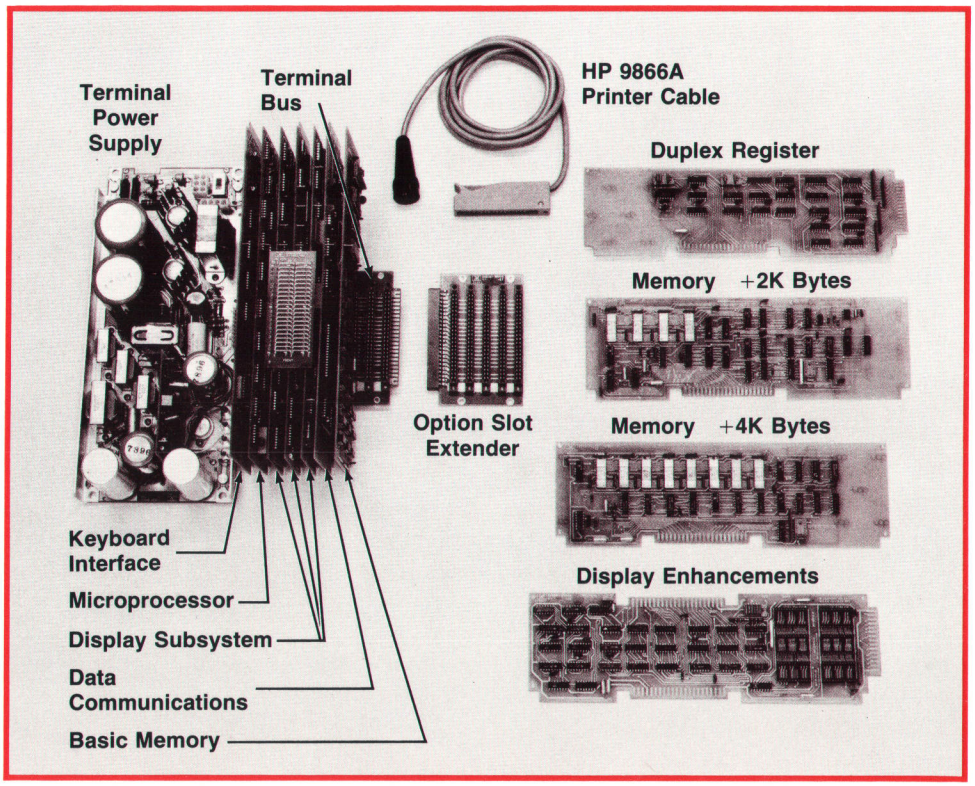


Fig. 1. *Terminal bus is the backbone of the modular 2640A logic system. The bus has seven slots for the basic terminal printed circuit modules, and two for options. An optional bus extender adds five more slots.*

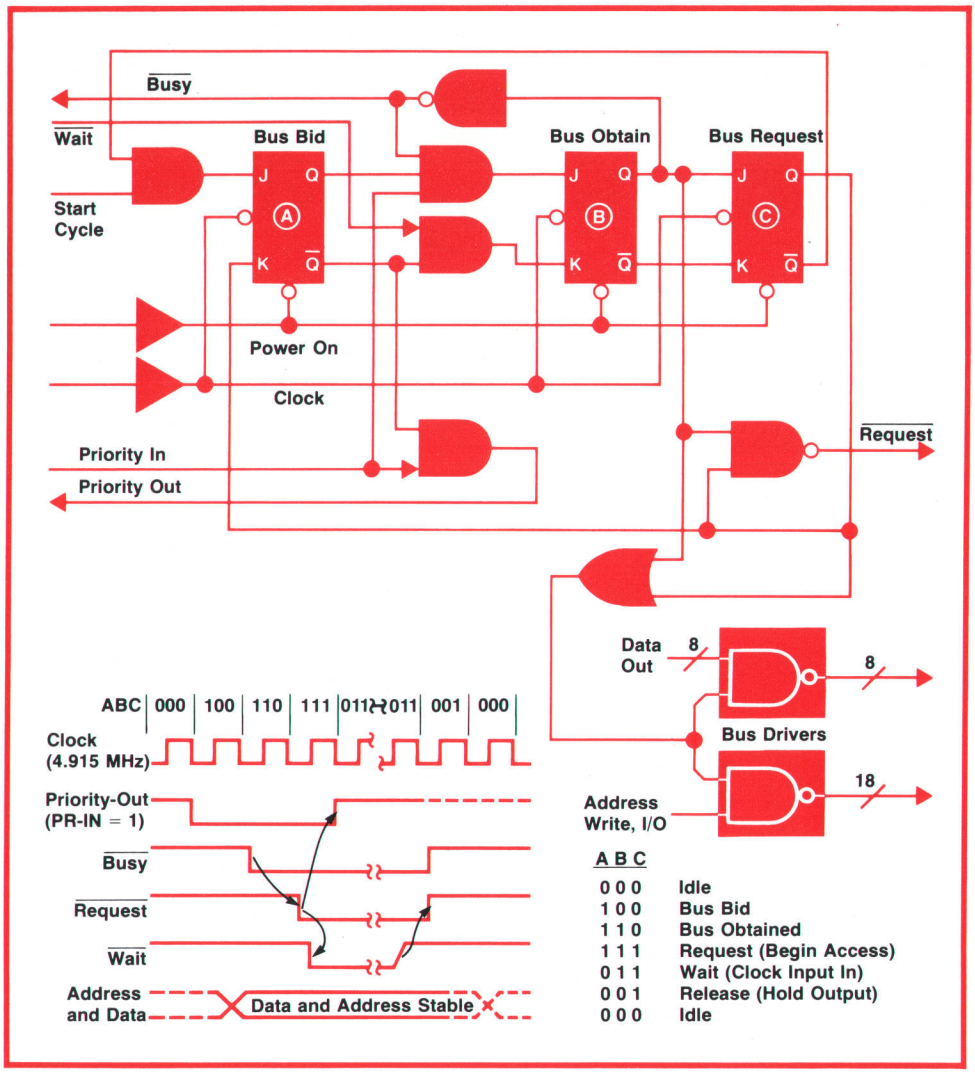


Fig. 2. *Each module has bus interface logic and is assigned a priority based on its position. The timing diagrams and truth table show the states of various control lines during a typical bus cycle.* REQUEST *is the command that ultimately causes the desired action to occur.*

address, and control lines for communication between the various logic functions. The terminal bus provides communication paths between processor, memory, input/output, and display refresh on a shared basis.

Before any module could be designed and placed on the terminal bus, rules had to be established to maintain electrical and operational compatibility. Standards have been set for bus drivers and receivers on the data, address, and control lines. A number of modules need to share control of the terminal bus, so a protocol has been established to decide which module has the bus and which will get it next. Also, conventions for data flow, addressing, and timing are standardized. All operations are synchronized with the system clock, but may be of various lengths (for example, for slow or fast memory).

Important features of the bus control scheme are its simplicity and flexibility. Address and data are stable before and after they are acted upon, so clocked registers or latches can be used on any module for data input. The design is very conservative and eliminates logic race conditions and timing problems. Asynchronous timing allows mixing of memory technologies, but the synchronous clocking makes it easy to design the individual modules. All modules are slot-independent and carry their own select code or memory address. This eases configuring. There are only two rules: group the three display modules together, and leave no empty slots between the power supply and the last module.

A bus access cycle begins when a requesting module determines it needs the terminal bus for instruction or data fetch or input/output. If the terminal bus is busy, the requesting module must wait until it is available. To determine who gets the bus next, a priority chain has been established. The modules nearest the power supply are first in the priority chain, and a module wanting the bus next breaks the chain for modules farther away from the power supply.

When the bus is not busy and the requesting

module has priority, then the requesting module is granted the bus. The requesting module then begins the bus cycle described in Fig. 2. Using the control lines WRITE and I/O, the requesting module specifies a memory read, memory write, input, or output operation. It also provides the address of the destination module. The key signal in the bus cycle is REQUEST, which is the action command that causes the modules to act upon the address and control information. The WAIT signal is used to extend a bus request cycle until data is ready. When the controlling module is finished, it releases the bus.

Microcomputer Module

The most important module to use the bus protocol is the microcomputer module. A commercially available microprocessor was selected over the alternatives of designing a custom LSI chip, which would have been expensive and time-consuming, or using standard logic, which would have taken too much power and space.

The microprocessor chip has 48 instruction types of one, two, or three bytes (characters) each, an accumulator, six registers, a program counter, an address stack for seven subroutine levels, and addressing capability of 16,384 bytes of program or data memory. The microprocessor chip alone could not do the whole job, so it was combined with standard logic functions to create a microcomputer card, Fig. 3.

The microprocessor chip has an eight-bit input/output bus. This bus is used not only for data, but also for a fourteen-bit address for memory and input/output operations. Four control outputs from the microprocessor chip are used to decode the various cycles or states necessary to multiplex data and address to and from the processor chip. Inputs to the microprocessor chip include power, two clock inputs, an interrupt request, and "ready", a signal that synchronizes the processor with the bus.

The microcomputer module has bus requesting logic as previously described. Bus requests for memory or I/O are decoded by the state decoder logic. The clock generator provides the two-phase clock inputs to the processor and generates other timing information which, when combined with the state decoder outputs, controls the other module functions.

During a typical instruction fetch, a sequence of processor cycles will output the address to holding registers (upper and lower of halves of the 14-bit address), wait for the memory, input the instruction, and finally execute the instruction. The instruction execution could begin additional cycles and bus accesses for data, or additional instruction bytes (instructions can be up to three bytes long).

Two other logic blocks, interrupt and restart, provide special functions for the microcomputer module. The interrupt logic initializes the microprocessor chip when power is turned on. The bus "power-on/reset" signal activates the interrupt signal to the processor, causing a special instruction to be fetched which starts the processor executing programs at memory location zero.

The restart block implements a conditional program interrupt to help service the data communications (computer) input. Restarts are placed in the program wherever an interrupt would be acceptable, but they are acted upon only when the hardware re-

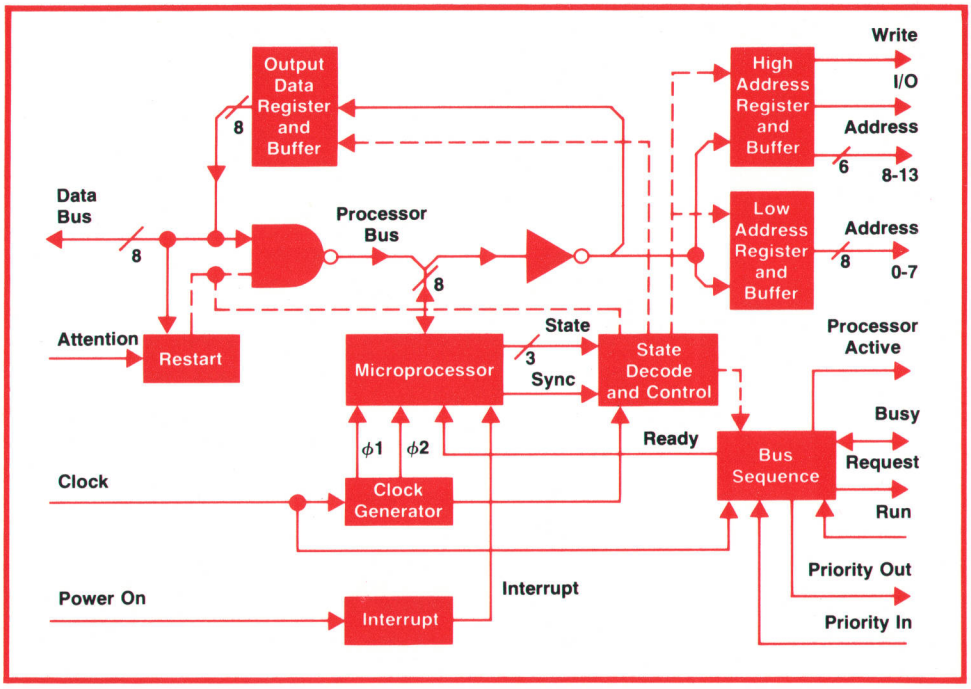


Fig. 3. *Microcomputer module controls all terminal functions except generation of character patterns and CRT drive. A commercially available single-chip microprocessor is its principal component.*

Data Communications

When it communicates with a computer system, the 2640A CRT Terminal is an ASCII, asynchronous, RS-232C-compatible terminal. This means that it conforms to the United States of America Electronic Industries Association Recommended Standard RS 232C (almost identical to CCITT V24), which defines electrical, mechanical, and logical interface standards for bit-serial, character-serial data transmission. Data characters are encoded according to the American Standard Code for information interchange (ASCII). Synchronization between sender and receiver is on a character basis rather than a block basis, i.e., transmission is asynchronous. Most computer terminals and all Hewlett-Packard computer systems use these same specifications for data transmission.

The 2640A provides five data transmission rates: 10, 15, 30, 120 and 240 characters per second.* There is also a special data clock input for externally generated transmission rates. This external clock allows the computer to set the transmission data rate at the receiver. The terminal also provides output data clocks for its five transmission rate settings, allowing the terminal to provide data timing. The use of external clocks is allowed only when the computer and 2640A are connected directly without telephone lines.

Communication over telephone lines requires a modem (modulator/demodulator), or Data Set as it is called by the Bell Telephone System. The 2640A is compatible with two modem types, Bell Telephone Data Set type 103 (30 characters per second or less) and type 202 (120 characters per second or less). Both of these modems support the asynchronous data transmission.

Hardware and Firmware

Data communications in the terminal is both a hardware and a firmware function. One of the standard terminal modules is the basic data communications card. This input/output card has the necessary logic to interface to the terminal bus and to the RS 232C interface. The card performs parallel-to-serial and serial-to-parallel conversion of data. The drawing shows a block diagram of the card.

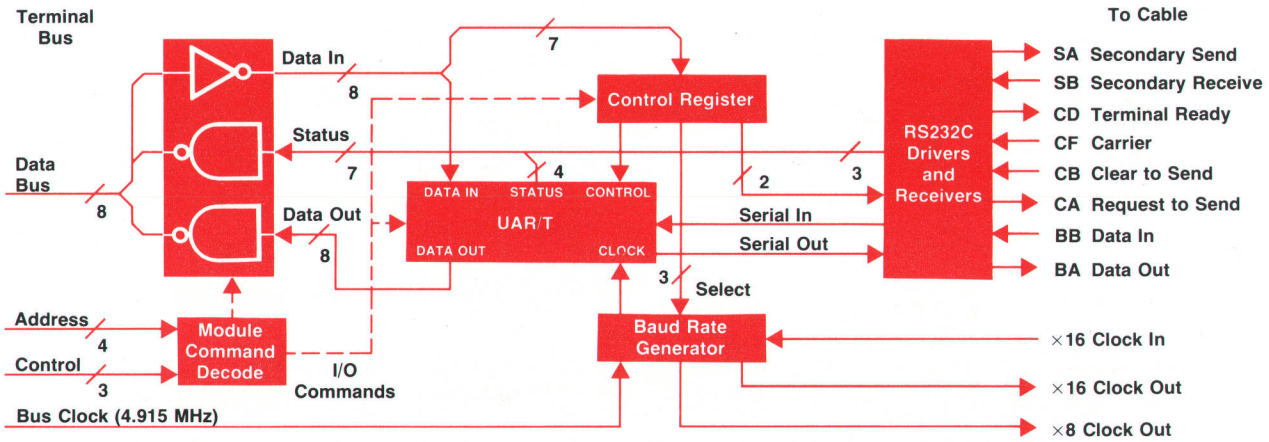
The RS 232C interface is implemented with special buffer integrated circuits that convert internal logic levels to those required by RS 232C. The control register holds information about the data format and the transmission rate; it is loaded from the terminal bus by an output instruction from the microprocessor. Two other bits in the control register implement an interface control line (Request to Send) and a break or interrupt condition on the data out line. The baud rate generator is a set of binary counters that divide the bus clock down to frequencies required for the standard transmission rates. The outputs of the counters are selected by logic controlled by the baud rate code in the control register.

The universal asynchronous receiver/transmitter (UAR/T) is an LSI integrated circuit that accepts parallel data out from the bus, serializes it, and adds the framing or synchronizing bits (start and stop). The UAR/T performs the reverse process for incoming data, converting serial data to parallel information and removing the start and stop bits. The UAR/T generates and checks parity if the control register contains the proper control code, and also detects data overruns. A status word gives the processor information about the data communication interface and the UAR/T. The hardware on the card has been minimized to keep the majority of control in the firmware programs executed by the microprocessor.

The terminal firmware for data communications has three main functions. First, the program transfers control settings from the keyboard, along with parity, transmission rate, and operating mode (full or half duplex) to the data communications hardware.** The same programs implement the transmit light, remote/local switch, and the break key. The second function of the firmware is to process input characters and to transmit data characters. Many decisions are made on incoming characters, especially on ASCII control codes. The data communications card basically acts as an input/output device for these terminal programs. The final area of concern is modem control using the interface control lines on the data communications board. The direct connect case and the Bell type 103 modem require minimum program control, while the Bell type 202 modem is more complicated. The type 202 modem allows data transmission in only one direction, so the modem control lines are used by the terminal and computer to "turn the line around" when the direction of data flow needs to be changed. The program logic to do this is combined with other firmware that implements block transfer. The computer decides who is to transmit and when.

*Data transmission rates are usually expressed in baud, which corresponds here to bits per second. Each character is 10 or 11 bits long.

**Half duplex: terminal displays keyboarded character and transmits it to computer. Full duplex: keyboard transmits character and displays character returned by computer.



Data communications module.

quires an interrupt. When the ATTENTION line of the terminal bus is low, indicating a processor interrupt request, the restart instruction causes a subroutine call to a special program to handle the needs of the data communications module. If ATTENTION is not set, the restart is changed to a no-operation and the program continues.

Terminal Memory

Like any other computer system, the microcomputer module is useful only if it has a program to execute and memory in which to store data. This is the function of the terminal memory modules, which are of two types, read/write or random-access memory (RAM) for storing display characters and data, and read-only memory (ROM) for storing terminal programs. Terminal programs are called firmware because the ROM makes them more permanent than software but less permanent than hardware. In the 2640A, one half of the available memory is dedicated to ROM or program memory and the balance of the available memory locations, 8192 bytes, can be used for RAM. All of the terminal memory is (MOS) semiconductor memory.

All of the memory modules, whether ROM or RAM, have their own independent control logic. The address logic uses the terminal bus control inputs and the most significant address lines (from 4 to 6) to decode the requested memory address and compare it to its own module address. Each memory module carries a jumper network to allow a memory start address to be assigned to that module. Whenever the module is accessed from the terminal bus, the timing and control logic provide control inputs to the memory chips, control data in and out of the module, and respond to the bus when the module has completed its read or write operation.

The basic memory module combines both ROM and RAM, and stores programs and data for the standard 2640A terminal. All of the terminal's ROM is on this module. There are four ROMs, each of 16,384 bits organized as 2048 × 8 bits. The beginning of ROM is location 0 of the memory address space; this is where the microcomputer module looks for its first instruction when power is turned on. Also on the basic memory module are 1024 bytes of static RAM memory.

Optional +2K and +4K RAM modules are added when more random-access memory is required for display and data storage. The optional RAM modules use the semiconductor 4K×1 RAM chip used by HP's 21MX computer family,[1] which requires periodic refresh to retain its contents. Both memory options provide additional control logic to perform this refresh function. This added control logic acts in conjunction with the basic control logic to perform pseudo-reads on sixty-four row addresses every two milliseconds. The +2K-byte memory does this by requesting control of the terminal bus every two milliseconds and performing a burst refresh lasting about 40 microseconds. The module requires control of the bus for gating the refresh address counter onto the bus and back into the memory address inputs. The +4K-byte option does it somewhat differently, taking a cycle-stealing approach. A refresh operation is done once every 32 microseconds on one row address when the memory module is not busy. After sixty-four of these individual row refresh cycles, the two-millisecond refresh requirement has been fulfilled. The address is gated to the memory chips within the module so no terminal bus operation is required.

Input/Output Modules

Also a part of the logic system are the three terminal input/output modules: the keyboard interface card, the data communications card, and the eight-bit duplex card (used for the HP 9866A Printer interface). None ever requests control of the bus, but all must respond to commands from the microcomputer and its programs.

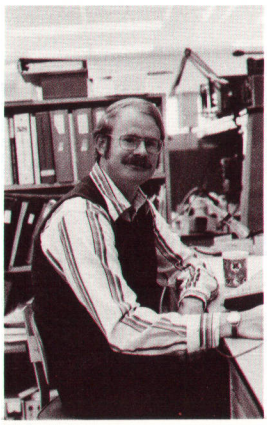
The basic I/O commands output data or control from the microprocessor and input data or status from the interface module. Each of the I/O cards has different data and control formats, but all are controlled by the microcomputer. Each I/O module has a rear edge connector for the attachment of a connector hood and cable assembly to carry the signals out the back of the terminal.

The display subsystem has two functions that use the bus. Cursor control is an output function and the DMA refresh is a bus requestor for memory read operations.

Reference

1. R.J. Frankenberg, "All Semiconductor Memory Selected for New Minicomputer Series," Hewlett-Packard Journal, October 1974.

Arthur B. Lane



Art Lane received his BSEE degree from Texas A&M University in 1969 and his MSEE from Arizona State University in 1970. He came to HP in 1972 with experience in data communications design. His principal contributions to the 2640A were the data communications module, the 2K and 4K RAM options, and the printer interface. Art was born in Lake Jackson, Texas, and now lives in Sunnyvale, California, just two blocks from HP's Data Systems Division, with his wife of six years. He enjoys backpacking trips, plays tennis and chess, and is a student of the Bible and the history of World War II.

A High-Resolution Raster Scan Display

by Jean-Claude Roy

IMPORTANT DESIGN OBJECTIVES for the display of the 2640A CRT Terminal were high quality and legibility of characters, along with low cost, high reliability, and ease of manufacture.

A raster scan deflection method, similar to that used in television sets, was chosen over the directed beam method used in oscilloscopes and some CRT terminals. In a raster scan display, the electron beam traverses the screen in a series of closely spaced horizontal lines, starting from the top. Characters are formed from line segments and dots produced by turning the beam intensity on and off at appropriate times.

For a low-cost alphanumeric display, the raster scan method offers several advantages over the directed beam. It doesn't require accurate, high-speed, and therefore expensive digital-to-analog converters. Instead, it uses counters on both axes to locate dots and characters. Second, the deflection circuitry need not have wideband, essentially identical channels; each axis can be optimized for its particular operating rate. Similarity with television techniques allows the use of low-cost television components in the deflection and high-voltage circuits. Finally, the raster display minimizes the power consumption of the monitor by means of an energy-conserving flyback-type horizontal deflection circuit (see box, page 14).

The 2640A Raster

The 2640A uses a low-profile CRT to keep overall height to a minimum while maintaining a screen capacity of 1920 characters, partitioned into 24 rows of 80 characters each. All of the character positions are fundamentally rectangles 7 dots wide by 9 scan lines high. Four additional scan lines beneath the 7×9 matrix are used for the descender areas of lower-case characters, for underlining, and for the blinking underscore cursor. One other dot is used on either side for character-to-character spacing, and one scan line is reserved at the top and bottom for row-to-row spacing. This results in a character cell of 9 dots by 15 scan lines replicated over the entire screen area (see Fig. 1).

A 25th row of 15 scan lines is used for the vertical retrace interval. Thus the total line count is 375 scan lines per frame. Domestic terminals operate with a 60-Hz frame rate, so the line rate is 375 × 60 Hz, or 22.5 kHz. This nonstandard line rate is used in the 2640A for two reasons. First, only the lines needed are generated, and second, an ultrasonic horizontal deflection circuit eliminates the 15.75-kHz "whine" that is characteristic of most raster-scan displays and is sometimes bothersome to operators.

Twenty-four additional column positions are used for horizontal retrace. With 9 dots per column a total of 104 column counts or 936 clock pulses define each scan line. This establishes the basic display clock at 936 × 22.5 kHz or 21.060 MHz.

Half-Shift and Character Enhancement

Fig. 1 illustrates an alphanumeric character designed around a standard 7-by-9 dot matrix. Because of the limited resolution of the matrix, most of the character's curves look somewhat jagged. This can be greatly improved by means of a horizontal shift of one-half dot to the right, thereby allowing dots to ap-

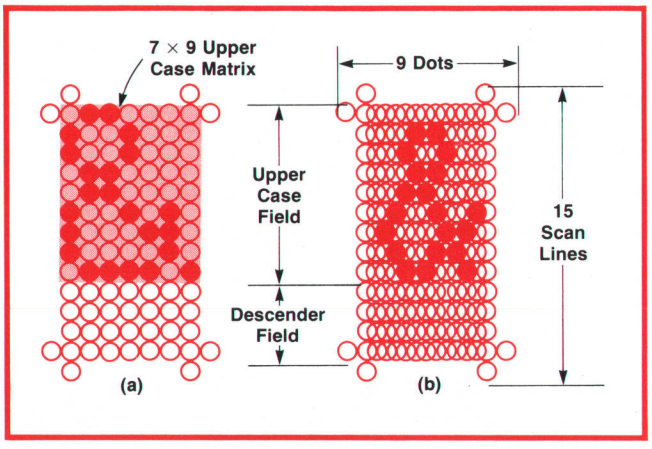


Fig. 1. *Basic 2640A character cell is nine dots wide by fifteen scan lines high, including spaces between characters and rows. Diagram at left shows an alphanumeric character designed on the basic 7 × 9 dot matrix. At right is the same character as it appears in the 2640A with the horizontal half-shift.*

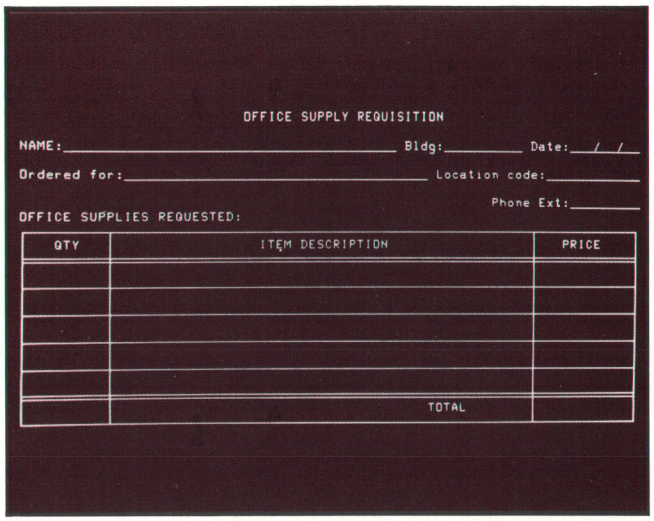


Fig. 2. *Optional 2640A line drawing character set is used for grids, graphs, and pictorial information.*

pear between the seven unshifted horizontal dot positions of the matrix. These interstitial dots increase the effective resolution of the cell to 13 by 9 points for an upper-case character. Fig. 1 also illustrates the same character enhanced by means of the half-shift.

Alphanumeric and Microvector Character Sets

Two types of character sets can be stored within the 2640A Terminal: alphanumeric sets and microvector sets. Alphanumeric sets support the primary use of the 2640A, displaying textual and numeric information. Characters are designed around a basic 7×9 dot matrix with provision for lower-case descenders. The characters are embellished by use of the half-shift. With this type of set the character-to-character spacing of two dots is hardwired. This prevents the design of characters that would form continuous horizontal lines. However, all 15 scan lines of the row are available so that vertically contiguous symbol segments can be designed. An example of this is the three-row-high integral sign found in the math symbol set.

Microvector sets use the entire 9-dot-by-15-scan-line character cell without the half-shift. This allows characters to be designed with both horizontal and vertical continuity. This type of set finds its greatest application where a minimal set of graphic kernels is needed to represent more complex pictorial information. Fig. 2 illustrates the use of the line drawing set in representing a form or application blank.

Display Features and Alternate Character Sets

The basic 2640A Terminal has a repertoire of 64 alphanumeric characters (128 optional) and one display feature, inverse video fields (black characters on white backgrounds). With the addition of the display enhancement board, up to three additional 128-character sets can be stored within the terminal. Three display features are also added: half-bright, underline, and blinking fields. All sixteen possible combinations of the four display features can be applied to any character or characters on the screen. No displayable character positions are required to start, stop, or modify either the features or the character sets. Therefore, consecutive characters on the screen may be from different sets or have different display features.

Display Circuits

A simplified block diagram of the basic display subsystem is shown in Fig. 3. The subsystem is divided into two major portions: display memory access (DMA) and display timing and control logic. The function of the DMA is to fetch blocks of ASCII characters from the memory and load them into a line buffer. The display logic converts the ASCII characters in the line buffers into a video signal. It also generates the CRT monitor drive signals and initiates the DMA's memory transfers.

There are two line buffers, each holding 80 eight-bit words. Seven of the eight bits are for the ASCII codes of the 128 characters addressable by the basic system, and the eighth bit is for the inverse video function.

At the start of each new row the appropriate line buffer is selected and an initiation command is sent to the DMA. The display logic circulates through the 80 words of the new line buffer fifteen times, once for each scan line of that row. The ASCII data forms the seven most significant address bits for the character ROMs. The four least significant ROM address bits are supplied by the modulo-15 scan-line counter. The character ROMs then output the proper control signals for the CRT monitor.

After the initiation command the DMA continues threading through the chained display memory and loads the second line buffer with the next line to be displayed. Each displayable character encountered is loaded into the line buffer. This continues until 80 characters are loaded or an end-of-line (EOL) or end-of-page (EOP) control word occurs. When either of these occurs the DMA finishes the line or page with blanks.

If a display control word is found with the inverse video bit set, the DMA sets its inverse video buffer flip-flop. All subsequent characters in the line buffer are then inverted until a new display control word is found in which this bit is not set. Thus the inverse video display feature may start and stop anywhere in a row without wasting character positions.

Once per frame a synchronization signal is sent to the DMA during vertical retrace to force the address register to the first word of the display memory. This

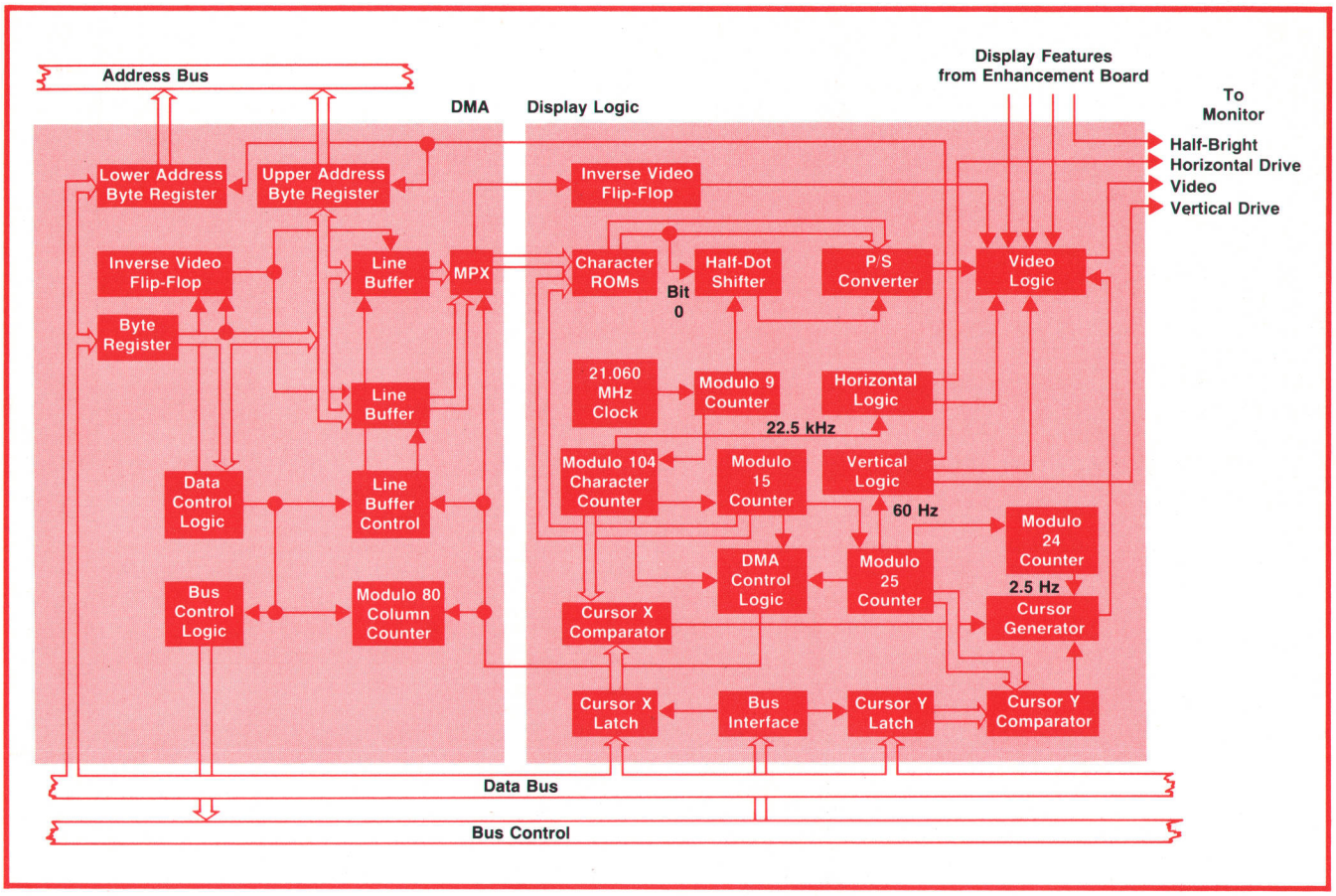


Fig. 3. *2640A display subsystem.*

insures that the display hardware and the firmware pointers operate in unison and no inadvertent rolling of the screen occurs.

The sequential operation of the DMA depends on the data control logic, which decodes incoming memory links, EOL, EOP, ASCII characters, and display control words. ASCII characters increment the column counter and all memory fetches halt when this counter reaches 80 counts. Data transfers are initiated for the next row upon receipt of the interrupt command, which clears the counter. All bus-related operations are handled by the bus controller logic, which requests the bus and controls the transfer operation.

The source of all raster synchronous timing is the display clock of 21.060 MHz. A nine-bit ring counter provides dot-related timing signals for the half-dot shifter and drives the character/column counter. The output of this modulo-104 counter is at the horizontal line rate of 22.5 kHz. The scan lines are subdivided into clusters of 15 per row by the modulo-15 counter. In turn, the rows are divided by 25; 24 are displayed on the screen and one is for vertical retrace. Finally, the 60-Hz frame rate is again divided by 24 to provide the 2.5-Hz blinking signal for the cursor.

The horizontal logic generates the horizontal blanking signal to turn off the CRT beam during horizontal retrace. It is also the source of the horizontal drive signal for the monitor. Similarly, the vertical logic provides the vertical blanking and drive signals.

The shifter is controlled by bit 0 of the ROM output word, which is the half-shift control bit. When it is set the shifting signal sent to the parallel-to-serial converter is delayed by one-half clock period. This has the effect of shifting the serial dots one-half dot width to the right.

The output of the parallel-to-serial converter is a serial bit stream. It is merged with the inverse video control signal, blanking signals, any display signals from the display enhancement board, and the cursor. The resulting composite video is finally sent to the monitor's three-state video amplifier. There it is merged with the half-bright signal to form characters of either full, half, or no intensity.

The cursor's position is loaded by the processor into X-position and Y-position latches. These absolute coordinates are constantly compared against the instantaneous row and column positions of the beam as it sweeps the raster. Upon coincidence a cursor signal is sent to the video logic.

2640A Sweep System

The sweep system of the 2640A Terminal, shown in the block diagram, is designed for good spot size and definition, stability, and linearity along with low cost, low power, and high reliability.

The CRT is a custom design with a low-profile aspect ratio of five inches by ten inches (12.7×25.4 cm), optimized for alphanumeric text. The deflection angle of 70°, large neck diameter of 2.85 cm, and electron gun design provide outstanding resolution, both at the center and at the corners of the screen, with no sacrifice of brightness or efficiency.

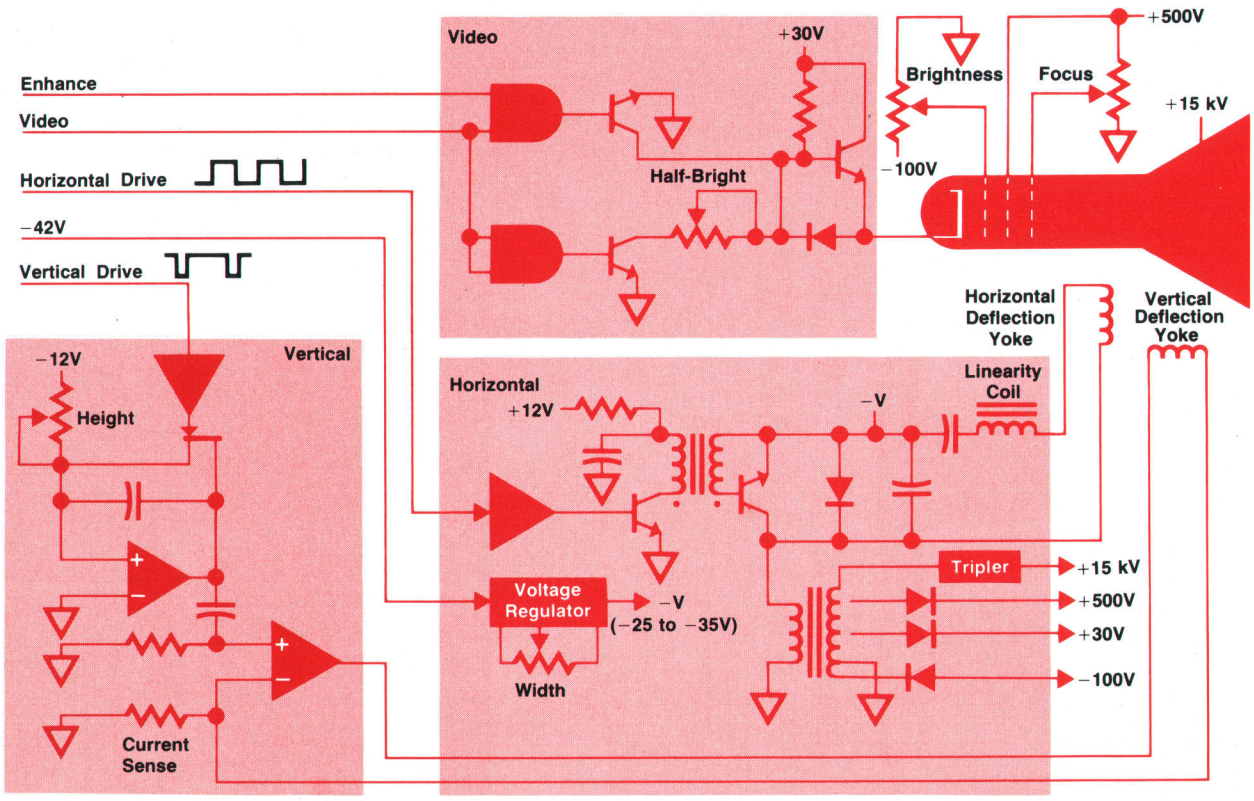
The video circuit receives TTL video signals from the display system and amplifies them to a level suitable to drive the CRT. Good spot crispness on the screen requires a fast signal at the CRT cathode—approximately 20 ns on and 40 ns off. An optional feature is a half-bright level that can be actuated by the display logic.

The vertical scan circuit consists of an integrator that generates a voltage ramp and an amplifier that drives the vertical deflection yoke with a current proportional to the ramp. The amount of electron beam deflection is proportional to yoke current, so this method provides excellent linearity. The TTL vertical drive signal is normally high during the sweep and goes low during vertical retrace.

To avoid the annoying whistle that radiates from most CRT systems, the horizontal and high-voltage circuits are designed to operate at a line rate of 22,500 Hz, well above audibility. Cost was kept down by using inexpensive television-type components wherever feasible. Power was minimized by using a standard "ringing" yoke circuit, which is typical of most high-frequency CRT scan systems. The linearity coil is an inductor specifically designed to correct for nonlinearities introduced by the horizontal output transistor and yoke.

Sweep width is controlled by varying the voltage applied to the horizontal output transistor. This method has the advantages of eliminating a variable inductor as a width control and reducing circuit sensitivity to power-supply variations.

George Crow



Display Enhancement Board

The display enhancement board (DEB) has two functions. First, it is the source of the half-bright, blinking, and underline display features and the character set select bits. These are obtained by loading additional line buffers located on the DEB when a display control word is found in the display memory. These line buffers are in parallel with those on the DMA and under its control. This has the effect of widening the DMA line buffers to include the other display features and alternate-set select bits without burdening the minimum system.

The second function of the DEB is to hold the three additional 128-character sets and to control set selec-

2640A Power Supply

The power supply used in the 2640A Terminal was designed to meet several important design objectives. It had to be capable of supplying enough power for the maximum demands of the terminal plus some excess for future expansion of the system. It had to satisfy the regulation requirements of the system electronics, but be efficient and fit in a reasonably small space. It had to be low in cost and easy to manufacture and repair.

The power supply is designed to operate with an input voltage of 88 to 125 volts on a nominal 115-volt line or 196 to 250 volts on a 230-volt line, and at a frequency of from 47 to 64 Hz. The output specifications are:

Output Voltage	Output Current
+5 ± 3%	2 A min, 6 A max
+12 ± 5%	1.5 A max (3A max pulsed)
−12 ±5%	1.5 A max (3A max pulsed)
−42 +10, −5%	0.6 A max

Efficiency is about 70%. The supply provides full output power of 92 watts with an input power of 125 watts.

A switching mode power supply was chosen because of the efficiency and space requirements. The incoming power passes through an RFI filter and then is either voltage-doubled (115-volt operation) or rectified (230-volt operation). Switching transistors are turned on alternately and their on times are modulated to regulate the output voltages. Base drive for the switching transistors and primary current sensing is done by three small transformers mounted in one case. Only the +5-volt output is sensed and directly regulated. However, matching between the supplies is good enough so that they all stay within their rated voltage tolerances. A circuit on the regulator card senses a low line condition, and completely shuts down the supply before the line voltage drops enough to put the supply out of regulation. When the line again rises to the minimum line voltage at which the supply will regulate, the supply will again start normal operation. A current limit circuit shuts down the supply if primary current becomes excessive. The supply will recover once the source of the overcurrent condition is removed.

To make repair and manufacture simple, the supply is constructed on two printed circuit boards. One, the mother board, contains the power elements including all large filters, inductors, and switching transistors. The smaller board contains the low-level components and regulating elements. The entire power supply can be removed from the terminal without tools, or the low-level card may be unplugged from the supply. The printed circuit layout was kept simple and open to allow easy access to all components. Several test points are included to aid trouble shooting.

Costs were minimized by using integrated circuits wherever possible to keep component count down. Only four transistors are used in the supply. Coupling transformers are used to isolate the primary and secondary circuits because of their reliability and low cost. Except for the inductors, all the components used in the power supply are standard off-the-shelf items, and were selected for cost and reliability.

George Crow

tion. Six ROM sockets are provided for 64-character ROMs. Each set is jumper-programmable for either 64 or 128 characters and can be of either the alphanumeric or the microvector type. The two set-select bits from the line buffer are decoded and are used to enable one of the four character sets. When an alternate set is selected, the basic character set is disabled.

The shifter on the DEB is slightly more complex than that in the display logic because the microvector sets use the entire 9-dot-by-15-scan-line character cell. The set type jumper of the selected set is read and the appropriate logic within the shifter is activated.

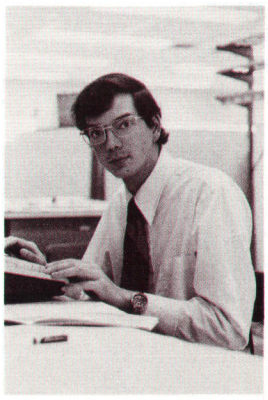
Character ROM Organization

The basic 2640A has a single 64-character alphanumeric set. It is stored in an 8192-bit bipolar ROM, organized as 1024 words of eight bits each. Each character occupies 16 consecutive words of which 15 are addressed, one per scan line. This allows the design of vertically continuous special characters that cross row boundaries. Bit 0 of the eight-bit word serves as the half-shift control bit. The other seven bits correspond to the seven dot positions of the basic character cell. When 128 characters are desired a second ROM is added. It stores the 32 lower-case characters and the 32 control characters of the ASCII set.

Microvector character ROMs have 9216 bits organized as 1024 words of nine bits each. Again each character occupies 16 words of which 15 are addressed. In this case each bit corresponds to a dot on the 9-dot-by-15-scan-line character cell. The two types of ROMs are physically identical and interchangeable. Electrically, the ninth output bit of the microvector ROM is an enable input on the alphanumeric ROM. This difference is taken into account by the jumper logic and in turn by the shifter.

Acknowledgments

Thanks are due George Crow for his excellent monitor design. George's insights into television circuits have contributed significantly to the quality of the display.



Jean-Claude Roy

Born in Montreal, Canada, Jean Roy did his undergraduate work at the University of California at Davis, graduating in 1970 with a BSEE degree. He joined HP's Santa Clara Division the same year and helped develop the software for the 5407A Scintigraphic Data Analyzer. Now with the Data Systems Division, he was responsible for the organization and logic design of the 2640A display. In 1974 he received his MSEE degree from Stanford University. A bachelor and a gourmet cook, Jean spends much of his leisure time woodworking, painting, and reading. Sunnyvale, California, is his home. He's a member of IEEE.

Firmware for a Microprocessor-Controlled CRT Terminal

by Thomas F. Waitman

THE HP 2640A CRT TERMINAL was from the very beginning viewed as the first of a family of terminals that would serve many different needs. To implement this goal without making large changes in the basic hardware, it was decided that wherever possible, the required logic would be implemented in firmware (microprocessor programs stored in read-only memory).

The firmware approach has made it possible to make almost all of the functions of the terminal operate the way the typical user would like them to operate. Many of the more powerful functions are transparent to the operator. In a conventional terminal, most or all of the logic is implemented in hardware, and there are frequently compromises in how the features work because of the complexity of the hardware required to handle special conditions. While this factor is still present in a firmware-based system, it is much easier to handle special situations in a way that is consistent with what the user would really like.

System Monitor

The monitor is a section of the firmware that dispatches data within the terminal. The processor normally executes a basic loop, in which it scans the keyboard and the data communications interface and waits for something to happen (see Fig. 1). When a character is received from either the keyboard or the data communications interface a general character interpretation subroutine is executed to determine the action to be taken. The monitor then performs the specified functions, such as putting a character on the display, transmitting a character over the data communications interface, or moving the cursor. When this has been completed, the monitor returns to the basic scan loop to look for the next input.

I/O Subsystem

The I/O subsystem contains the firmware required for performing all input/output functions. The firmware operates without the benefit of a true interrupt. All inputs from devices such as the data communications interface and the keyboard are found by scanning these devices. If a new key depression is detected, the key number associated with this key is calculated and used as an index into a table that assigns a code to the key. If the key is one of the ASCII keys, the proper code is determined based on the state of the control, shift, lock, and caps lock keys.

If the key in question is not one of the ASCII keys, the firmware may be required to generate a multiple character sequence consisting of an ASCII escape character followed by one or more characters that define the escape sequence. Keys in a third group do not generate codes at all, but simply perform internal terminal functions, such as block mode, remote, and caps lock.

I/O associated with the display is minimal because the display memory access module (DMA) causes the display to be refreshed without processor intervention. Display I/O control mainly involves transmitting the cursor coordinates to the display whenever necessary and turning the DMA off whenever there is a potential interaction between the firmware and the DMA.

Data communications is a good example of an area where a great many hardware/firmware tradeoffs were made. Originally it was felt that the processor could do the parallel-to-serial conversion of the data. Later, it became clear that the processor did not have the necessary speed to perform this function, so the function was implemented in hardware. This made the firmware required for the Bell type 103 modem and for hardwired connections trivial.

The problem of data communications protocol for the type 202 modem was more complex. A significant amount of firmware development time went into the definition of the 202 protocol to make the 2640A compatible with existing HP systems. The basic algorithms are entirely implemented in firmware and make the 2640A a slave to the external computer.

Cursor Movement

The 2640A firmware contains many subroutines for moving the cursor around on the display. All cursor movement is handled by the firmware. When a character is typed on the keyboard and appears on the display, the cursor moves to the next column posi-

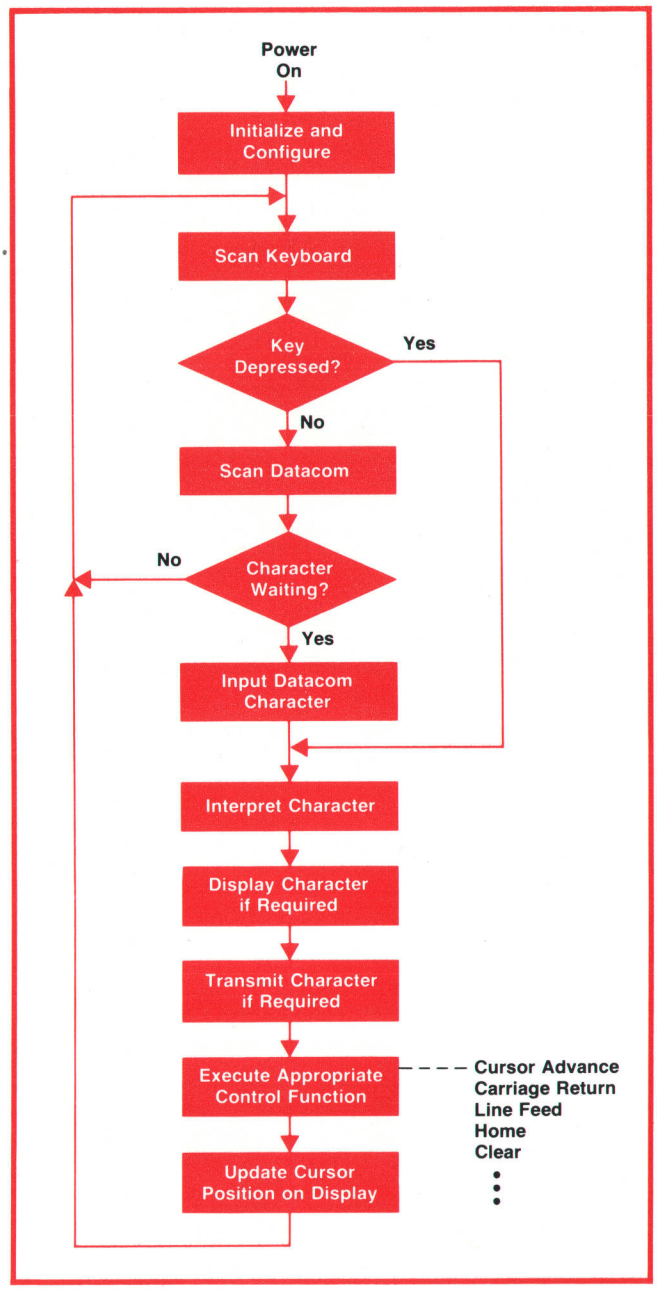


Fig. 1. *The microprocessor normally executes a section of firmware called the system monitor, a basic loop in which the processor scans the keyboard and data communications interface and waits for something to happen. When a key is pressed or a character received, the appropriate subroutine is executed.*

tion because a cursor advance subroutine has been executed and has calculated the new cursor position. Similar subroutines exist for moving the cursor up, down, right, left, and home. The tab function is also a firmware routine; it uses a one-bit-per-column table to determine the next tab stop.

Display Memory Management

The largest part of the 2640A firmware is devoted to management of the display memory. In addition to the obvious fact that most of the 2640A is centered around the display, several crucial design decisions led to this result. Early in the design the decision was made to use memory as efficiently as possible, because this would make it possible to store a maximum amount of useful information on the display. Most conventional terminals use a byte of display memory for every displayable position on the CRT screen. If there are many short lines, as is frequently the case, there is a substantial amount of unused memory. The 2640A does not allocate memory for character positions to the right of the last character entered, so this memory is available for other purposes. It was also felt desirable to be able to turn on or turn off the various display enhancements and character set selections, or start and end unprotected fields, between individual characters without an intermediate blank character position. With these features, the address of a character occupying a given row and column cannot be directly computed without some sort of scanning process. Because cost considerations allowed no special hardware for moving data around in memory and for scanning, a scheme had to be designed to permit fairly rapid movement through memory by the processor.

The display memory consists basically of a linked list of fixed-size blocks of RAM (see Fig. 2). This list is set up in such a way that the DMA can start at the first address on the screen and follow the list to produce an entire screen of information. All memory not currently allocated for display use is kept on a free-storage link list. Individual rows are linked with next and preceding rows, while blocks within a row are linked only in a forward direction. The storage allocated for a row may be as little as one block (16 bytes), or much larger than 80 characters, depending upon the number of displayable and nondisplayable characters needed to create the row on the CRT.

The firmware finds the address corresponding to a given character position by starting at the last known position and moving through the list either backward or forward until it finds the new address. If the end of the list is found before the row in question has been found, blocks are removed from the free-storage list and used to create new rows. Once the correct row has been found, the firmware searches for the cursor column. If the end of the row is found before the column has been found, additional blocks are removed from the free-storage list and used to build the length of the row out to the column required. Whenever a block is required and the free list is empty, an existing row must be released from display memory. This row is the first row of memory if the addition is at the end of memory, and is the last row of memory if a row other than the last row is being lengthened.

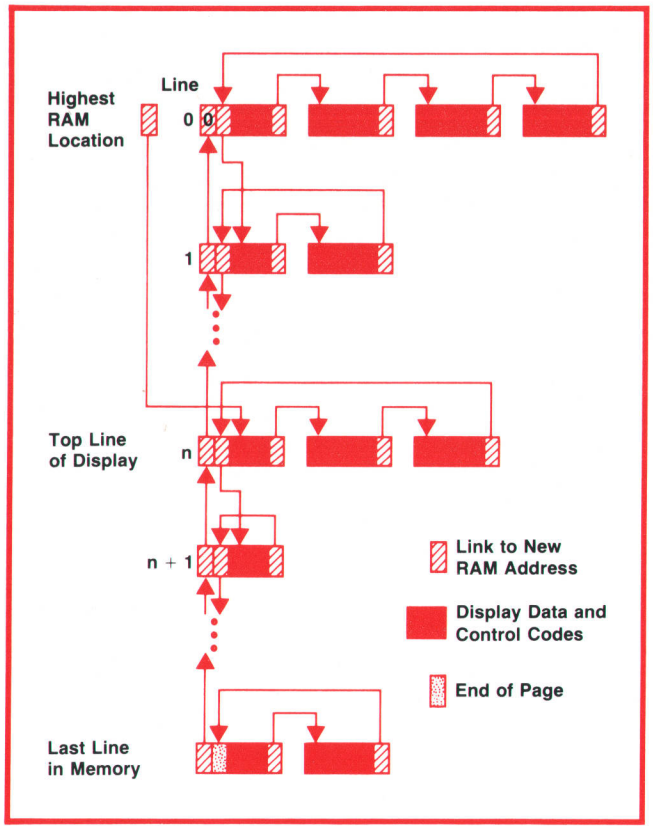


Fig. 2. *Display memory consists of a linked list of fixed-size blocks of RAM. The display system starts at the first address on the screen and follows the list to produce an entire screen of information.*

Editing Features

The editing controls are implemented by firmware within the link structure. Four editing controls are provided: character insert and delete, and line insert and delete. The latter are performed quite easily, as they simply involve adding or deleting an entry in the link structure. Character insert and delete involve moving information one way or the other through the structure, and hence involve a large number of boundary conditions. Although character insert and delete are time-consuming functions as measured by electronic speeds, they seem to happen more or less instantly to the human sitting at the display. These functions are extremely useful in block mode, and when combined with the enter function, can be used to considerable advantage in character mode.

Format Mode

Format mode allows the user to define certain areas of the display as protected, and others as unprotected. When the terminal is placed in format mode, only the unprotected areas may be modified. This allows a user to create a form in which only those areas to be filled in by the operator are unprotected. The operator can then fill in the blanks in the form without danger of destroying the form itself. The firmware implications of format mode are extensive, because many of the basic terminal functions operate differently in format mode and non-format mode. Some examples of the changes in functions are:

- The home function moves the cursor to the first unprotected field on the CRT.
- The tab function positions the cursor to the first column of the next unprotected field rather than to the next horizontal tab setting.
- The erase functions erase only the unprotected fields.
- Character insert and delete operate within the current unprotected field rather than the current row.
- In block mode, only data from unprotected fields is transmitted to the computer.

Block Mode

Block mode is the mode of operation that makes best use of many of the terminal's functions. With the block mode key released, the terminal operates in character mode, in which characters are transmitted to the computer as they are typed. In block mode, nothing is transmitted from the terminal to the computer unless explicitly requested by either the computer or the operator. This allows the operator to compose text on the display, edit it until he is satisfied, and then send it to the computer as a block of information. It also allows the computer to ignore the terminal while the operator is creating the information, and allocate input buffer space only after the terminal has requested it. Information may be transferred to the computer in blocks consisting of a single unprotected field, a single line, all unprotected fields with a separator between fields, or an entire display memory. Which of these four options is in use is determined by the operating mode of the terminal and an internal jumper.

This protocol makes block mode capability usable not only on systems that are specifically designed to accept large blocks of data at a time, but also on systems that expect no more than one line at a time.

Novel Terminal Functions

The 2640A has several functions not generally found in CRT terminals. For example, the status of the terminal can be read by the computer by means of an escape sequence. The terminal returns an ASCII string that gives information about memory size, the state of the jumpers, the current status of the latching keys, and the states of several transfer and error condition flags. This information is useful for determining whether a terminal is configured properly for a given application.

Testing the HP 2640A

The HP 2640A contains a built-in self-test feature. Pressing the TEST key on the terminal's keyboard causes an internal diagnostic to be executed. The internal diagnostic checks both memories (ROM and RAM), and exercises the display and keyboard controls. By observing the actions of the diagnostic and the resultant display, the operator can determine whether or not the terminal is functioning properly.

In servicing the terminal, one may require more thorough and detailed testing than provided for by the self-test routines. This is the role of the external diagnostic. Typically, diagnostics for a device are very much different from system to system and service personnel have to learn all of the different diagnostics. To minimize this source of confusion, a decision was made to perform all testing within the terminal. The external system would provide for test selection, loading of the diagnostic, execution monitoring, message reporting, and the control interface between the user and the diagnostic. Microcoded tests would be down-loaded into the terminal and executed by the terminal's microprocessor.

This required the implementation of a microcode loader in the terminal. Because binary code cannot be handled by all systems, the code is transmitted as ASCII characters that are translated by the loader in the terminal to binary code. ASCII is the normal communications code for the terminal. Therefore, virtually any system operating the terminal can load and execute the diagnostic.

Besides the different systems the diagnostic had to handle, there is also great variety in 2640A terminals. The diagnostic had to be able to test the minimum terminal configuration, and yet not be restricted in handling the various terminal options. Allowances also had to be made for future expansion of the terminal.

The required flexibility is provided by organizing the diagnostic into subtest blocks. Each block is self-contained except for a block of data communications drivers common to all subtest blocks. A single test consists of one or more subtest blocks. By adding or deleting a subtest block, one can tailor the diagnostic to the specific terminal being tested.

Each subtest block is made up of a number of ASCII records consisting of a header record, the object microcode, and messages. The header record contains the test title, test and subtest sequence number, and flags indicating the terminal configuration for which the subtest is valid. The object microcode portion contains all the necessary characters for loading the subtest object code after the terminal's loader is initiated by the external system. The message portion contains all the messages used by the subtest. Output from the microcode subtest indicates which message to use and the values to be inserted in the message.

The user provides the external monitor program for the particular system from which the diagnostic is to be executed. However, three versions of the monitor are supported by HP: HP 3000, HP 21MX, and HP 2000F Timeshared BASIC. Initiation and control for each version differ, but the specific tests are identical because the same microcoded tests are used.

As a result of this effort, the 2640A diagnostic can be run on virtually any system operating the terminal. Having a common diagnostic shortens the training period for service personnel and facilitates troubleshooting of the device.

Edward Tang

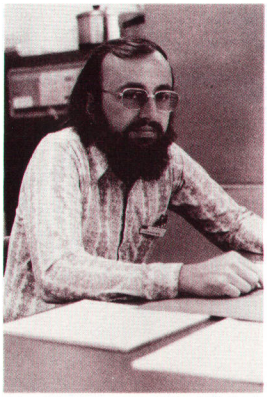
Display functions is a mode of the terminal that causes all characters received by the terminal to be displayed on the screen and not interpreted. This is an extremely useful debugging tool that makes it possible to see the exact code sequences being sent to the terminal, and hence to determine whether a program is performing as it should.

Memory lock is a feature that operates in one of two modes. If the function is enabled when the cursor is in the top row of the display, then total memory lock is in effect. In this mode, when all of the available terminal memory has been used, the terminal will no longer accept input. This mode is convenient for filling the memory with a maximum amount of information without the risk of losing data already entered. If memory lock is enabled when the cursor is in any row other than the top row of the display, all rows of the display above this row are fixed on the display. When a rollup is executed, the rows below this area are rolled around the area and reinserted into the off-screen storage immediately above the display. This mode is useful for placing instructions for an operator on the display and then using the lower portion of the display for interactive operation.

Acknowledgments

Ed Tang developed an excellent diagnostic strategy for the 2640A, and wrote all of the diagnostic microcode and the 21MX Computer diagnostic monitor. He also made several significant contributions to the overall firmware design. Ron Grant was involved in the early diagnostic effort and wrote the diagnostic monitor for the 2000F Timeshare System.

Thomas F. Waitman



Tom Waitman, now project manager for terminal firmware at HP's Data Systems Division, was responsible for development of the 2640A firmware. He came to HP in 1972 with five years' experience in the design of medical information systems, electronic countermeasures equipment, and electronic telephone switching systems. Born in Prescott, Arizona, he received his BSEE degree from the University of Arizona in 1965, and his MSEE degree from Massachusetts Institute of Technology in 1967. Tom is a bachelor with a strong interest in children. He has two foster sons (ages 9 and 11), is involved in the Big Brother program, and serves as a director of a school for children with learning disabilities. He also enjoys skiing, camping, and music.

A Microprocessor-Scanned Keyboard

by Otakar Blazek

THE FIRST DECISION made in designing the 2640A keyboard was what keyswitch to use. For high reliability and low cost, the choice was the contactless ferrite core switch. Its advantages are no moving contacts, no bounce, no variations in contact resistance, high reliability, and a long life expectancy of 100 million cycles.

For the system design, two approaches were considered. One was to design hardware that recognizes a depressed key and interrupts the processor, indicating which key was depressed. The other was to have the processor scan the keyboard at discrete intervals and let the software or firmware recognize a depressed key. Considering low cost as an important design goal, it turned out that the processor-scanned keyboard was superior. This approach also meant fewer parts and therefore higher reliability.

The keyboard was designed with *N-key rollover*, meaning that a depressed key will be recognized regardless of the state of any other key on the keyboard. To prevent double triggering for extremely slow typists, *hysteresis in key travel* was introduced. A key depressed to the threshold of the on state must be partly released to reach the off state. *Automatic repeat* is achieved by holding a key down longer than 0.5 second.

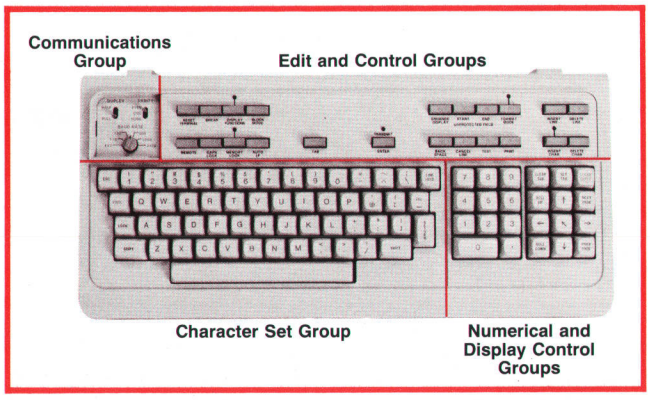


Fig. 1. *Keys are partitioned into groups according to their function. Data communications switches are also located on the keyboard. The status of some keys is indicated by light-emitting diodes. For user convenience the keyboard is attached to the terminal by a five-foot cable.*

Hardware Organization

The keyswitch used consists of a ferrite core, a drive wire, a sense wire, and two magnets. When the switch is not depressed the two magnets are close to the core, thus saturating it and inhibiting the coupling of a signal from the drive wire to the sense wire. When the switch is depressed, the magnets are moved away, the core unsaturates, and the drive signal is coupled into the sense line.

Each key is assigned a position in a matrix of sixteen columns and eight rows (see Fig. 2). Each column in the matrix is addressable, so the processor reads eight switches at a time. Only the selected column is allowed to provide the drive current that is coupled into the sense lines of depressed switches. Before the present state of the switches in one column is read, the column's previous state is loaded into an eight-bit latch. The latch outputs set the reference voltages of differential comparators to either higher or lower thresholds. The differential comparators detect the sense outputs of the keys. Because the sense output is proportional to the amount of key depression, hysteresis in key travel is established.

The processor also loads the display latch that determines the states of the LED indicators.

Firmware Organization

Because each column is scanned at regular time intervals it is necessary to store in memory the previous state of each key to recognize a change in the state of a key. There are four possible combinations:

Previous State	Present State	Action
0	0	None
0	1	Key has been depressed
1	1	Key is held depressed
1	0	Key has been released.

The keyboard scanner (see Fig. 3) is a subroutine called by the system monitor. Each time this subroutine is called, one column (eight switches) is scanned. When a depressed key is recognized an ASCII code from a table in memory is assigned to the key.

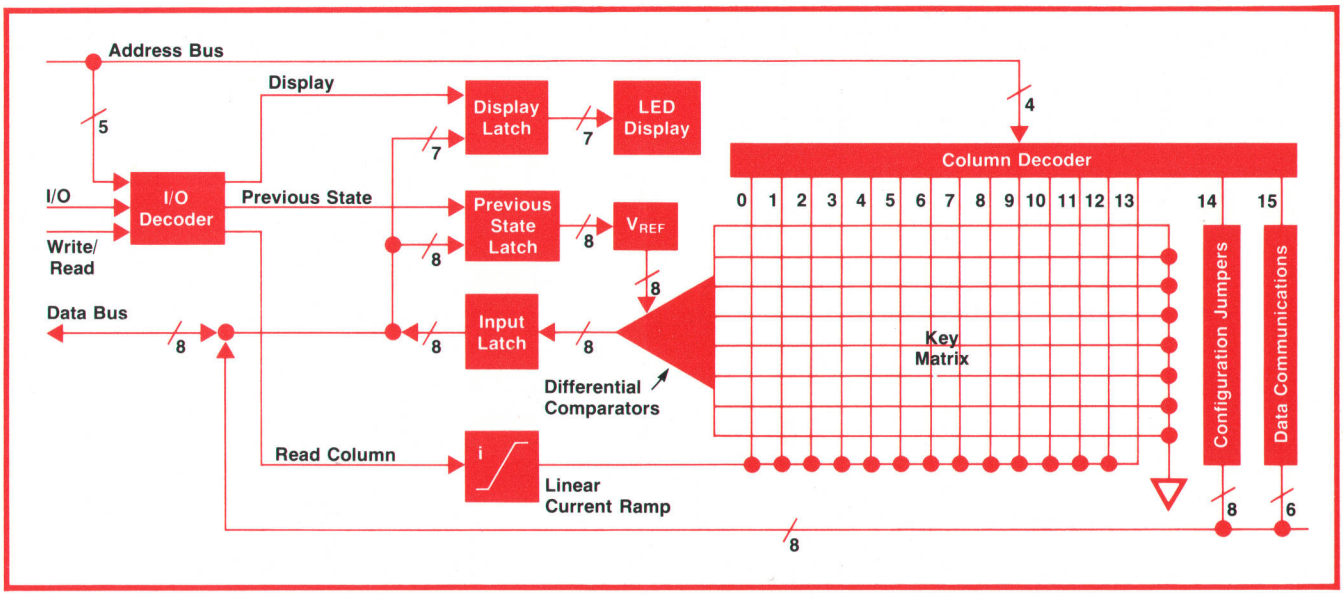


Fig. 2. *Keyboard hardware implementation. Each key is assigned a position in a matrix of sixteen columns and eight rows. The microprocessor scans this matrix continuously, reading one column at a time.*

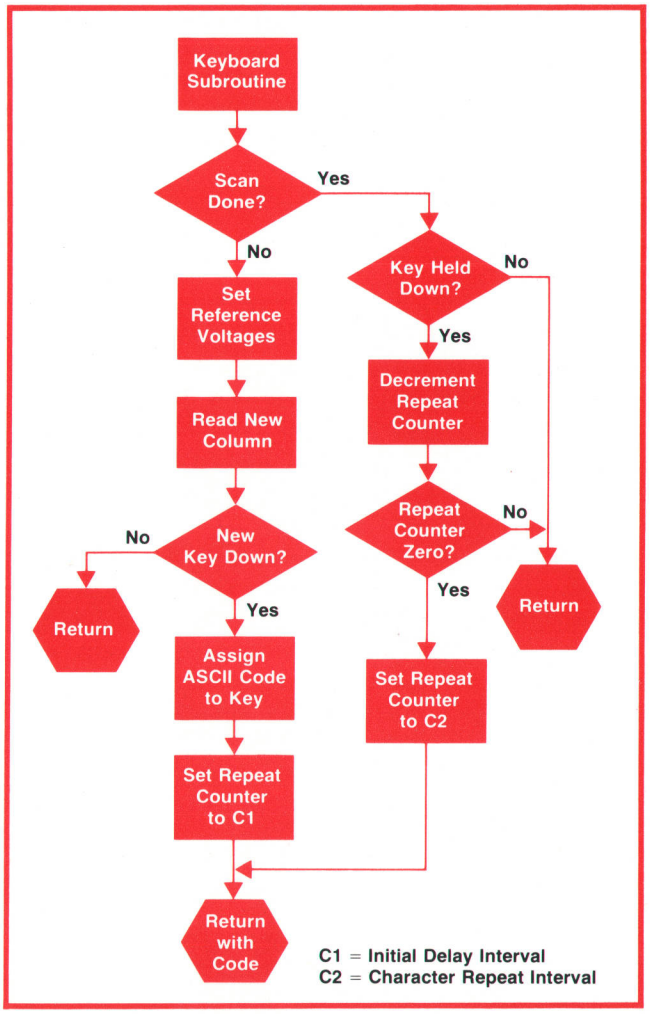


Fig. 3. *Simplified keyboard scanner, a firmware subroutine called by the system monitor.*

Automatic repeat is achieved by setting a repeat counter to a predetermined value C1 when a key has been depressed. When all 16 columns have been scanned the counter is decremented. When the count is zero the character is displayed and the repeat counter is reinitialized to another value C2. C1 determines the time between the first and second characters on the screen; thereafter, the repetition rate is determined by C2.

Acknowledgments

I would like to thank David DeMoss for the mechanical design of the keyboard.

Otakar Blazek

Oty Blazek holds the equivalent of an MSEE degree from the Technical University of Pilsen, Czechoslovakia, his birthplace. He graduated in 1963. In 1971 he received another MSEE degree, this one from the University of California at Berkeley. Before coming to HP in 1972, he worked as a production engineer in Czechoslovakia, Germany, and California. At HP, he has contributed to the design of the HP 3000 Computer and designed the 2640A keyboard and ROM. Oty speaks five languages: Czech, English, German, Russian, and some French. He's single, lives in Santa Clara, California, and enjoys skiing and tennis.

Packaging for Function, Manufacturability, and Service

by Robert B. Pierce

THE PACKAGING OF A CRT terminal presents diverse challenges. A CRT terminal must be exceptionally suited to user requirements, much in the manner of a typewriter, keypunch, or other device with which the operator may spend the entire day. Human factors such as height and viewing angle of display, height and slope of keyboard, relative location of keyboard and function switches, and access to I/O cables can be sources of pleasure or frustration to the operator.

In addition to the user requirements, there are requirements of manufacturing and service. Fabrication, assembly, testing, and repair times must be minimized. The time to gain access to and replace modules must be as short as possible. Like users, manufacturing and service personnel have thresholds of pleasure and frustration. The goal was to make the 2640A a friendly device to all.

Three Major Modules

The 2640A is housed in three major modules (see Fig. 1). The mainframe contains the logic, memory, and I/O cards and the power supply module. The display monitor contains the CRT, the sweep electronics, and the fan when required. The keyboard houses the keyswitches and associated electronics. Each of these major modules is quickly and easily removable and detachable.

The display monitor and mainframe are attached by two slide-apart hinges and are fastened in the closed or operating position by two tamper-resistant spring catches. The display monitor is held in the open position by a snap-action top prop to facilitate servicing and configuration. Two small cables connect the two assemblies and are quickly removable by disconnecting two slide-apart connectors. The safety shield, attached by quick-disconnect dart fasteners to the display monitor, also acts as a logic card retainer when the assembly is in the operating or closed position.

The keyboard is a separate entity that can be placed by the user in a convenient location. It is attached to the mainframe by means of a hooded edge connector and an I/O card.

All three major modules are housed in structural foam plastic (see box, next page). It has outstanding impact, flexural, compressive, and tensile strength and is one of the few molded plastic materials that has a self-extinguishing flammability rating. In addition, all mounting and printed-circuit guide detail is molded in, minimizing the total number of parts.

Design Features

Significant features of the packaging system are:

- *Pop-in/pop-out modularity.* All modules are removable without tools. A simple key unlocks the tamper-resistant spring catch, making the logic boards easily removable. The power supply safety cover and power supply are removable by means of quick-disconnect snap fasteners. The monitor board is removable by means of snap fasteners identical to those in the power supply. All cables are removable by disconnecting slide-apart connectors. All eighteen modules can be removed and replaced in less than ten minutes using no tools except the key that opens the box.
- *Single-level modularity.* All modules are removable without removing other modules. The three major modules help ensure that modules are not buried under other assemblies.
- *Pop-in expandability.* All options or known future options have a designated location, allocated space, and planned implementation. Mounting bosses are molded in and die inserts have been implemented. The minimum system consists of a nine-card backplane and no fan. Thus the minimum system user is not burdened by unnecessary overhead. The backplane may be expanded with a five-connector backplane or replaced with a single fifteen-connector backplane. Vent holes in the mainframe, monitor housing, monitor housing side panels, and monitor board allow the minimum system to operate without a fan with less than 10°C average air temperature rise. The fan is added when the tenth logic, memory, or I/O card is added. The fan cable plugs into a mating connector on the power supply card.

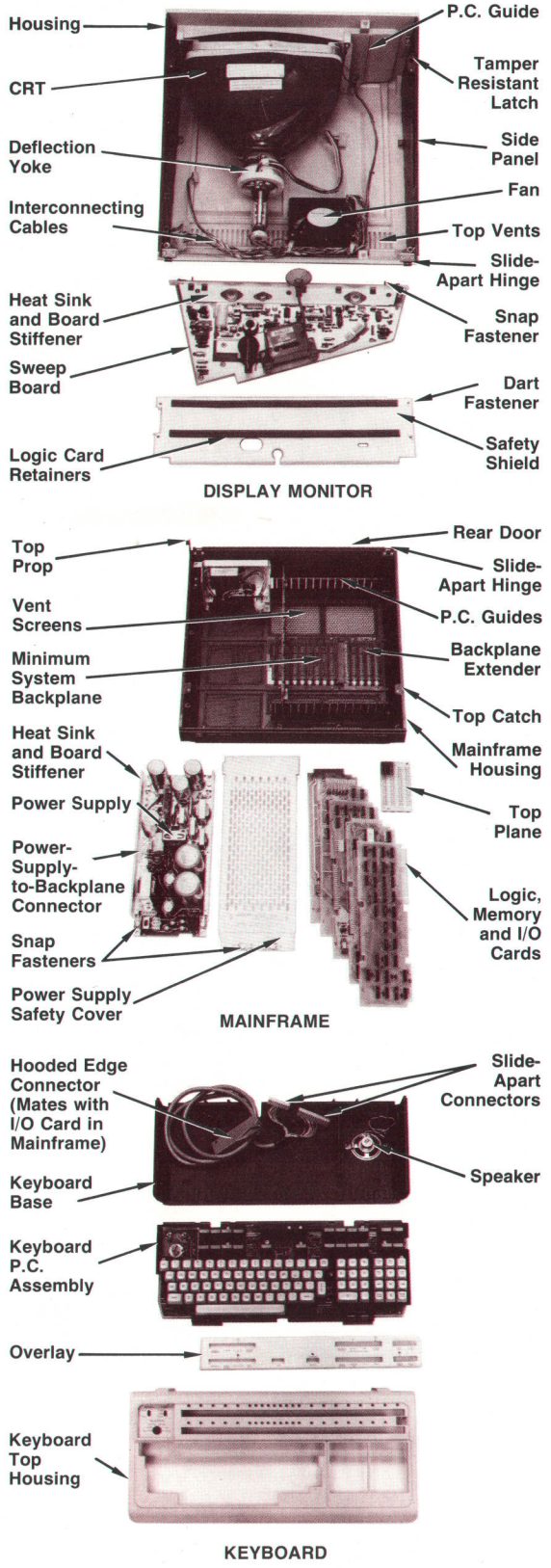


Fig. 1. *The 2640A Terminal is designed with pop in/pop-out modularity. The only tool required to replace a module is a key to get inside. Any module can be replaced in two minutes.*

Designing with Engineering Foam Plastics

With any new product, one of the most useful tools in the early stages of design is a mockup or model of some type. In the case of the 2640A, it was decided to have a precision wood model constructed. This model was accurate within a few thousandths of an inch, and served as the test bed for the power supply, the printed circuit boards, and the CRT mounting design. It also was used to run the initial temperature tests using dummy-loaded PC boards. The housing was then easily modified to perfect the final venting system. Later the model also served as an aid to the mold makers by helping them visualize how the final product should look.

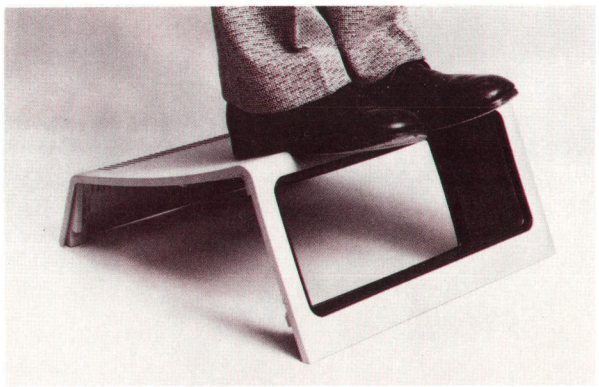
Several methods for producing the housing were considered. Among these were die casting, side-frame type construction, sheet molding, and structural foam. Only structural foam appeared to satisfy most of our design requirements.

From a design standpoint, this material is particularly attractive. Because of the internal foaming action and consequent lower material density, maintaining a constant-thickness wall section throughout the part is not so critical as it would be with other molding techniques. Transitions from thin walls to large thick bosses and ribs showed no evidence of sink marks. Although this is a distinct advantage it should be kept in mind that molding time is directly proportional to wall thickness in a ratio of approximately 1 min/0.5 cm. This caused some concern in the design of the CRT display section. A heavy 3-cm-thick wall above the display opening seemed almost a necessity to maintain the clean external appearance of the instrument. Because of the strength and flexibility of the material, a severe undercut that eliminated the excess material on the inside of the housing was possible. The undercut area has a large radius and the part is flexed and rolled off the core of the mold.

The foam material was also particularly adaptable to the PC board guide arrangement in the lower half of the housing. Two rows of card guides 7.6 cm high × 0.6 cm thick × 23 cm long are integrally molded into the base. Each row contains fifteen mounting slots located on 1.6-cm centers. It was decided that foam was the only practical way to obtain a detail such as this. Since the foam is non-conductive, insulating the PC boards from the guides and the housing required no consideration. The molded parts need no secondary finishing operations other than paint and installation of threaded inserts.

The outstanding strength (see photo), moldability, and design freedom offered by structural foam makes it the ideal material for applications such as the 2640A terminal.

Jerome Keever

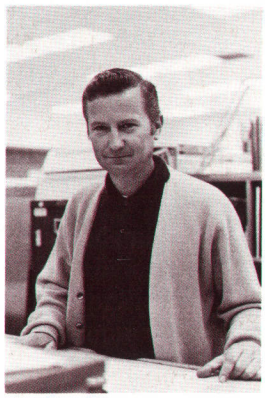


- *Serviceability.* Our MTTR (mean time to repair) objective was 15 minutes. It has been met primarily by way of the pop-in/pop-out/single-level modularity. In addition, all functional modules are self-contained and separately testable. Access, removal, and replacement time for any single module is less than two minutes.
- *Manufacturability.* The modularity and serviceability features also reduce manufacturing costs. The short time to remove, replace, and test any item is helpful in manufacturing as well as in service. The use of multifunction parts also reduces manufacturing costs. Heat sinks on the power supply and monitor are used as board stiffeners and for fastener mounting. The foam plastic housings include mounting bosses, printed-circuit guides, cooling vents, structural members, and latching detail. Logic cards are automatically held in by a safety shield. The rear door holds in I/O connectors. The keyboard housing clamps the keyboard printed circuit card in place, holds the speaker and cable clamp, and provides a bezel or shroud for the keyswitches.
- *Functional.* Proper viewing angle of display, proper keyboard height and slope, convenient position of keyswitches, and easy I/O cable access are all designed into the 2640A. Durability and reliability are enhanced by meeting HP class B environmental specifications.
- *Safety.* The materials, their application, and the overall configuration meet UL, CSA, IEC, HP and common-sense safety standards.

These features add up to cost savings to the user as a result of lower manufacturing cost and therefore lower price, lower service costs, and the value of paying for only what is needed. Also, pop-in expandability ensures that future needs can be met at minimum cost with clean and simple modifications.

Acknowledgments

Roger Lee contributed the industrial design and human engineering aspects. Jerry Keever contributed the mechanical design and detail design of the mainframe and top sections. Dave DeMoss contributed the product design of the keyboard. Special acknowledgment to Bob O'Keefe for his efforts in keeping our documentation package intact and complete.



Robert B. Pierce

Bob Pierce was project manager for the 2640A monitor, power supply, and packaging. An 18-year veteran at HP, Bob has served as OEM mechanical peripherals manager, project manager, mechanical design manager, design services manager, product designer, and packaging designer. He's a 1957 graduate of California State Polytechnic College (San Luis Obispo); his BS degree is in mechanical engineering. Originally from Atascadero, California, Bob now lives in Palo Alto. He's married, has four children, and his interests include golf, bowling, camping, fishing, and photography.

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