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# Universal Counter Resolves Picoseconds in Time Interval Measurements

*A new triggered phase-locked oscillator and a dual vernier interpolation scheme provide 20-picosecond resolution without averaging. Microprocessor architecture adds flexibility and processing power.*

**by David C. Chu, Mark S. Allen, and Allen S. Foster**

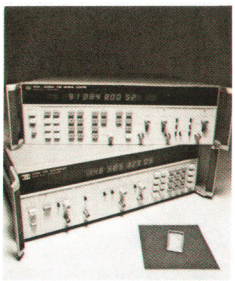
THERE WAS A TIME when the typical precision single-shot time interval measurement was made by a nuclear physicist working with transient subatomic particles. Today, single-shot time measurements are needed in circumstances that are not so esoteric. To measure, for example, the jitter in the period of a pulse train, the frequency of a short RF burst, the frequency drift of an oscillator immediately after turn-on, or the best and worst-case delays of a circuit, or to detect phantom glitches in a regular pulse train, single-shot time measurements are necessary, for in each case, the time information must be extracted precisely without the benefit of averaging. Single-shot measurement is also used in measurements of repetitive signals where averaging is not practical.* For example, the oscilloscope trace of a fast pulse that occurs at a low rate may be too dim for viewing on a standard oscilloscope, and measurement by time interval averaging[1] could take too long.

Model 5370A Universal Time Interval Counter is designed with many such applications in mind. It has a single-shot time interval resolution of 20 picoseconds and typical internal rms jitter of 35 ps, far better than any previously available instrument. This powerful measurement capability is augmented by sophisticated architecture. Flexible arming controls make it possible to extract time intervals from streams of input events, and internal processing converts raw time data to more useful information.

Model 5370A (Fig. 1) measures time intervals from −10 seconds to +10 seconds with 100-picosecond accuracy. It also measures period and frequency up to 100 MHz, giving 11-digit resolution for a one-second measurement time. The exceptional 20-ps single-shot time interval resolution is achieved by means of a new triggered phase-locked oscillator and a digital dual vernier interpolation scheme that eliminates the ±1-count uncertainty inherent in electronic counters. A microprocessor makes the technique economically feasible and adds features such as statistical computations for characterizing jitter. Other new features are the positive and negative time interval capability, useful for differential measurements, display of trigger levels, and automatic calibration of systematic errors. Programmability via the HP-IB (IEEE 488-1975, ANSI MC1.1) is standard.

Model 5370A is expected to find applications in

*It should be noted that the term "single-shot" may be misleading. The single event from which timing information is extracted is seldom isolated but one among a stream in most applications.



**Cover:** *Model 5359A Time Synthesizer (bottom) and Model 5370A Universal Time Interval Counter (top) are shown with the invention that makes their low jitter and high resolution possible. The triggered phase-locked oscillator (foreground) provides a means of synchronizing a stable frequency reference to randomly occurring pulses without losing any stability.*

**In this Issue:**


**Fig. 1.** *Model 5370A Universal Time Interval Counter measures time intervals from −10 to +10 seconds with 20-ps resolution in single-shot measurements. It can compute the mean, standard deviation, maximum, and minimum of repetitive time intervals. It measures frequency to 100 MHz, giving 11-digit resolution in one second. HP-IB interface and remote programmability are standard features.*

accurate component testing, radar and laser ranging systems, nuclear systems, digital communications, and calibration.

### Dual Vernier Interpolation

The traditional method of measuring time is by counting cycles of a time base clock. The unavoidable quantization error of ±1 count is usually larger than the jitter of many circuits to be measured, even for a very high-frequency clock (e.g., 2 ns for a 500-MHz clock). To achieve subnanosecond precision, interpolation between clock pulses is necessary.

The 5370A uses a dual vernier method to interpolate within the 5-ns period of a 200-MHz time base clock. In this method of time interval measurement, the start and stop pulses, which may be totally unsynchronized with the 200-MHz time base clock, start the oscillations of two separate oscillators. These oscillators both have a period of precisely $5\times257/256 = 5.01953$ ns and are phase-coherent with the start and stop pulses, respectively. The outputs of these oscillators are mixed with the 200-MHz time base clock and the phase crossover points (coincidences) between the oscillators and the time base are detected. As Fig. 2 shows, the number of start oscillator pulses up to start coincidence is counted as $N_1$, the number of stop oscillator pulses up to stop coincidence is $N_2$, and the number of 200-MHz clock pulses between the two coincidences is counted as $N_0$. The unknown time interval is $T_x$.

The time interval AB in Fig. 2 can be expressed in two different ways, which must be equal:

$$N_1\times(5.01953\text{ ns})+N_0\times(5\text{ ns}) = T_x+N_2\times(5.01953\text{ ns})$$

Thus the unknown time interval $T_x$ is given by:

$$T_x = 5N_0 + 5.01953(N_1 - N_2)\text{ ns}$$

Assigning a negative sign to $N_0$ whenever the stop coincidence precedes the start coincidence makes this equation valid under all conditions. The start and stop pulses need not be synchronous with the time base, nor must they arrive in a fixed order. A negative sign will be generated automatically for $T_x$ if the stop pulse arrives ahead of the start pulse.

Notice that the start coincidence signal must simultaneously terminate the $N_1$ count and initiate the $N_0$ count without ambiguity. Fortunately, the coincidence signal appears only at phase crossovers and is therefore synchronous with both pulse trains, so gating to generate the bursts can be accomplished without ambiguity. The same goes for the stop coincidence.

As an added benefit, since only the difference $(N_1 - N_2)$ appears in the computation, systematic offsets in these counts are self-cancelling. This property allows additional freedom in the design of the vernier oscillators as long as the start and stop channels are treated the same way.

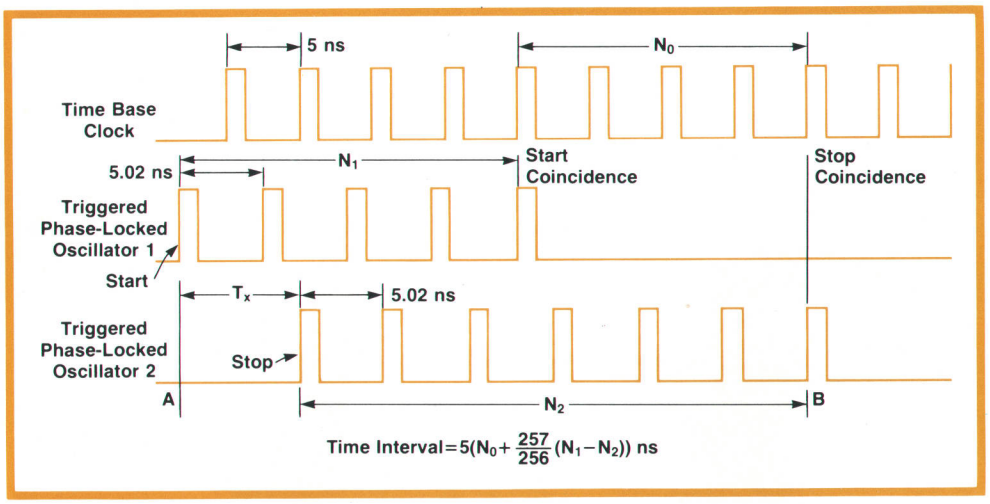



**Fig. 2.** *Dual vernier method interpolates within the 5-ns period of the 5370A's 200-MHz time-base clock to obtain 20-ps resolution. The start and stop pulses start the oscillations of two triggered phase-locked oscillators. Coincidences of the oscillator waveforms with the time base clock define the counts $N_0$, $N_1$, and $N_2$, as shown. The unknown time interval is computed from these counts.*

There are some difficulties in using the dual vernier method. The most fundamental is the extremely stringent requirement on the stability of the oscillators, particularly the triggered vernier oscillators. To interpolate by a factor of 256, as in the 5370A, requires a timing error of less than 1/256 of one period in a maximum of 256 periods, or 0.0015% absolute stability under changing environmental conditions. Furthermore, detection of the coincidences between the vernier and the main clocks had to be done with timing discrimination better than 20 ps. These problems are solved by the triggered phase-locked oscillators,[2] also known as phase-shiftable, phase-lockable oscillators, which were developed especially for this counter and related instruments (see box, page 8). These oscillators eliminate long-term drift and post-trigger short-term drift, and generate the necessary vernier burst and coincidence signal for main time base gating.

Two triggered phase-locked oscillators are used in the 5370A, as shown in the measurement section block diagram, Fig. 3. Reference 200 MHz is derived from an internal 10-MHz time base oscillator or from an external 5-MHz or 10-MHz standard. Input events are conditioned and triggered by matched 500-MHz-bandwidth input amplifiers with digitally displayable trigger levels. An arming control selects the correct time interval for triggering the vernier oscillators. The vernier bursts $N_1$ and $N_2$ are counted and data made available through the microprocessor bus. The start and stop coincidences (CO1 and CO2) are used to gate the 200-MHz clock to generate the $N_0$ count, which is also accessible to the bus. The arming control circuit also counts the number of input events during time interval holdoff and during frequency measurements.

### Time Interval Measurements

The ability to measure both positive and negative time intervals presents an ambiguity problem when the time intervals occur repetitively. To illustrate, suppose a 30-ns time interval is fed to the counter every 100 ns as shown in Fig. 4. Depending upon exactly when arming occurs, there are two possible time interval measurements, 30 ns and −70 ns.

If an external arming signal is available, this signal can be used on the EXTERNAL input of the 5370A, and the appropriate time interval will be measured without ambiguity. In many applications, a separate arming signal is not available, and arming is done internally by the start and stop events themselves. The ambiguity problem must then be resolved to avoid random fluctuation between the two possible readings.

A simple way to resolve this ambiguity is to imitate a conventional counter and require that the start event come before the stop event. The 5370A offers this feature as +TI ONLY mode. The +TI ONLY arming scheme is used to make simple time interval measurements as well as frequency and period measurements. The major disadvantage to requiring that the start event come first is that it takes a finite time for the information about the occurrence of the start event to reach the stop channel. In +TI ONLY the 5370A will measure any time interval less than ten nanoseconds.

### Hysteresis Arming

To eliminate this disadvantage, and to allow measurement of both positive and negative time intervals, special circuitry was added to keep track of the start and stop channel events. Essentially, this adds hysteresis to the time intervals being measured so that once either the positive or the negative time interval has been selected, the 5370A tracks this interval until the signals drift out of range or the user selects otherwise. For example, to measure the 30-ns or −70-ns time intervals depicted in Fig. 4, the user selects ±TI, and the 5370A chooses either 30 ns or −70 ns. To select the other answer, the user presses the front-

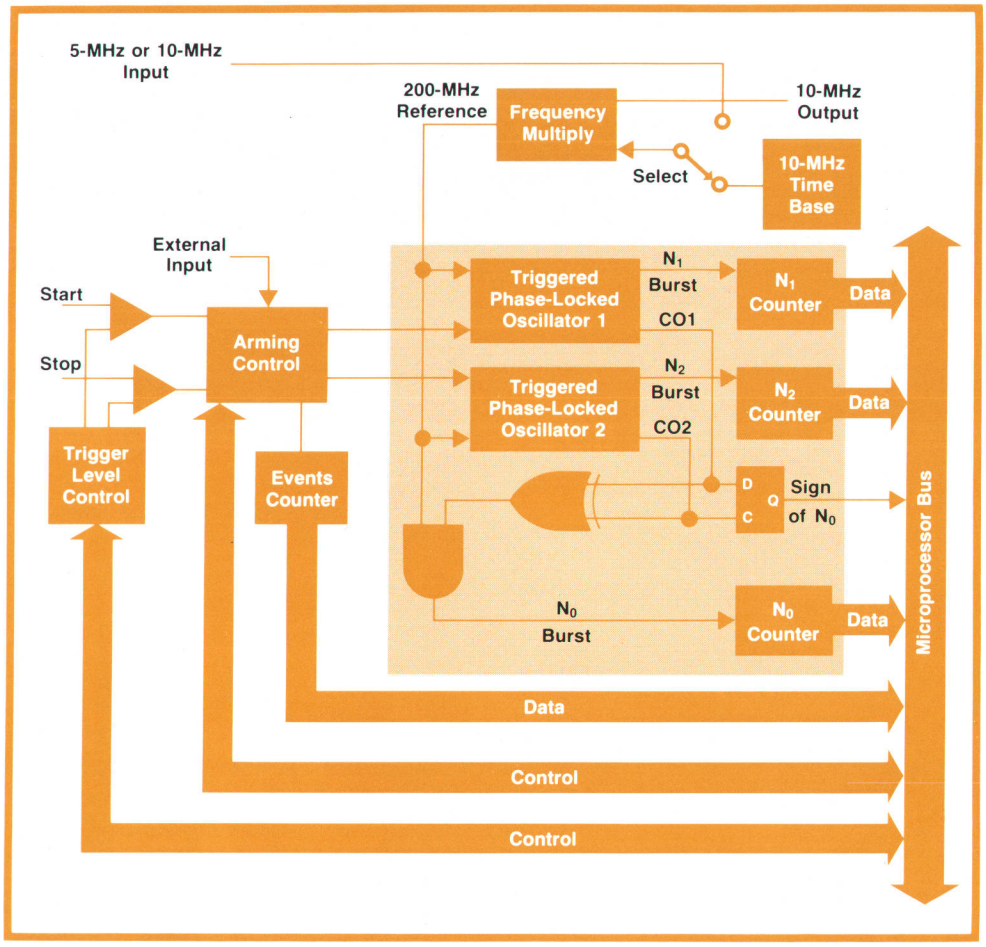



**Fig. 3.** *Measurement section of the 5370A Counter. The two triggered phase-locked oscillators feed two vernier-burst counters. Counts go to the microprocessor, which computes the unknown time interval.*

panel PERIOD COMPLMNT button.

To understand how the hysteresis circuitry works, refer again to Fig. 4. In ±TI, both channels are armed simultaneously. If the arm signal arrives at B, the time interval measured will be from E to C. Similarly, if the arming signal arrives at D, the time interval measured will be B to E. To control the arming, it is only necessary to select one input channel or the other as the source of the arming signal.

Fig. 5 shows the hysteresis circuitry that controls selection of the arming source. The left portion is a rudimentary phase detector that generates a logic low if the start event came before the stop event, and a logic high if the stop event came first. The right portion of the circuit allows useful control of the phase detector's output. The phase detector locks onto and follows the input signals, and the user control allows selection of the positive or negative time interval by changing the sense of the phase detector's output.

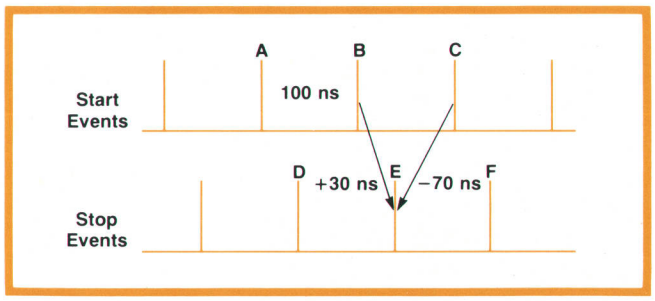



**Fig. 4.** *Because the 5370A can measure both positive and negative intervals, repetitive time intervals present an ambiguity problem. For example, if a 30-ns time interval is fed to the counter every 100 ns, the result can be 30 ns or −70 ns, depending on when arming occurs. Hysteresis arming keeps the reading from fluctuating between the two values.*

When the time interval is zero, the two pulse trains are in phase, and it does not matter which channel is selected as the arming source because the start and stop events are simultaneous. The phase detector itself is unable to determine exactly which event came first. As the pulse trains drift in either direction, the phase detector recognizes this and chooses the correct source. The result is a consistent time interval reading from minus one period to plus one period going smoothly through zero. The reading will not jump between periods within this range.

### Frequency and Period Measurements

Frequency and period are measured by the 5370A Counter by measuring the time interval of a number of events. Frequency f and period T are then computed internally as follows:

$$f = \frac{\text{Number of events}}{\text{Time Interval}}$$

$$T = \frac{\text{Time Interval}}{\text{Number of events}}$$

The time interval is measured to a typical rms resolution of 35 ps (100 ps maximum) whereas the number of events is measured without ambiguity.

The gate time for counting the events is either generated internally or externally supplied. The typical fractional rms frequency resolution is 35 ps divided by the gate time. For example, a 350-$\mu$s gate will yield an rms resolution of 1 part in $10^7$, or 1-Hz resolution for a 10-MHz signal, or 10-Hz resolution for a 100-MHz signal. Such high resolution with a short gate is highly desirable for pulsed RF measurements, since the long gate times needed by some counters to obtain equivalent resolution may be longer than the RF pulses.

Used in conjunction with a precision time delay generator such as the 5359A Time Synthesizer (see article, page 12) the 5370A can be used efficiently for frequency profiling, as shown in Fig. 6. A pulsed excitation source causes a step change in the input to a voltage-controlled oscillator (VCO). The time synthesizer is triggered by the leading edge of the excitation pulse and generates a delayed window that is used as an external measurement gate for the counter. By varying the delay, the VCO output frequency at different locations relative to the leading edge of the excitation gate can be sampled.

A novel feature of the 5370A Counter is that the number of events within the gate in a frequency or period measurement can be displayed by simply pressing the DSP EVTS switch. This feature is available in both internally and externally gated frequency and period measurements, as well as in time interval measurements with holdoff. In the latter, stop channel events are ignored until the end of the external gate. By applying the same signal to the start and stop channels and using an external gate one can simultaneously measure both the number of events and the time frame they occupy.

By changing the width of the delayed gate in Fig. 6, a profile of time versus events can be obtained even for a complicated signal such as a fast-switching VCO waveform. For convenience, signal conditioning is provided for the 5370A's external input channel as well as for the start and stop channels.

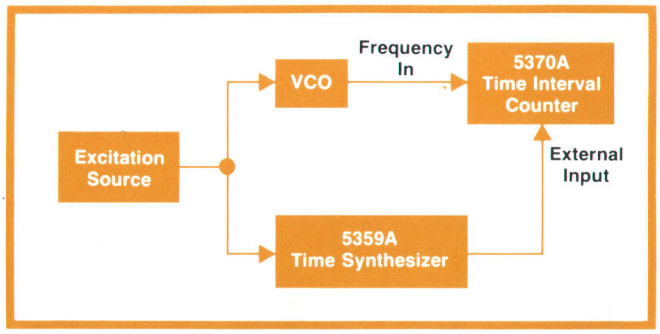



**Fig. 6.** *With the 5359A Time Synthesizer generating precision time delays and gate times, the 5370A can be efficiently used for frequency profiling. Here a pulsed excitation source causes a step change in the input to a voltage-controlled oscillator. The 5359A delay is varied to obtain a profile of the VCO frequency versus time following the change.*

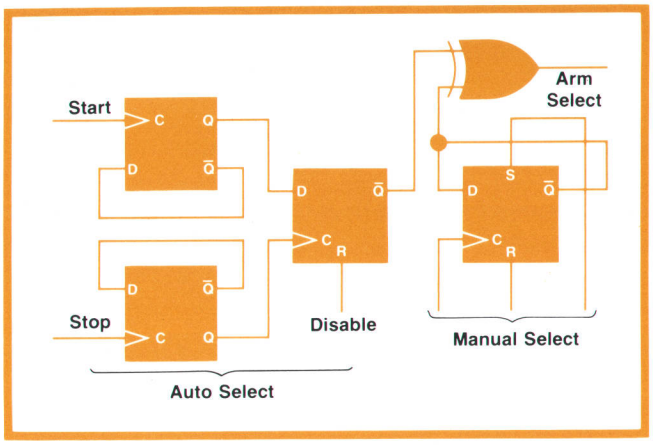



**Fig. 5.** *Hysteresis arming circuit consists of a rudimentary phase detector (left) that indicates whether the start event or the stop event occurred first, and a user control section (right) that allows the user to select either of the two possible time-interval readings. The 5370A will track one reading until the user selects the other.*

### Microprocessing and Digital Hardware

A 6800 microprocessor in the 5370A performs the calculations for the basic time interval measurements and for additional features like frequency measurements and statistics. It also provides control of the instrument via the front-panel pushbuttons or the standard HP-IB interface, and assists in instrument service in both factory and field.

The processor section (see Fig. 7) is modular, with each board functioning independently. These boards plug into a backplane section consisting of eight bidirectional data lines, 16 address lines, and ten control lines. Each board does its own address decoding using memory mapped input/output, allowing flexibility in design and implementation. The processor board contains a clock generator, 384 bytes of RAM (read/write memory), and data and address buffers. Other buffers and 8K bytes of ROM (read-only memory) for program storage are housed in the ROM assembly. Strobing for the 16-digit display is provided by the display interface board assembly. The same board provides logic for scanning the front-

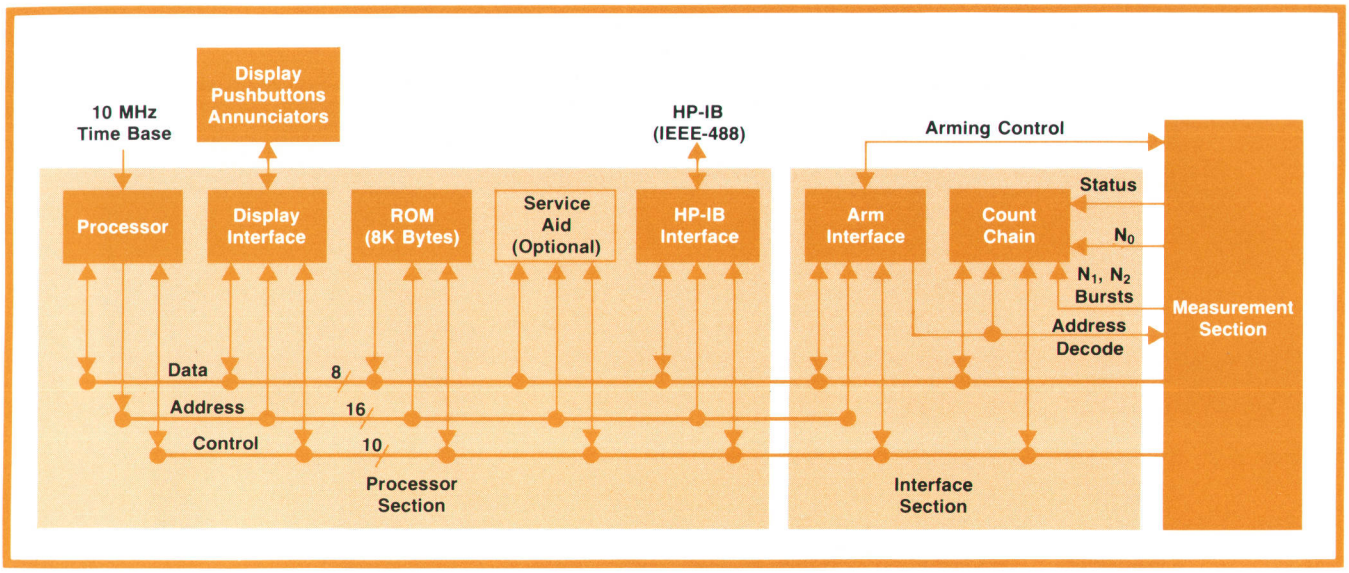



**Fig. 7.** *5370A processor section is modular. Provision is made for self test, troubleshooting by signature analysis, and use of the HP-IB for testing. An optional service accessory package includes a service aid board that provides access to many of these features.*

panel switches to notify the processor of changes in status.

The pulse bursts $N_1$, $N_2$, $N_0$ and events from the measurement section are counted by the count chain assembly up to 16 bits. Software counters are used to extend the count range up to 40 bits for longer measurements. When the instrument is under remote control, two digital-to-analog converters (DACs) are used to set the trigger levels of the input amplifiers. The same DACs are used with software control to measure the trigger levels set from the front-panel when the instrument is under local control.

Programmability via the HP interface bus (IEEE 488-1975, ANSI MC1.1) is standard. All front-panel functions except input attenuation, coupling, and impedance are programmable. Arbitrary sample size, teach/learn, and fast data dump modes are available. The HP-IB interface assembly handles most HP-IB protocol with minimum processor intervention. This reduces processor overhead and allows the processor to do internal chores during the measurement cycle.

### Service

Because microprocessors are relatively new to instrument design, serviceability was one of the main design concerns. Internal diagnostics are provided. Upon power-up, a checksum test is performed on the ROM to check data integrity and a memory test is done on RAM to verify function. A test failure results in a front-panel display that designates which ROM or RAM has failed. Other tests are performed on the I/O system and a phase lock test is done on the measurement section. Hardware and software are provided for troubleshooting by signature analysis,[3] and the HP-IB can be used to enter diagnostic routines and perform additional tests.

These service features are used in a number of ways. A special extender board is provided with an optional service accessory package. It has switches that allow a board to be isolated from the processor bus to aid in finding stuck data, address, or control bus lines. The processor board contains switches that disable the data buffers and RAM and provide a microprocessor instruction to allow free running of the address bus to facilitate signature analysis. Indicators are provided for processor clock loss, phase-lock failure, and the status of various functions on the HP-IB interface. Switches are provided on the arm interface to open various loops for signature analysis and to assist in setting up preset conditions for troubleshooting the measurement section.

The service accessory package includes a service aid board that has switches to initialize the processor, to allow test of the interrupt system, and to place the processor in a special interface mode that allows direct HP-IB control of any register, memory location, or I/O port. The service aid board also has a breakpoint register that can be used to set program interrupts to aid in functional testing. There are also two DACs for displaying the lower eight bits of the address bus on one axis of an ordinary oscilloscope and the upper eight bits on the other axis to provide a "map" presentation that, to someone familiar with it, gives an instant indication of the behavior of the instrument.

### Statistics

One use of the computational power of the processor is to generate statistical parameters from samples

# The Triggered Phase-Locked Oscillator

**by David C. Chu**

*Problem:* design an oscillator that can be phase-synchronized with a random trigger pulse. The frequency of oscillation must be as accurate as that of a frequency reference.

Usually these two requirements are contradictory. Phase locking for frequency accuracy typically destroys prior phase relationships, and for this reason, phase-triggerable oscillators generally run open-loop, unable to take advantage of a stable reference frequency source.

Our approach to this problem is to run the triggered oscillator continuously while locked to the reference by the ratio N/(N+1) in frequency. The trigger pulse is used only for phase-shifting the oscillator. The random phase shift of the oscillator from being triggered manifests itself in the beat frequency, N times lower in frequency, but by the same angle. This new phase of the beat frequency is matched digitally by one of N possible phases of a divide-by-N counter. Phase locking is then resumed, locking the beat frequency to its new phase, and by correspondence, the oscillator to its new phase.

### Pre-Trigger Operation

The basic oscillator circuit is shown in black in Fig. 1. The triggered oscillator consists of one inverting gate with feedback through a delay $\tau_2$. Its output, at frequency f, is mixed with the reference frequency $f_0$ to produce a beat frequency $f_0-f$. At the same time, the oscillator frequency is divided by N to produce a signal of frequency f/N. These two signals are inverted and compared by a frequency/phase detector that develops a phase error signal based on differences in the times of occurrence of positive transitions. The error signal is integrated and filtered and used to tune the oscillator via the varactor diode, completing the phase-locked loop.

In this quiescent locked condition, the positive transition of the mixer output, signifying oscillator/reference phase crossover, occurs at the same time as the positive transition of the divider, signifying counter turnover. This condition must also be met after triggering when oscillations will be at a random new phase determined by the trigger.

By equating the frequency of both phase detector inputs, f/N and $f_0-f$, the frequency f can be computed to be

$$f = \frac{N}{N+1} f_0 .$$

### Trigger and Relock

A random trigger pulse sets the lockout flip-flop. The difference in delay $\tau_1$ between the Q and $\overline{Q}$ transitions at the input to the NOR gate generates a pulse of width $\tau_1 (>\tau_2)$ that stops the oscillation within $\tau_2$ and restarts the oscillation precisely $\tau_1$ later. The new phase is therefore completely synchronized to the trigger pulse and not at all to the old oscillation. Signal S rises in response to the $\overline{Q}$ transition of the lockout flip-flop. This inhibits both inputs to the frequency/phase detector and resets the counter. After a delay of $\tau_3$ (not critical), the coincident flip-flop is receptive to a positive transition from the mixer. One such transition will come within the beat period $(N+1)/f_0$ to clock the coincident flip-flop. Signal S is thereby removed, enabling both inputs to the phase detector and relocking the loop.

Notice that the removal of S allows the counter to begin counting from count zero. The condition before triggering is now reestablished, that is, the zeroth count is matched in time to the

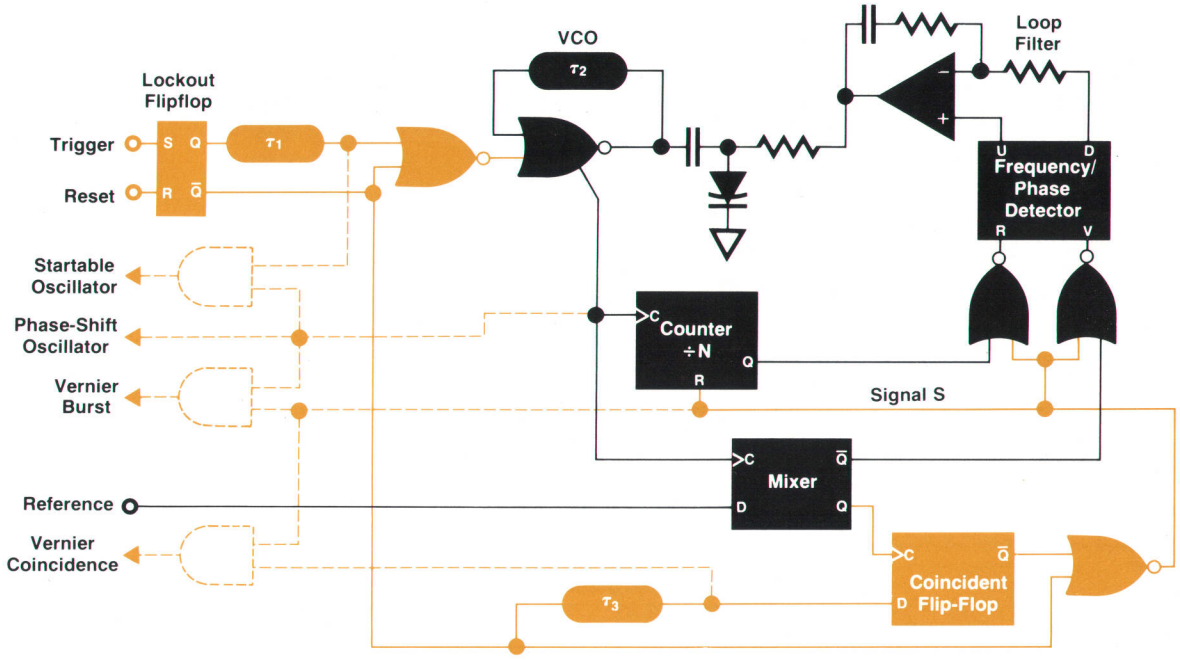



**Fig. 1.** *Simplified block diagram of a triggered phase-locked oscillator with interpolation factor N. The black components are active during quiescent (pre-trigger) conditions. Solid-color components become active when the oscillator is triggered. Dashed gates show how the oscillator can be configured for different applications.*

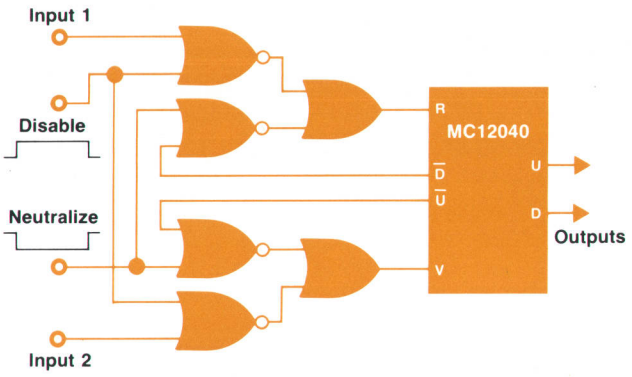



**Fig. 2.** *The phase detector is disabled for a short period after a trigger. Aided by feedback, a neutralizing pulse guarantees the parity of the inputs so the phase detector does not signal a gross phase error during this period.*

itself to lock to the new beat frequency. By one-to-one correspondence, this also locks the new phase of the triggered oscillator. The loop may now be reset to receive another trigger pulse if desired.

A simple check for correct loop operation is to observe the tuning voltage. Absolutely nothing should happen throughout the trigger and relock sequence.

Notice that except for a brief interruption of duration $\tau_1$, the oscillator is always oscillating, before and after triggering. This greatly reduces post-trigger frequency drift compared with an oscillator that is at rest before triggering.

### Implementation Considerations

The delay $\tau_1$ (approximately 10 ns) is generated by a coaxial transmission line to minimize transition time after the delay. Variations of $\tau_1$ with temperature are self-cancelling in the 5370A because identical lines are used for the start and stop channels. Delay $\tau_2$ and the inverting oscillator gate and buffers are implemented as a hybrid thin-film circuit on a ceramic substrate. The frequency tuning range is about ±1% of nominal corresponding to the circuit open-loop variations under changing environmental conditions. The delay $\tau_3$ is necessary to avoid clocking a possible initial mixer positive transition not related to phase crossover. The actual value is not critical provided it is sufficient. We used lumped LC elements.

Inputs to the phase detector, even under locked conditions, are never exactly in phase. This phase error can be minimized but not totally eliminated. Should the disabling of the phase detector occur at the unfortunate though narrow time between input arrivals, a pulse is generated at one side but not the other, causing detection of a gross phase error. The circuit of Fig. 2 employs feedback from the detector outputs to assure neutrality of the phase detector by generating an extra pulse to guarantee parity of the inputs during disabling.

The mixer output beat frequency is unsigned, that is, f may be higher or lower than $f_0$. The loop is regenerative and therefore unstable at the wrong sideband. To assure start-up on the correct sideband, a lock fix signal disables the mixer for a short period. The loop then forces the oscillator to come up from the low-frequency side toward the final value when the mixer is reenabled.

### Integrated Circuits

The triggered oscillator hybrid circuit consists of active circuitry on a ceramic substrate in a hermetic hybrid package with a heat sink stud on the bottom (see Fig. 3). The heat sink stud also provides a high-integrity electrical ground connection to

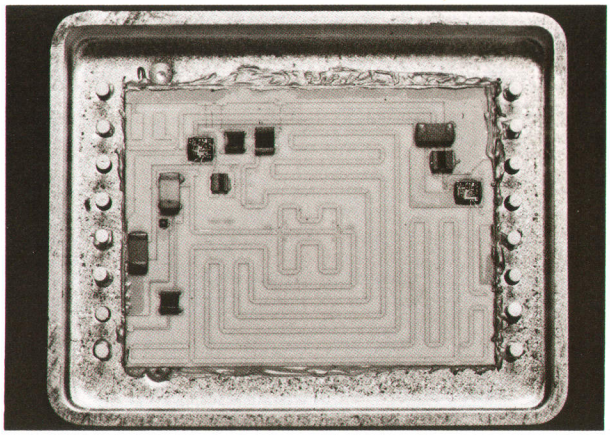


**Fig. 3.** *Triggered oscillator hybrid circuit is on a ceramic substrate in a hermetic package. Most of the substrate is taken up by a delay line with multiple path bonding options to compensate for process variations. The two ICs are HP 5-GHz-process bipolar circuits.*

the package. The 1.9×2.5-cm ceramic substrate is mostly delay line with the rest taken up by the active circuitry including chip resistors and capacitors. The delay line has multiple path bonding options to compensate for process variations.

Two HP 5-GHz-process bipolar integrated circuits are used, one as the oscillator and the other as an output buffer.[1] The significant contribution of the 5-GHz-process circuits is their small (300-picosecond) propagation delay. This is important because the nominal frequency of oscillation is determined by the delay around a feedback loop consisting of an inverting gate and an external delay line. The total delay is half the period of oscillation, which for a 200-MHz nominal frequency is 2.5 nanoseconds. Since the propagation delay through the gate varies with temperature more than the delay through the external delay line, it is important that the gate portion of the total delay be minimized. The 300-picosecond propagation delay of the 5-GHz process gate makes this goal achievable.

The 5-GHz circuits also provide higher short-term stability. This comes about for two reasons. First, trigger error caused by noise is reduced with very fast transitions. Second, since the external delay line is very stable, making the gate delay small compared to the line delay improves overall stability. The very fast circuits also decrease the memory effect during oscillator stop and restart, minimizing the time required and reducing any transient phenomena associated with this operation.

The mixer that detects the oscillator/reference phase crossover is an edge-triggered D-type master-slave flip-flop made with the 5-GHz process. It resolves 20 ps very easily.

### Applications

Oscillations prior to the arrival of the trigger can be screened from the user by gating with the lockout flip-flop. For time synthesis, such as by the 5359A Time Synthesizer (see article, page 12), this mode is used. For vernier interpolation in the 5370A Universal Time Interval Counter (see article, page 2), the burst is gated by the signal S. The coincidence signal (end of S) can be generated as shown.

Besides time interval generation and measurement, the oscillator can be used for indefinite duplication of single-shot time intervals, for accurate magnification of small time jitter to facilitate measurement, or as a triggerable frequency standard.

### Reference

1. D. DiPietro, "A 5-GHz $f_T$ Monolithic IC Process for High-Speed Digital Circuits," Proceedings of the 1975 IEEE Solid-State Circuits Conference, pp 118-119.

of high-resolution single-shot data. Small variations of the signal input that are large compared to the counter's own internal measurement jitter can be characterized with pushbutton ease. Time intervals can be processed at rates up to 3,000 measurements per second for a preselected sample size. Four statistical parameters of the sample—mean, standard deviation, maximum, and minimum—are available for display. For users with buffer memory and external computational power, the 5370A offers a computer dump mode in which unprocessed raw time interval data can be output at up to 8,000 points per second.

The four statistical parameters are computed as follows:

$$\text{MEAN} = t_o + \frac{1}{N}\sum_{i=1}^{N}(t_i - t_o)$$

$$\text{STD DEV} = \sqrt{\frac{1}{N-1}\left\{\sum_{i=1}^{N}(t_i - t_o)^2 - \frac{1}{N}\left[\sum_{i=1}^{N}(t_i - t_o)\right]^2\right\}}$$

$$\text{MAX} = t_o + (t_i - t_o) \text{ max of N readings}$$

$$\text{MIN} = t_o + (t_i - t_o) \text{ min of N readings}$$

where N is the sample size selected and $t_o$ is an initial measurement. Notice that $t_o$ is cancelled out mathematically in each case and does not, ideally, affect the final results. But the use of $t_o$, particularly if $t_o$ is typical of all $t_i$, greatly minimizes truncation errors in computation, since all operations are done with only the differences $(t_i - t_o)$. In the 5370A, $(t_i - t_o)^2$ is rounded off to 16 bits.

Regardless of the sample size, only five memory registers are needed to generate the four statistical parameters. These registers hold $t_o$, $\sum(t_i - t_o)^2$, $\sum(t_i - t_o)$, max $(t_i - t_o)$, and min $(t_i - t_o)$.

### User-Defined Time Reference and Self-Characterization of Jitter

In subnanosecond measurements, the definition of zero time is a problem. The slightest mismatch in probes, cable lengths, or input amplifiers of the start and stop channels can show up as a systematic error in the measurement. To calibrate out such errors in the 5370A, the user simply sets up the same start and stop input conditioning, feeds the same signal to both channels, and measures the time interval with ±TI arming. Thus the same input transition triggers both the start channel and the stop channel. The time interval measured is the residual error of the whole system, probes and all. By pressing SET REF, the measurement value is stored, to be automatically subtracted from all future measurements. In effect, zero time reference is defined by the user.

The SET REF feature is also useful in measurements where changes, and not absolute values, are of interest. By zeroing out the initial value, any change can be read directly later.

Pressing STD DEV causes the standard deviation of this "common" time interval to be displayed. The value is the rms measurement jitter of the instrument itself and is characteristic of the specific instrument. With fast pulses (10 ns rise time or less), trigger error is negligible, and the jitter is typically less than 35 ps.


### Acknowledgments

The authors wish to acknowledge the other two principal designers of the 5370A: Leonard Dickstein, time base, power supply, hybrid circuit development, and production engineering, and Carl Spalding, mechanical engineering. The project also benefitted from the software development tools of Tom Coates and Luiz Peregrino, the high-frequency ICs of David DiPietro, the industrial design efforts of Bernie Barke, the marketing and service support of Jim McNeish and Randy Goodner, the technical and managerial assistance of Keith Ferguson and Jim Sorden, and the documentation of Bill Anson. Special thanks go to Charlie Trimble who supported the work at its risky infant stages and to Jim Horner who firmly sustained that support.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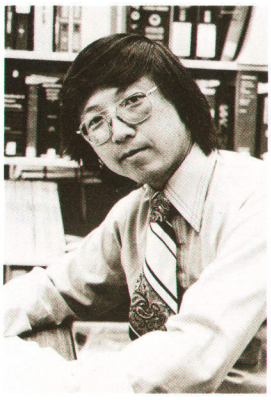



**David C. Chu**

David Chu is project leader for the 5370A Counter and is the inventor of the triggered phase-locked oscillator. He's been with HP off and on since 1962, serving as design engineer, consultant, and project manager, working mostly on top-of-the line counters and plug-ins and on mathematical modeling and statistical analysis. A Phi Beta Kappa BSEE graduate of the University of California at Berkeley in 1961, Dave received his MSEE degree from Stanford University in 1962. After several years with HP, he went to Africa to serve as a professor of physics in Liberia, then returned to Stanford for his PhD degree, specializing in coherent optics. He's authored many papers on time and frequency measurements, computer holography, and related subjects and is responsible for many patents in the same areas. Dave lives in Woodside, California. His favorite summer sport is racing his El Toro sailboat, frequently upside down. In the winter, he limps around the lab with his latest skiing injury.

## Mark S. Allen

Mark Allen received his BS and Master of Engineering degrees from Harvey Mudd College in 1973 and 1974. He spent the summer of 1973 with HP working on pulsed RF measurements, then joined the company permanently the following year. He's done hardware and firmware design for the 5370A Counter and other microprocessor-based instruments, and software design for a 6800 development system. He is co-author of a paper on the relationship of IEEE standard 488 to microprocessors. Born in Los Angeles, Mark is married and lives in Saratoga, California. His interests include music, swimming, and sailing.

## Allen S. Foster

Al Foster was responsible for the digital architecture and design of the 5370A Time Interval Counter. With HP since 1963, he's designed high-precision crystal oscillators, the digital section of the 5340A Microwave Counter, and an automatic tester for the 5340A. Al was born in San Francisco and grew up in Marin County, California. He received his BSEE degree from the University of California at Berkeley in 1963 and his MSEE degree from Stanford University in 1971. In his spare time, he enjoys building television systems and restoring his eight-year-old Porsche 914-6. He's single and lives in San Jose, California.

# SPECIFICATIONS
## HP Model 5370A Universal Time Interval Counter

### Input Amplifiers

**SEPARATE INPUTS**
SENSITIVITY: 100 mV p-p, 35 mV rms sine wave times attenuator setting.
IMPEDANCE: Selectable 1 MΩ||30 pF or 50Ω nominal.
TRIGGER LEVEL: Adjustable from −1.3V to 0.5V with 10 mV displayed resolution.
TRIGGER SLOPE: Independent selection of + or − slope.
ATTENUATORS: ÷1 and ÷10 nominal.
DYNAMIC RANGE (preset):
50Ω ÷1 100 mV to 1V p-p pulse
÷10 1V to 7V p-p pulse
1 MΩ ÷1 100 mV to 1V p-p pulse
÷10 1V to 10V p-p pulse
Dynamic range for rms sine wave is one-third of the above values.
SIGNAL OPERATING RANGE:
50Ω ÷1 −2.5V to 1V
÷10 −7V to 7V
1MΩ ÷1 −2.5V to 1V
÷10 −25V to 10 V
COUPLING: ac or dc switch selectable.
MINIMUM PULSE WIDTH: 5 ns
MAXIMUM INPUT:
50Ω ÷1 ±7V dc
7V rms below 5 MHz
3.5V rms (+24 dBm) above 5 MHz
÷10 ±7V dc, 7V rms (+30 dBm)
1MΩ ÷1 ±350V dc
250V rms to 20 kHz decreasing to 3.5V rms above 5 MHz
÷10 ±350V
250V rms to 20 kHz decreasing to 35V rms above 5 MHz
**COMMON INPUT:** All specifications are the same as for separate operation with the following differences:
IMPEDANCE: 1 MΩ becomes 500 kΩ shunted by <60 pF. 50Ω same as in separate.
SENSITIVITY: (preset)
50Ω ÷1 200 mV p-p, 70 mV rms
÷10 2V p-p, 700 mV rms
1MΩ Same as in separate
DYNAMIC RANGE: (preset)
50Ω ÷1 200 mV to 2V p-p pulse
÷10 2V to 5V p-p pulse
1MΩ Same as in separate
MAXIMUM INPUT:
50Ω±5V dc or 5V rms
1 MΩ same as in separate
ATTENUATORS: Becomes ÷2 and ÷20 for 50Ω.

### Frequency and Period Measurements

**FREQUENCY RANGE:** 0 to 100 MHz
**PERIOD RANGE:** 10 ns to 10 seconds
**RESOLUTION:** $\frac{20\text{ ps}}{\text{gate time}}$
INTERNAL GATE TIME: 1 period, 0.01, 0.1, 1 second
**ACCURACY:** $\frac{100\text{ ps rms} \pm \text{trigger error}}{\text{gate time}} \pm \text{time base}$
**PERIOD/FREQUENCY STATISTICS:** (1-period gate only) mean, standard deviation, maximum, minimum
SAMPLE SIZE: 1, 100, 1000, 10,000, 100,000; 1 to 16,777,215 via HP-IB.
EXTERNAL GATE INPUT: 20 ns to 10 s/sample size

### Time Interval Measurements

**TIME INTERVAL RANGE:**
±Mode: −10 seconds to +10 seconds. +Only Mode: 10 ns to 10 seconds.
**TIME INTERVAL STATISTICS:** Mean, standard deviation, maximum, minimum.
**SAMPLE SIZE:** 1, 100, 1000, 10,000, 100,000; 1 to 16,777,215 via HP-IB.
**MINIMUM TIME BETWEEN MEASUREMENTS:** 330 μs
**RESOLUTION:** $\frac{\pm 20\text{ ps}}{\sqrt{\text{sample size}}} \pm 2\text{ ps}$
**ACCURACY:** Jitter ±1 ns systematic ± time base ± trigger error/$\sqrt{N}$. For time intervals greater than 10 ms the high-stability time base Option 001 is recommended.
**JITTER:** 35 ps rms typical, 100 ps rms maximum
**TRIGGER ERROR:** $\frac{\pm 2 \times \text{noise peak voltage}}{\text{Signal Slope V/μs}}$ μs
Trigger error due to input signal noise is usually the limiting factor in high resolution frequency measurements at low frequencies. If peak noise amplitude is greater than 10 mV, additional miscounting may occur. (This situation can arise when measuring high-level outputs of broadband synthesized signal sources.)

### General

**EXTERNAL GATE**
INPUT IMPEDANCE: 1 MΩ||10 pF nominal
SLOPE: Selectable + or −
LEVEL: Continuously adjustable −2V to +2V, preset 0V
MINIMUM PULSE WIDTH: 20 ns
EXTERNAL GATE RANGE: 20 ns to 10s/sample size
**TRIGGER OUTPUTS** (rear panel)
START: Edge going from 0 to −0.7V nominal into 50Ω in sync with the opening of the start channel.
STOP: 0 to −0.7V edge into 50Ω in sync with the closing of the stop channel.
**FREQUENCY STANDARD INPUT** (rear panel): 5 or 10 MHz >1.0V p-p into 1 kΩ. Maximum input 10V.
**FREQUENCY STANDARD OUTPUT** (rear panel)
10 MHz
1V p-p into 50Ω in sync with time base chosen (INT or EXT)
**DISPLAY:** 16 digits + sign, suppressed leading zeros
**DISPLAY RATE:** 10 ms to 5 s or hold
**OPERATING TEMPERATURE:** 0° to 50°C
**POWER REQUIREMENTS:** 200 VA; 100, 115/120, 220, 230/240 volts +5%, −10%.
**DIMENSIONS:** 133 mm H × 425 mm W × 457 mm D (16¾ × 5¼ × 18 in).
**WEIGHT:** 14.5 kg, 32 lb.
**TIME BASE:** Crystal frequency 10 MHz
STABILITY:
AGING RATE: $<3\times10^{-7}$ per month
SHORT TERM: $<2\times10^{-9}$ rms for 10 ms to 1s
TEMPERATURE: $<2\times10^{-6}$ 25°C to 35°C
$<5\times10^{-6}$ 0°C to 50°C
LINE VOLTAGE: $<1\times10^{-8}$, ±10% nominal
**OPTION 001:** HIGH-STABILITY TIME BASE (HP Model 10544A)
CRYSTAL FREQUENCY: 10 MHz
STABILITY:
AGING RATE: $<5\times10^{-10}$ per day for oscillator off time less than 24 hours.
SHORT TERM: $<1\times10^{-11}$ for 1s average
TEMPERATURE: $<7\times10^{-9}$ 0°C to 50°C
LINE VOLTAGE: $<1\times10^{-10}$, ±10% from nominal, 15 minutes after change.
**PRICES IN U.S.A:**
5370A Universal Time Interval Counter (includes HP-IB), $6500.
Option 001 High-Stability Time Base, $575.
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.

# SPECIFICATIONS
## HP Model 5359A Time Synthesizer

**MODES:**
EXTERNAL TRIGGER MODE: "Delay" and output pulse width must both be selected. "Delay" is the time from the leading edge of the sync output to the leading edge of the output pulse.
INTERNAL TRIGGER MODE: Period or frequency is selected and the width of the output pulse is specified. "Delay" is not specified in this mode.
**RANGE:**
DELAY: 0 ns to 160 ms
WIDTH: 5 ns to 160 ms (width+delay≤160 ms)
PERIOD: Minimum 100 ns or width+85 ns. Maximum 160 ms.
FREQUENCY: Same as corresponding period
**STEP SIZE:** 50 ps minimum, keyboard selectable, for both "width" and "delay".
**ABSOLUTE ACCURACY:** ±1 ns ± time base error
**INSERTION DELAY:** Less than 150 ns in preset. For "delays" greater than 100 ns, reduced to less than 50 ns in the auto position. Fixed in both cases.
**JITTER:** Between external trigger or sync out, and the output pulse.
STANDARD TIME BASE:
100 ps rms typical 200 ps rms max (delays 0 to 10 ms)
500 ps rms typical 1 ns rms max (delays 10 ms to 160 ms)
HIGH STABILITY TIME BASE (Option 001):
100 ps rms typical 200 ps rms max (delay 0-160 ms)
**EXTERNAL TRIGGER INPUT:** Trigger level adjustable −2V to +2V. Slope selectable + or −.
**MANUAL TRIGGER:** Pushbutton
**SYNC OUTPUT:** 1 volt positive pulse into 50Ω, from 200Ω source impedance.
Width 35 ns nominal. Rise/Fall times <5 ns.
**OUTPUT PULSE:**
Amplitude adjustable from 0.5V to 5V into 50Ω from 50Ω output impedance.
Offset adjustable from −1V to +1V, or OFF.
Normal or Complement Mode selectable; Rise/Fall times less than 5 ns; typical 3.5 ns.
Short circuit proof; external voltage must not be applied.
Offset and Amplitude may be displayed.

**REPETITION RATE:**
INTERNAL TRIGGER MODE: Maximum repetition rate 10 MHz.
Period ≥width + 75 ns typical.
EXTERNAL TRIGGER MODE: "Preset" Sync Delay
Maximum repetition rate 7.5 MHz typical
Period ≥delay + width + 75 ns typical
"Auto" Sync Delay
Maximum repetition rate 13 MHz typical
Period ≥delay + width − 30 ns typical
The "Auto" mode requires a delay of at least 100 ns. For delays of less than 100 ns, the same specifications as for "Preset" apply.
**EDGE 1 OUTPUT:** (rear panel)
Occurs with fixed time relationship to the leading edge of the output pulse. Specifications are the same as for SYNC OUT.
**EDGE 2 OUTPUT:** (rear panel)
Occurs with fixed time relationship to the end of the output pulse. Specifications are the same as for SYNC OUT.
**EVENTS MODE:** Substitutes an external input for the internally counted clock. "Delay" and "Width" must both be specified in events.
TRIGGER LEVEL: Adjustable −2V to +2V
SLOPE: Selectable + or −
FREQUENCY: Up to 50 MHz
Delay from "Ext Trigger Input" to the first event counted is less than 50 ns
RANGE: "Delay" 2 events to 16777215 events
"Width" 1 event to 16777214 events
"Width" + "Delay" <16777216 events
**FREQUENCY STANDARD** (rear panel)
INPUT: 5 or 10 MHz >1.0V p-p into 1 kΩ. Maximum input 10V.
OUTPUT: 10 MHz. 1V p-p into 50Ω in sync with time base chosen (INT or EXT).
**TIME BASE:**
CRYSTAL FREQUENCY: 10 MHz
STABILITY:
Aging Rate: $<3\times10^{-7}$ per month.
Short Term: $<2\times10^{-9}$ rms for 1 s
Temperature: $<2\times10^{-6}$ 25°C to 35°C
$<5\times10^{-6}$ 0°C to 55°C
Line Voltage: $<1\times10^{-8}$, ±10% from nominal
**OPTION 001: HIGH STABILITY TIME BASE:**
CRYSTAL FREQUENCY: 10 MHz
STABILITY:
Aging Rate: $<5\times10^{-10}$ per day for oscillator off time less than 24 hours.
Short Term: $<1\times10^{-11}$ for 1 s average
Temperature: $<7\times10^{-9}$ 0°C to 55°C
Line Voltage: $<1\times10^{-10}$, ±10% from nominal 15 min. after change.
**OPERATING TEMPERATURE:** 0° to 50°C
**POWER REQUIREMENTS:** 100, 115/120, 220, 230/240 volts +5%, −10%. 250 VA.
**WEIGHT:** 14.55 kg (30 lbs.).
**DIMENSIONS:** 133 mm H × 426 mm W × 521 mm D (5¾ × 16¾ × 20½ in.)
**PRICES IN U.S.A.:**
5359A Time Synthesizer (includes HP-IB), $6500.
Option 001 High Stability Time Base, $575.
**MANUFACTURING DIVISION:** SANTA CLARA DIVISION
5301 Stevens Creek Boulevard
Santa Clara, California 95050 U.S.A.

# Time Synthesizer Generates Precise Pulse Widths and Time Delays for Critical Timing Applications

*This time synthesizer's extremely stable, low-jitter time delays may be synchronized precisely to an external trigger. Automatic calibration and HP-IB compatibility are standard features.*

**by Keith M. Ferguson and Leonard R. Dickstein**

ADVANCES IN TIME AND FREQUENCY measurement capability have generated an increasing need for the generation of accurate time intervals. In frequency measurements, for example, the accuracy for a given gate time has been continuously improving. Modern counters, such as the HP 5370A (see article, page 2), obtain great accuracy with very short gate times (better than 0.5% in 20 ns), an important consideration when measuring changing signals, such as the sweep of a VCO, or bursts (pulsed RF). This ability to obtain useful results with short measurement gate times creates a need to position and move these gate times accurately with respect to the time of occurrence of the event of interest.

The ability to position a pulse in time easily and accurately leads to other advantages. For example, in characterizing complex logic networks or systems it is desirable to test for "race" conditions at critical points in the circuit (see Fig. 1). The availability of a stable, long, variable delay with known absolute accuracy and high resolution can simplify this measurement.

To be useful in applications such as these, a delay generator needs the following characteristics:

- Stable over the entire delay range (low jitter)
- Stable insertion delay (low jitter from the external trigger and the sync output to the delayed output)
- Good absolute accuracy from the sync output (so that an oscilloscope or a counter is not needed to verify the delay setting)
- High resolution (the ability to move the pulse in small steps)
- Ability to generate both zero delay (sync output coincident with delayed output) and relatively long delays.

Traditional pulse generators provide versatile output shaping and levels, but typical jitter specifications of 0.1% limit their usefulness at longer delays for precision timing applications. The digital entry of delay data provided in the newer pulse generators can be a real advantage in the ease of setting up a measurement, but for applications requiring better than 1% accuracy, an oscilloscope or a meter may still be necessary.

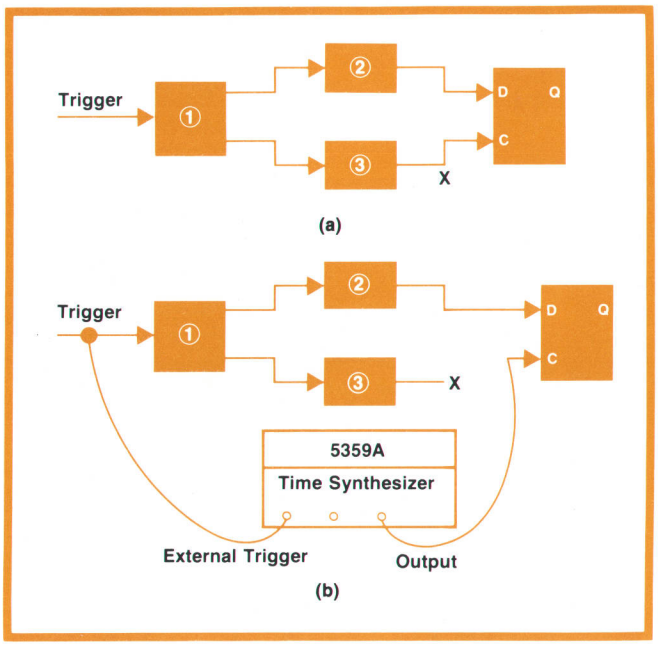



**Fig. 1.** *Model 5359A Time Synthesizer can help test for race conditions in logic systems. In the hypothetical system of (a), an input trigger passes through subsystems 1, 2, and 3 before arriving at the D and C inputs of the flip-flop. Changes in propagation delays through the two paths could result in improper operation of the flip-flop. The problem is to measure the allowable range of delays. The measurement is more difficult if the D input is a data string from which one bit is to be selected, or if the setup time of the flip-flop is unknown. In (b), the time synthesizer output is substituted for the signal at point X. The synthesized delay can be varied easily to determine the limits of proper operation. Because the synthesizer can produce relatively long delays, it can be triggered from the input of the system, which is often easier than finding a suitable internal trigger point.*


**Fig. 2.** *Model 5359A Time Synthesizer generates precise time delays and pulse widths from 0 to 160 ms (width + delay ≤160 ms). Absolute accuracy is ±1 ns ± time base error. With the optional high-stability time base, jitter is <200 ps rms (100 ps typical). Features include keyboard control, HP-IB programmability, and automatic calibration.*

### New Time Synthesizer

Clearly a need exists for an instrument capable of providing a high-accuracy, low-jitter timing signal. Model 5359A Time Synthesizer, Fig. 2, was designed with this need in mind. It provides delays from its sync output to its delayed output that are accurate within one nanosecond (plus time base error) over its entire delay range of 0 to 160 milliseconds. With its optional oven oscillator, worst-case jitter is 200 picoseconds rms; 100 ps is typical. Fig. 3 compares the time synthesizer's output to that of a high-quality pulse generator at a delay of about 100 $\mu$s.

Model 5359A's output pulse width is selectable from 5 ns to 160 ms. Resolution (minimum step size) in both width and delay is an extremely low 50 ps. Output amplitude and offset are also selectable. All output parameters are specified using the front-panel keyboard or remotely via the HP-IB interface (IEEE 488-1975, ANSI MC1.1), a standard feature.

Calibration is automatic—an important feature in high resolution time measurement work. In just two seconds, five internal parameters are calibrated for the effects of temperature and aging. Thus the instrument can be calibrated immediately before use, assuring specified accuracy in each measurement.

Applications of Model 5359A include investigation of timing relationships in digital communications and digital computer circuits, component testing, radar systems testing, and calibration. In testing components, the 5359A can simulate an accurate delay line. It can also be used to generate precise delays for oscilloscope sweeps and for accurately time positioning external gates for frequency counters.

### Design Approach

After considering several delay generation techniques, we decided that the 5359A would have two internal channels, with one channel setting the delay from the sync output to the delayed output, and the other setting the width of the delayed output pulse. The requirements outlined above indicated a digital system, that is, one counting cycles of a clock to generate the desired delay.

Traditional techniques have involved either of two approaches. One approach uses an accurate, continuously running clock, such as a crystal. This yields good repeatability from the sync output to the delayed output, but has an inherent jitter of up to one clock period in the insertion delay, because the time of occurrence of the external trigger is random with respect to the internal clock. Nevertheless, for long delays, the accuracy and stability of the crystal are desirable, and it can be rationalized that the insertion delay jitter is of lesser importance.

The other traditional approach uses a startable oscillator, thus eliminating the digital jitter on the insertion delay. Unfortunately, startable oscillators generally do not have the stability or accuracy of continuously running crystals, creating problems at longer delays. Attempts to phase lock the startable oscillator to a crystal normally result in shifting the phase of the

startable oscillator, negating the benefit of the startable oscillator by reintroducing the one-period jitter.

In an early 5359A design, counting of a 200-MHz startable oscillator generated the major portion of the delay, and analog circuits were used to interpolate between counts. A time interval counter measured the actual delay, and a microprocessor used the measurement data to correct the input parameters to the digital and analog delay circuits. A working breadboard was built using this approach.

Several drawbacks were inherent in this method. Foremost was the uncertainty in the frequency of the startable oscillator, which varied not only with temperature and aging, but also with the rate at which it was restarted (because of temperature effects). This led to the need for frequent recalibrations; each time new data was entered, the output was measured and corrected. Some improvement in the frequency stability of the startable oscillator was obtained by running it almost continuously, stopping it only briefly before each new restart, but this improvement was not enough.

A solution to many of these difficulties came with the invention of the triggered phase-locked oscillator (see box, page 8). This oscillator provides the advantages of a startable oscillator in producing a stable insertion delay. By locking to a crystal oscillator, it also provides accuracy for long delays. Its principal feature is that the phase-locking process introduces only negligible phase shift, thus providing the best characteristics of both traditional approaches to delay generation.

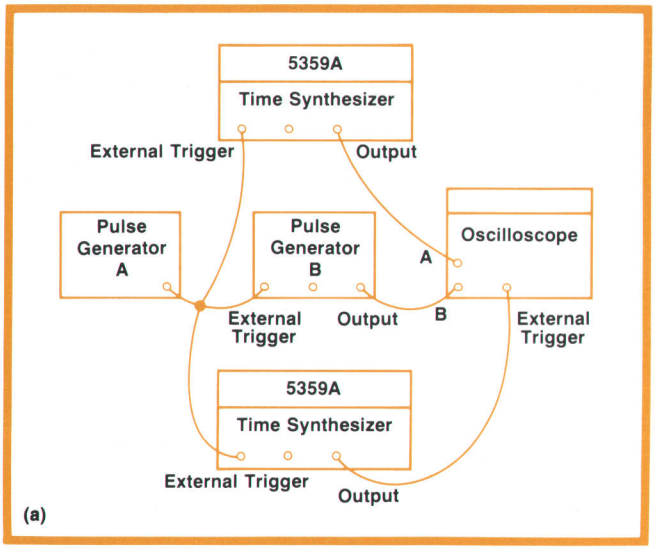
Fig. 4 shows a block diagram of the resulting instrument. The two delays are initiated from the same point, the input trigger, making it possible to use only one triggered phase-locked oscillator while avoiding the problems of synchronizing two separate count chains. Although the two delay channels actually set the delays from the input to the beginning and end of the output pulse, the user specifies the output in terms of a delay and a width, and the microprocessor performs the necessary calculations.

Because the triggered phase-locked oscillator provides an accurate, known frequency to the digital delay chains, it is not necessary to perform a new calibration each time new data is entered. However, errors in the output timing could still arise from the following sources:

- Fixed delays associated with the various elements in the delay chains and output circuitry
- Inaccuracies in the analog interpolators
- Finite rise and fall times of the output pulses.

### Fixed Delays

Care was taken during the design to guarantee that the fixed delays were really fixed, that is, that they did



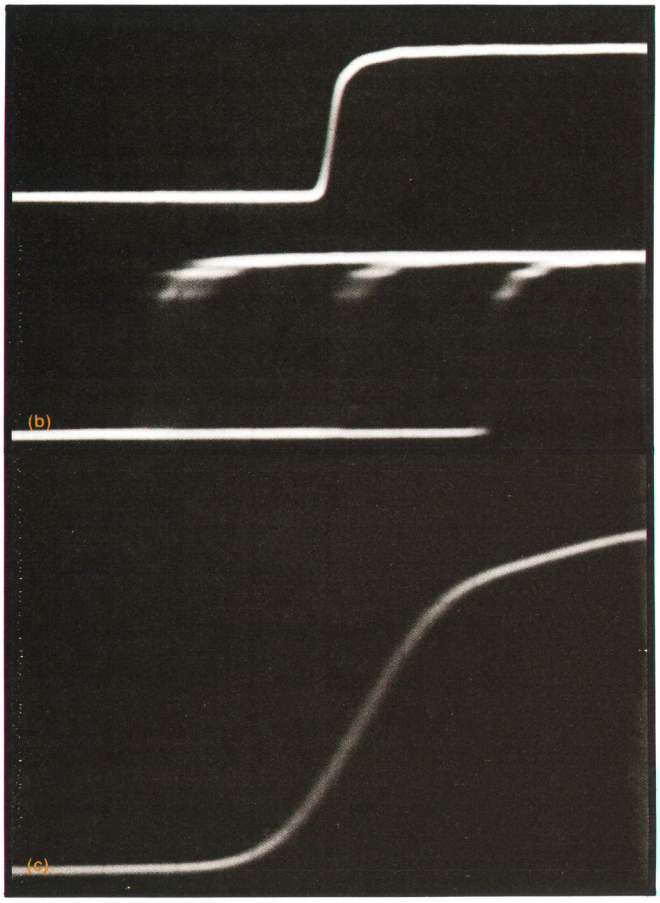




**Fig. 3.** *Jitter of Model 5359A Time Synthesizer compared to that of a pulse generator at 100 μs delay. (a) Test setup. Pulse generator A supplies trigger signals to the two synthesizers and pulse generator B. The lower synthesizer provides a delayed trigger to the oscilloscope. The two synthesizers operate on independent time bases. (b) Upper trace: 5359A output. Lower trace: pulse generator output. Horizontal scale: 10 ns/div. Delay about 100 μs. Multiple exposure over 20 seconds. Note stability of upper trace compared to lower. (c) 5359A output. 1 ns/div. Delay about 100 μs. Multiple exposure over 20 seconds. Note low jitter and drift.*

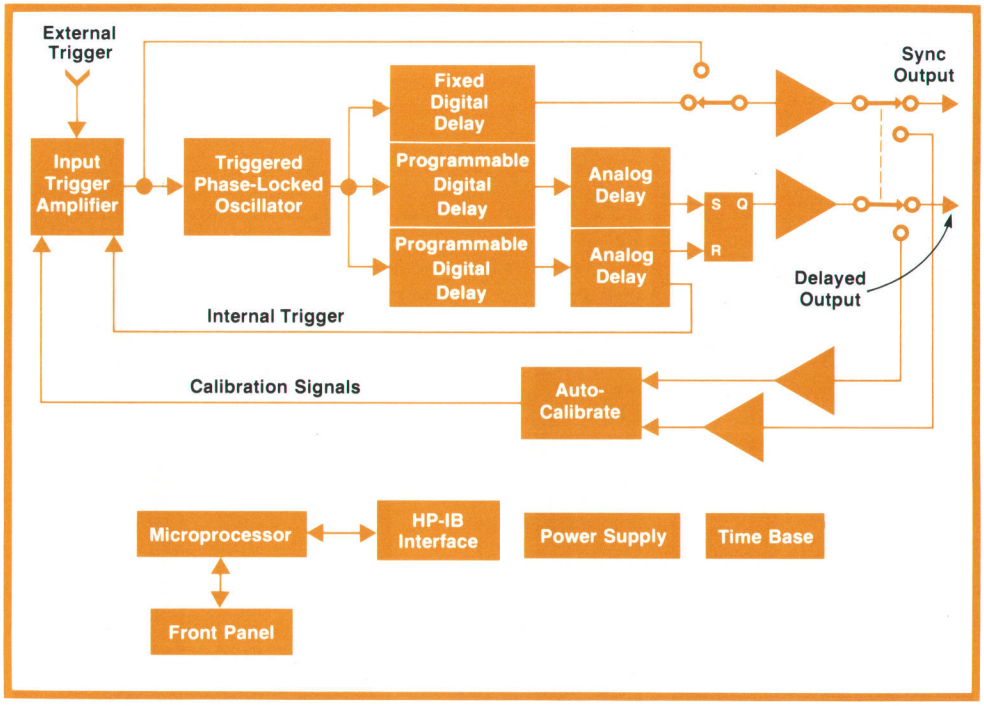



**Fig. 4.** *The 5359A's two programmable delay channels generate delays from the sync pulse to the beginning and the end of the delayed output pulse, respectively. Analog circuits interpolate between clock pulses to give 50-ps resolution.*

not vary as a function of the delay, width, or pulse repetition rate. We recognized, however, that they would vary with temperature, aging, and component-to-component variation among instruments. Instead of attempting to control these factors, we provided an automatic calibration mode. A complete calibration, taking about two seconds, occurs at power-up and can be repeated at any time by touching a front-panel CALIBRATE button or sending a command via the HP-IB. The microprocessor stores the results of the most recent calibration and uses these to determine the correct settings for the digital and analog delays.

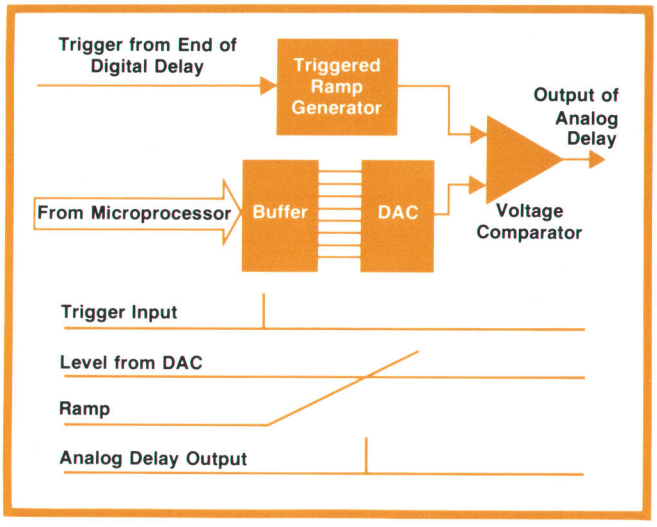



**Fig. 5.** *Analog interpolators use 8-bit digital-to-analog converters to divide clock periods into 256 parts.*

### Analog Interpolators

Each analog interpolator contains a current source that charges a capacitor, with the resulting ramp voltage supplied to one input of a voltage comparator, as shown in Fig. 5. The other comparator input is driven by a digital-to-analog converter (DAC). The digital input to the DAC sets the voltage level to the comparator, and thus determines the time from the start of the ramp until the comparator detects the crossover of its two inputs.

The range of each interpolator must be slightly longer than the minimum step size of the digital delay, which is one period of the counted clock, or about 10 ns. An eight-bit DAC is used, dividing this interval into 256 parts, each step representing about 45 ps. Thus the quantization error, or resolution, is small compared to the absolute accuracy.

Instead of requiring precise adjustment of the analog step size, we chose to have the calibration routine measure this step size. This measured value is then used in determining subsequent settings of the interpolators. The measurement actually determines the average step size over a range of about 10 ns, and therefore assumes linearity of the interpolator. Considering the relatively short range of the interpolator compared to the required accuracy, this is a reasonable assumption.

### Rise and Fall Times

Because real waveforms have non-zero rise and fall times, the apparent absolute accuracy of a precision delay generator depends on the points on the output waveforms at which the measurements are made. The

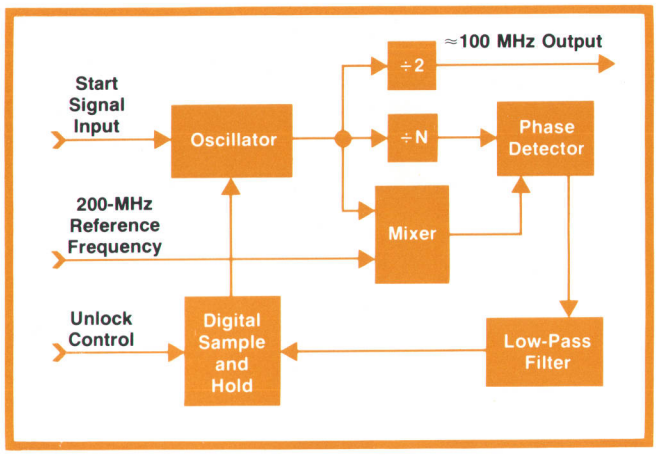



**Fig. 6.** *A triggered phase-locked oscillator generates the clock frequency counted by the digital delay circuits. A sample-and-hold circuit is activated when the selected (width + delay) is short. The circuit measures the VCO voltage during phase-locked conditions and holds that value during high-repetition rate operation.*

calibration technique used in the 5359A uses trigger amplifiers to examine the sync and delayed output signals and provide inputs to the measurement circuit. The trigger reference levels provided to these amplifiers determine the points on the output waveforms at which calibration occurs, and therefore the points at which the accuracy is assured. As the output amplitude and offset are varied, either from the front-panel controls or via the HP-IB, the trigger reference levels are maintained at the nominal 50% points on the waveforms (assuming 50Ω terminations).

### Period Generation

Instead of generating a pulse delayed from an externally supplied trigger, the two delay chains can be used to generate a pulse repetition rate (period) and a width. In this configuration the end of each output pulse serves as an internal trigger to restart the delay channels.

### Obtaining Zero Delay

For some applications, it is desirable to set the delayed output to zero delay, that is, to have it occur simultaneously with the sync output. Even with the digital and analog delay circuits set to their minimum values, the delays through these circuits will be longer than the minimum achievable delay in the sync channel. Therefore, a fixed digital delay is included in the sync path, moving that signal sufficiently in time for the minimum programmed delay to match it.

Adding a fixed delay to the sync channel represents an increase in the insertion delay of the instrument. From the user's viewpoint, it is equivalent to using a longer cable to drive the trigger input. For applications where a shorter insertion delay is critical, the added sync delay can be switched out, providing a sync output that is simply a shaped and buffered version of the trigger input. Under these conditions, however, the minimum programmed delay from sync output to delayed output is 100 ns.

### The Startable Oscillator

The startable oscillator generates the clock frequency counted by the digital delay circuits. The phase-locked loop circuitry is essentially the same as described elsewhere in this issue (see article, page 2) and will not be repeated here. However, because of the different use of the oscillator output, there are two significant differences (see Fig. 6). First, the oscillator output frequency is divided by two before being sent to the digital delay counters. This is necessary because these counters are capable of counting 100 MHz but not the oscillator frequency of approximately 200 MHz. Second, attempts to restart the oscillator at repetition rates greater than the phase detector input frequency ($f/N = 200\ MHz - f \approx 1.5\ MHz$) would prevent the phase-locked loop from ever acquiring lock. Left in this mode, the oscillator would drift to its limits, causing a large frequency error in its output. To prevent this while still allowing operation of the 5359A at up to 10-MHz pulse repetition rates, a digital sample-and-hold circuit was added to the loop. This circuit measures the VCO voltage during lock conditions and holds that value on the oscillator during high-repetition-rate operation. The command to sample and hold is sent from the microprocessor whenever the user requests a period or a combination of a delay and a width less than about one microsecond. That command initiates a measurement of the voltage present at that instant, and upon completion switches the oscillator VCO line over to the output of the hold circuit. Pressing the CALIBRATE key sets the instrument to a rate of operation that allows the loop to lock, reissues the sample-and-hold command and then returns to the desired rate.

The sample-and-hold circuit consists of an eight-bit analog-to-digital converter (ADC) and a digital-to-analog converter (DAC). The VCO voltage is measured by the ADC, held as a digital word, and applied to the DAC. The DAC output is the voltage applied to the oscillator.

### The Digital Delay Circuits

Each programmable digital delay consists of a single custom IC containing a presettable $2^{24}$ down counter. The preset number is stored in a 24-bit shift register on the same chip, and is automatically reloaded into the counting register at the completion of each count. Emitter-follower-logic (EFL), using multiple-emitter transistors (almost 1200 emitters),

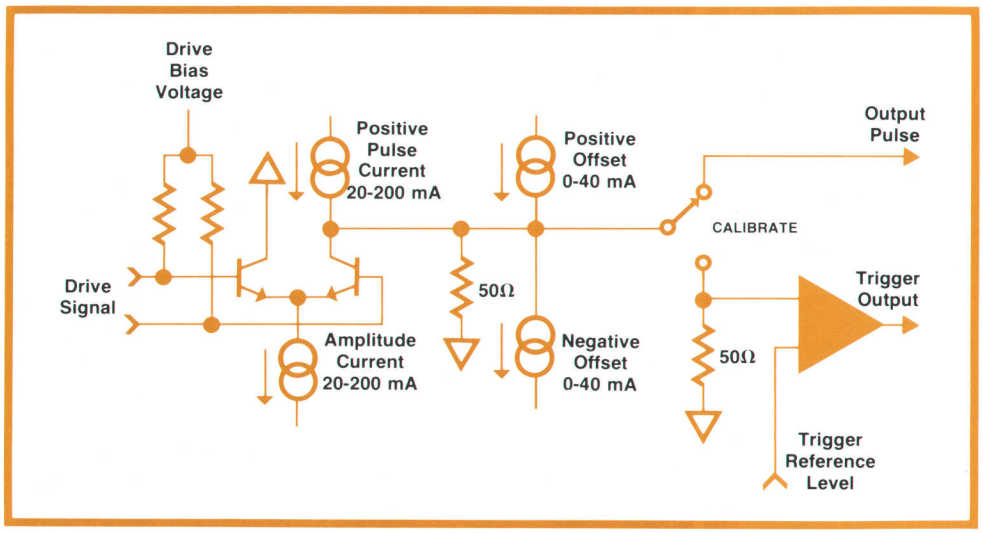



**Fig. 7.** *Time synthesizer output amplifier produces a pulse of ±0.5 to ±5.0 volts into 50Ω.*

makes speeds greater than 100 MHz possible, with about ¼ watt of power to each IC. The microprocessor converts the binary delay number into a special code used by these high-speed counters.

### The Output Amplifier

The output amplifier consists of two assemblies. The first is the actual output amplifier and calibration trigger circuits and the second contains the voltage and current sources that control the output polarity, amplitude, and offset, and generate the trigger reference voltage. The output stage consists of a current-mode, switching-pair amplifier followed by a switch and either the instrument output connector or an internal 50Ω load and high-speed voltage comparator (see Fig. 7).

During the calibration mode, the output signal is switched to the internal load and comparator, and the trigger reference level is set to the 50% point of the pulse. The trigger reference level is generated by an operational amplifier summing circuit that monitors the signal polarity, amplitude, and offset controls. If the user does not terminate the output in 50Ω, the output amplitude will be different from what it would be with a 50Ω termination. Because the rise time is non-zero, this will cause the 50% point to shift, resulting in a small error (typically less than 1 nanosecond) in the absolute accuracy of the output.

The output amplitude is specified at ±0.5 to ±5.0 volts into a 50Ω load with a 50Ω source impedance. This translates into a current requirement of ±20 to ±200 mA. The output circuit sinks 20 to 200 mA to generate the negative polarity pulse, and a 20-to-200-mA current source supplies current to the output node when positive polarity is required. The ±1 volt offset is set by sourcing or sinking an additional 40 mA.

The switching transistors are contained in a hybrid circuit consisting of both the drive stage and the output stage. Included on the hybrid substrate are thin-film resistors and chip bypass capacitors. The substrate is sapphire, resulting in a low thermal resistance to the package.

### Autocalibration

The autocalibration circuit, Fig. 8, consists of a precedence detector, a timing signal generator, and a simple state machine for on-board control. Besides providing a clock to the state machine, the timing signal generator injects reference signals into the 5359A timing channels during the calibrate operation.

The precedence detector is the heart of the autocalibrate scheme. Its function is to compare the time relationship of two signals, indicating which occurs first. Subnanosecond differences in the propagation delays and transmission paths of signals supplied to the precedence detector, as well as differences within the detector itself, can affect the apparent timing of the signals being compared. Because of this, the detector has an offset, or balancing feature, so that these differences can be calibrated out.

The circuit bears some resemblance to the analog interpolators already described. The A signal starts a ramp that is compared against a voltage level from a DAC, but here the result of the comparison is stored (sampled) upon receipt of the B signal (following a short, fixed delay). The detector is calibrated by initially driving the A and B signals from the same source, so that they occur, by definition, simultaneously. The voltage from the DAC is then varied until the ramp is just crossing it at the time of sampling. The DAC voltage is held constant at this level during future measurements, and A and B are connected to the signals of interest. The order of occurrence of A and B is thus determined by the relative position of

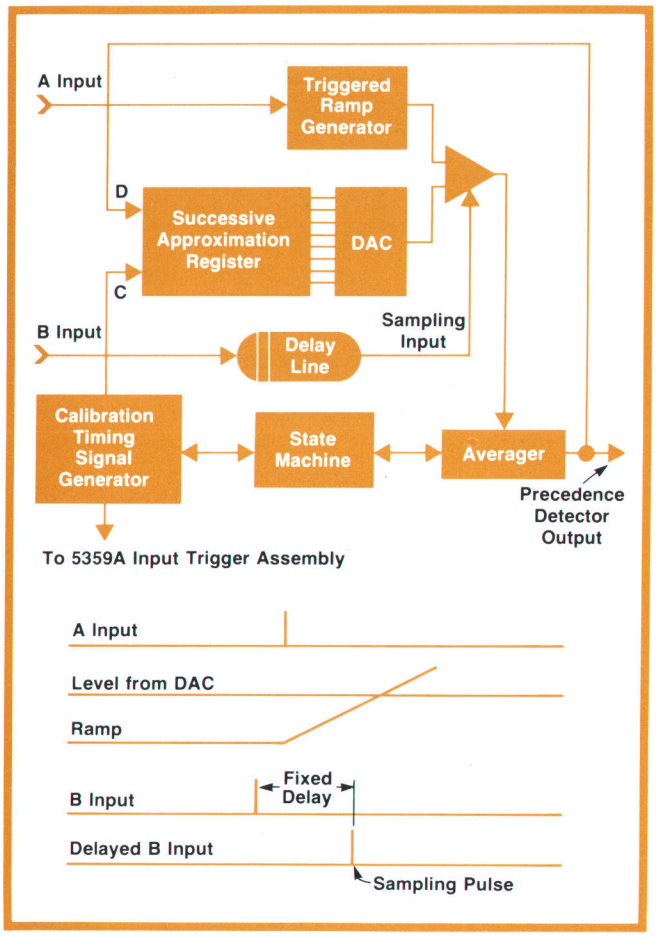



**Fig. 8.** *Autocalibration circuit consists of a timing signal generator, a state machine controller, and a precedence detector that tells whether A or B occurs first. In the example illustrated here, the sampling pulse occurs before the ramp crosses the DAC output level, indicating that the B input preceded the A input. The precedence detector is calibrated initially by driving the A and B input with the same signal. The successive approximation register then adjusts the DAC output so the ramp voltage crosses it at the moment that sampling occurs. Averaging reduces the effects of noise. To calibrate the 5359A, the microprocessor measures all fixed delays by moving the 5359A's delayed output with respect to the sync output until the precedence detector indicates a change in the order of occurrence of these signals. The programmed delay at that point is stored as a reference. Separate references are determined for programmed delays, width, and period.*

the ramp voltage with respect to the DAC voltage at the time of sampling. Balancing the precedence detector in this way removes the effects of delays not only in the detector, but also in the trigger amplifiers and the transmission paths. Averaging is used to reduce the effects of random noise.

To measure the fixed delays in the 5359A, the microprocessor moves the delayed output with respect to the sync output until the precedence detector indicates a change in the order of occurrence of these signals, thus determining coincidence. This then serves as a reference point from which any specified delay can be programmed.* Separate calibration constants are determined for the two different insertion delays (see above), for width, and for period.

When measuring the analog step size (see "Analog Interpolators" above), the offset feature of the precedence detector is used in a different manner. Here the technique is to adjust the digital delay for the closest possible coincidence while keeping the analog delay set to zero, and then to use the offset of the precedence detector to store this difference. In other words, the DAC level is moved until sampling occurs as the ramp crosses it, although the A and B inputs are not now occurring simultaneously. The digital delay is then changed by one step (about 10 ns) and the analog delay adjusted to restore this same offset. The number of "steps" of analog delay needed to equal the 10 ns change in the digital delay determines the analog step size. Separate measurements are made for each channel.

### External Calibration

The internal calibration scheme provides for timing accuracy at the output connectors of the instrument. In actual measurement situations, this accuracy may be needed at a point remote from the time synthesizer, such as at the ends of cables of varying lengths. The HP 5363 Time Interval Probes[1] can be used to probe the signals at the point of actual interest, with the output of the probes fed back to the 5359A. The autocalibrate circuit in the 5359A can then use these probe signals to compensate for delays external to the time synthesizer. In this mode of operation, the 5359A provides control signals to the 5363 probes, changing the configuration as needed during the various stages of the calibration procedure.

In some instances it may be desirable to pass the output of the 5359A through an external pulse generator or shaper, to provide different amplitudes or shapes than are directly available. Assuming that certain timing constraints are met by this external circuitry, the 5363 probes and the external calibration capability of the 5359A can be used to calibrate out the delays and rise/fall time effects of this external device.

### Acknowledgments

Credit is due Dick Morrell for design of the LSI integrated circuit, built by the Santa Clara Division IC facility and used for the digital delay chains; Karl Ishoy and the Santa Clara hybrid facility for support of the triggered oscillator and output amplifier hybrids; Carl Spalding for a product design that took full advantage of the commonality with the 5370A; Bernard Barke for industrial design; Al Foster, Mark Al-

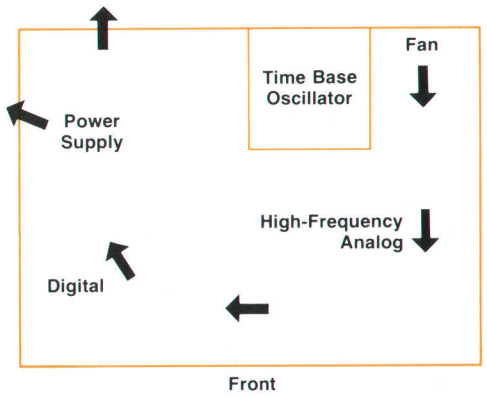
*During calibration a special delayed sync signal with a known time relationship to the normal sync signal is used. This simplifies the implementation without changing the basic technique described here.

## Instrument Commonality, Reliability, and Serviceability

The 5359A Time Synthesizer (page 12) and the 5370A Time Interval Counter (page 2) were designed as state-of-the-art instruments with emphasis not only on performance but also on reliability, serviceability, and manufacturability. Contributing heavily to this goal was the high degree of commonality between the two instruments. Besides using the same triggered phase-locked oscillator, both instruments share the same power supply, time base, and microprocessor circuitry as well as several mechanical design aspects. The emphasis in these areas was on ease of understanding, troubleshooting, and accessibility.

The common power supply is a linear series-pass design including current limiting, overvoltage protection, thermal cutout switch, and LED voltage indicators. The output voltages are referenced to a precision voltage reference, eliminating the need for adjustment trimmers and calibration procedures. Considerable derating was used in the choice of components to increase reliability. The very low-noise output of a linear supply helps achieve the picosecond jitter capability of these instruments.

The time base sections of both instruments consist of three assemblies: the room-temperature crystal oscillator (or optional high-stability oven oscillator), the internal/external oscillator buffer, and the 10-MHz-to-200-MHz multiplier. The high-stability oven oscillator option has it own power supply to maintain standby power and simplify servicing. The internal/external oscillator buffer accepts either a 5-MHz or a 10-MHz external input, uses a double-gating scheme to improve internal/external signal isolation, and includes a signal-present LED to indicate loss of signal. The multiplier technique was chosen to obtain the 200-MHz reference frequency because it provides a cleaner, more stable signal than a phase-locked loop design, besides being straightforward and easy to understand. This is important because the vernier oscillators are directly phase-locked to this 200-MHz reference, requiring excellent long-term and short-term stability.




The microprocessor section was an area of special concern, since service personnel could be unfamiliar in that area. Much attention was given to increased serviceability (see article, page 2). Both instruments use the same microprocessor assembly, display interface assembly, HP-IB interface assembly, and service aid accessory assembly. The program ROMs have different patterns in the two instruments, but otherwise this assembly too is common to both.

The exceptionally clean product design of both instruments benefitted from an effort to optimize air flow for effective cooling. As the diagram shows, forced air from the fan passes the high-frequency analog sections first, is directed through the digital sections, and is vented out past the power supply. The crystal oscillator is isolated in the "eye of the cyclone" for minimum thermal drift. The result of this approach is that the interiors of both instruments exhibit only a 7° C average rise above ambient, with a worst-case 12° C rise at high line power input, as well as a very open, accessible, well organized board layout.

*–Leonard Dickstein*

len, Art Lange, and Mike Ward for electrical design; Jim McNeish for marketing support; Charles Trimble for guidance in the early stages; Dave Chu, Jim Sorden and Jim Horner for their support and valuable suggestions along the way; and many, many others.

**Leonard R. Dickstein**

Leonard Dickstein did analog circuit design for the 5359A Time Synthesizer and the 5370A Counter and served as production engineer for a time on both instruments. Raised in Oakland, California, he received his BSEE degree in 1971 and his MSEE degree in 1973 from the University of California at Santa Barbara, and has continued his studies on a part-time basis since joining HP in 1973. Len spends his spare time remodeling and maintaining his home in San Jose, working on his three Chevrolets, and playing chess. He and his wife, who also works at HP, have a three-year-old daughter.

**Keith M. Ferguson**

Keith Ferguson, project leader for the 5359A Time Synthesizer, was born in Corpus Christi, Texas and studied electrical engineering at Massachusetts Institute of Technology, receiving the SB degree in 1962, the SM degree in 1964, and the degree of Electrical Engineer in 1965. He first worked for HP during the summers of his undergraduate years and joined the company permanently in 1965. He helped design and market the 5360A Computing Counter and was project leader for the 5365A Keyboard. He's a member of IEEE. Keith is an avid square dancer and an enthusiastic promoter of the hobby. He also enjoys backpacking, hiking, and classical music. A bachelor, he serves on the regional single adult task force of his church. He makes his home in San Jose, California.

### Reference

1. R.W. Offermann, S.E. Schultz, and C.R. Trimble, "Active Probes Improve Precision of Time Interval Measurements," Hewlett-Packard Journal, October 1975.

# Remotely-Controlled RF Switch for Multipoint Tests in Communications Systems

*Under manual or HP-IB control, this RF switch provides access to any one of 10 inputs carrying signals in a range of 10 kHz to 25 MHz or, when cascaded with other switches, to any one of up to 1000 inputs.*

**by Kevin J. Bradford**

CHECKING OUT A MULTIPLEXED communications system often requires connection of the measuring instrument to several different points one at a time. In many cases, elaborate switching networks using electromechanical relays are installed to facilitate making these connections.

During the development of the HP Model 3745A Selective Level Measuring Set,[1] it was realized that system checkout with this instrument could be speeded considerably if there were an RF switch that could be controlled through the HP interface bus* to make the system connections. This would greatly simplify the integration of automatic test systems for fast checkout of communications systems. However, no such switch existed at the time, so we undertook the development of one.

*Hewlett-Packard's implementation of IEEE Standard 488-1975, and ANSI Standard MC1.1.

**Fig. 1.** *Model 3754A Access Switch (lower unit) connects any one of ten RF inputs to a single output under control of the Model 3755A Access Switch Controller (upper unit). Inputs can be selected manually by way of the Controller's front panel pushbuttons or under automatic control by way of the HP interface bus. LED indicators in the dark panel above the Access Switch inputs light up to show which input is connected to the output.*

The access switch that resulted from this development is shown in Fig. 1. Known as HP Model 3754A, it is a unidirectional, single-pole switch with ten inputs, any one of which may be switched to the single output either manually or automatically by way of the HP interface bus. Besides applications in multiplexed communications systems, it is anticipated that this switch will also find use for switching RF signals in other types of automatic test systems, such as those involved in production test or data acquisition, where low insertion loss in the "on" channel and high isolation in the "off" channel are required. The switch is suitable for signals within a frequency range between 10 kHz and 25 MHz, and an amplitude range between +10 dBm and −115 dBm, the switch's thermal noise level.

### Separate Controller

Because the switch is intended for automatic systems, no provision was made for selecting inputs or outputs at the switch itself. Instead, a controller, Model 3755A (Fig. 1), was designed to operate one or more switches from a remote point. Channels can be selected manually by means of the pushbuttons on the controller, as well as automatically by way of the HP interface bus (HP-IB). One Model 3755A can control switches cascaded up to three levels, giving access from one controller to up to 1000 points (111 cascaded switches arranged in a 1-10-100 tree). One advantage of this arrangement is that only one HP-IB address is needed to access up to 1000 points.

### Design Details

The electromechanical relays previously used for test signal switching in frequency-division-multiplexed (FDM) communications systems often introduced insertion loss, exhibited poor return-loss

figures, and had poor isolation in the "off" channels. Frequently, expensive coaxial reed relays were used to minimize these problems.

The design approach chosen for the Model 3754A switch was to overcome the disadvantages of relays by imbedding the relays in an operational amplifier, as shown in Fig. 2. Switching is effected at the virtual-ground point where the voltage swings are very small. Thus, the effects of relay-contact stray capacitance are negligible even though conventional relays are used. As a result, insertion loss of the new switch is flat within ±0.1 dB between 50 kHz and 20 MHz, and within ±0.3 dB up to 25 MHz. Furthermore, the isolation between an "off" channel and the output is greater than 85 dB over the full 10-kHz-to-25-MHz frequency range, and the isolation between channels is greater than 90 dB.

Other advantages accrue from this configuration. The operational amplifier's series input resistor provides a convenient termination for the input signal cable, whether it is switched to the amplifier or switched to ground. Return loss is >30 dB for an "on" channel and >23 dB for an "off" channel. In addition, the amplifier gain can be adjusted to compensate for cable and relay losses. Internal jumpers enable the gain through the switch to be set to 0, 1, 2, or 3 dB.

### The Controller

Switching is effected by means of low-frequency pulses transmitted by the controller along the same RF signal cable that interconnects switches, a technique that greatly simplifies system integration by eliminating separate relay-control wiring. Pulses are generated at a rate of 20 pulses per second by an IC that interfaces directly to the front-panel keyboard. When a key is pressed, the IC, which was designed for pushbutton dialing, generates a number of pulses corresponding to which key was pressed (or to which number was sent over the HP-IB). The IC also has sufficient on-board memory to store keycodes as they are entered, when the controller is operating several cascaded switches, and transmit them in the correct sequence. The 3-digit LED display shows the input selected.

An example of how the controller interconnects with cascaded switches is shown in Fig. 2. The control technique makes use of the fact that the switch amplifiers are ac-coupled and have a lower frequency limit of 10 kHz. The control circuits establish a dc level of +10V at the output of each switch but the dc is kept from other parts of the system, including whatever device is connected to the RF output of the controller, by series capacitors.

Each switch has a pulse-counter circuit and control logic that monitors the output line. To see how the system works, consider a case where all switches

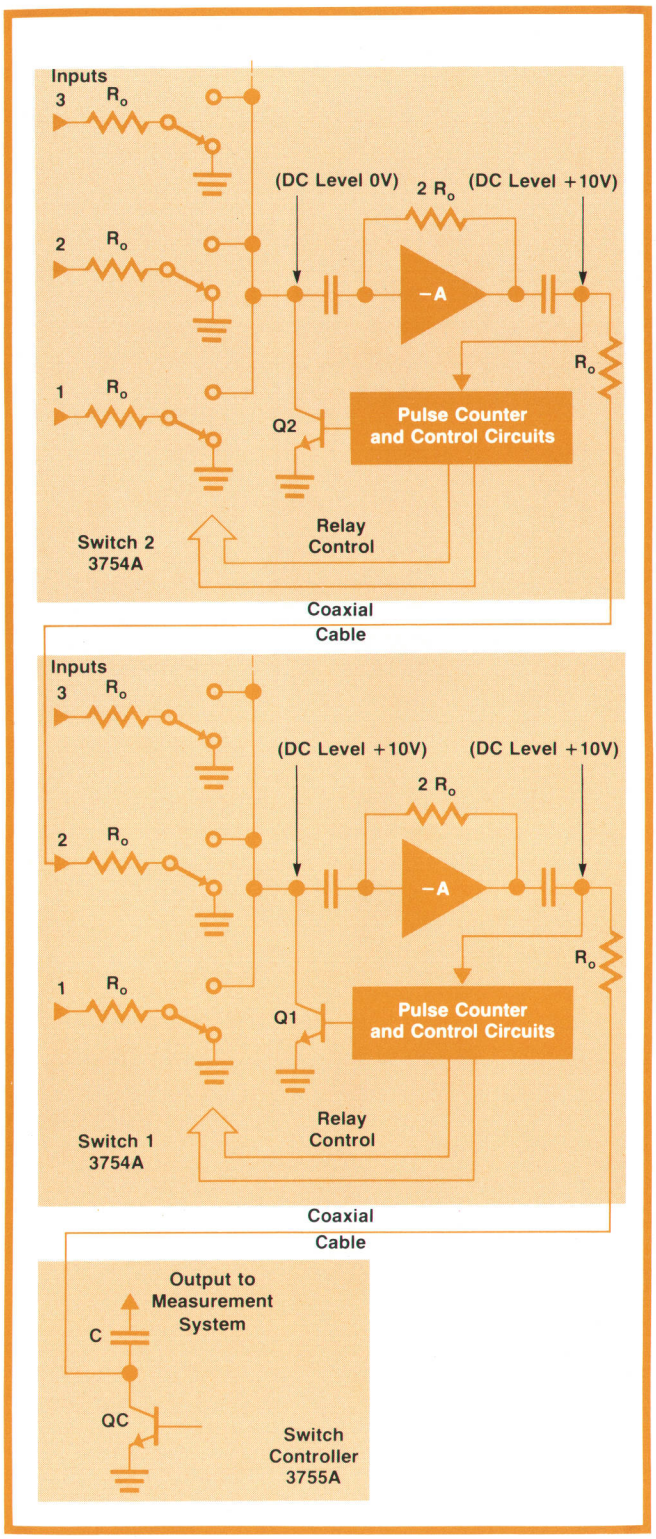



**Fig. 2.** *Basic switch configuration places relay switching contacts at the virtual-ground point of an amplifier where signal voltage swings are very small, reducing the effects of relay capacitance to negligible proportions.*

have just been opened (the CLEAR button was pressed). Now, if input 2 of Switch 1 (Fig. 2) is selected, transistor QC in the controller pulls the signal line to zero

volts twice. These two negative-going pulses are detected by the logic circuits in Switch 1, which close the relay for input 2. When this is done, the selection logic is disabled so the next string of pulses will have no effect on Switch 1.

The next string of pulses is regenerated in the control circuits of Switch 1 and applied to transistor Q1, which pulls the line connected to input 2 to zero volts the selected number of times. The logic circuits in Switch 2 count the number of pulses and connect the corresponding input to the amplifier. None of these pulses has any effect on any device connected to an input of Switch 2, however, since the +10V dc level does not exist at these points, leaving the collector of transistor Q2 at ground.

In general, the number of pulses corresponds to the number of the input desired. Once a selection has been made, the relay selection logic for that switch is disabled and any subsequent pulses are passed along to the next switch in the chain. In this way, any desired path in a large network of switches may be set up.

Switches are cleared by the controller's sending a string of fourteen pulses. Although the switch selection logic is disabled once an input selection is made, the pulse counters continuously monitor the pulse sequences and when an uninterrupted string of fourteen pulses is detected, the selected input is disconnected. Thus, all switches clear at the same time.

### Alternate Control Path

In cases where it is not possible (or convenient) to provide a continuous dc connection between switches—for example where there is an ac-coupled equalizer in the signal path—control signals can be passed along a separate pair of control wires. A pair of terminals for each channel is provided on the rear panels of the controller and the switches, enabling a choice of cable connection or separate-wire connection to the next switch on any channel.

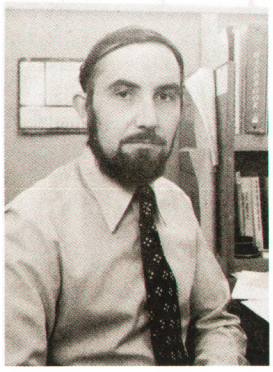
The separate control terminals also enable up to four switches to be operated in parallel from one controller. This is convenient where it is desired to switch two or more parallel signals simultaneously, such as the signal lines of a balanced-pair cable—both can be switched by a single channel command to the controller.


### Acknowledgments

Thanks are due Hugh Walker who originated the concept of relay switching at the virtual-ground input of an amplifier, David Dack for his encouragement in the early stages of the project to find a way of eliminating separate relay-control wiring, and Arthur Thornton for the product design.


### Reference


1. J.R. Urquhart, "An Automatic Selective Level Measuring Set for Multichannel Communications Systems," Hewlett-Packard Journal, January 1976.


**Kevin J. Bradford**

A native of Edinburgh, Scotland, Kevin Bradford earned a BSc degree at Heriot-Watt University in 1970. In 1972, he joined Hewlett-Packard Limited in South Queensferry, Scotland, after designing avionics equipment at another firm for two years. At HP, Kevin worked on the keyboard and display for the 3745A Selective Level Measuring Set before assuming project leadership for the 3754A/3755A Switch and Controller. At the same time, he attended Heriot-Watt part time and in 1977 earned an MSc degree in digital techniques. Most of Kevin's spare time is now spent in modifying the new home he acquired for himself and family (wife and two small children), getting the new garden under way, doing some woodworking, and whenever the water is right, swimming.


## SPECIFICATIONS

### HP Model 3754A Access Switch

**FREQUENCY RANGE:** 10 kHz to 25 MHz.
**INSERTION LOSS:** <±0.1 dB (50 kHz to 20 MHz); <±0.3 dB (10 kHz to 25 MHz).
**PRE-SET GAIN** (any one internally selectable): 0 dB; 1 dB, ±0.1 dB; 2 dB, ±0.1 dB; 3 dB, ±0.1 dB (75Ω version only).
**ISOLATION:** >85 dB between any input and the output; >90 dB between any two inputs.
**RETURN LOSS:**

| | | |
|---|---|---|
| SELECTED INPUT: | >30 dB | (60 kHz to 25 MHz) |
| UNSELECTED INPUT: | >23 dB | |
| OUTPUT: | >30 dB | |

**NOISE POWER RATIO:** >70 dB typical for −10 dBm total power applied over any 8-MHz band.
**THERMAL NOISE** (in any 3.1-kHz band):
<−115 dBm (60 kHz to 300 kHz);
<−120 dBm (300 kHz to 25 MHz).
**CONNECTOR TYPE:** 75Ω BNC is standard. Other types and impedances are available.
**POWER:** 100, 120, 220, 240V ac ±10%, 48 to 66 Hz, <20 VA, or ±15V dc ±2%, typically 150 mA (−15V) and 300 mA (+15 V), ripple <5 mV pk-pk.
**TEMPERATURE:** All specifications apply over the temperature range 0°C to 55°C.
**WEIGHT:** 6 kg (13 lb).
**DIMENSIONS:** 89 mm H × 425 mm W × 350 mm D (3.5 × 16.8 × 13.9 inches)
**PRICE IN U.S.A.:** $1720.

### HP Model 3755A Access Switch Controller

**FREQUENCY RANGE:** 10 kHz to 25 MHz.
**INSERTION LOSS:** <0.1 dB (input and output on rear panel); <0.2 dB (input and output on front panel).
**RETURN LOSS:** >30 dB (rear panel, 60 kHz to 25 MHz).
**NOISE POWER RATIO:** >70 dB typical for −10-dBm total power applied over any 8-MHz band.
**CONNECTOR TYPE:** 75Ω BNC standard. Other types and impedances are available.
**POWER:** 100, 120, 220, 240 Vac ±10%, 48 to 66 Hz, <20 VA.
**TEMPERATURE:** All specifications apply over the temperature range 0°C to 55°C.
**WEIGHT:** 5 kg (11 lb).
**DIMENSIONS:** 89 mm H × 425 mm W × 350 mm D (3.5 × 16.8 × 13.9 inches)
**PRICE IN U.S.A.:** $1440.

### 3754A/3755A Combination—General Data

**CONNECTION TIME** (nominal): 0.9 + (N × 0.05)s/switch (where N = input number).
**INPUT TERMINATION DISCONNECT TIME:** 0.5 ms (typical).
**ACCEPTABLE DC RESISTANCE OF TWO-WIRE PATH:** 100Ω between Access Switch and Controller, or between Switches.
**TYPICAL PERFORMANCE**
INSERTION LOSS (from the input of a single 3754A to rear panel of 3755A):
<0.1 dB (50 kHz to 10 MHz;
<0.15 dB (50 kHz to 20 MHz).
ISOLATION

| | Bandwidth | | | |
|---|---|---|---|---|
| | 4 MHz | 12 MHz | 18 MHz | 25 MHz |
| Any Input/Output | 105 dB | 100 dB | 95 dB | 90 dB |
| Any two inputs | 110 dB | 105 dB | 100 dB | 95 dB |

**MANUFACTURING DIVISION:** Hewlett-Packard Ltd.
South Queensferry
West Lothian EH309TG
Scotland

# Laboratory Notebook

## A High-Level-Language Microprocessor Prototyping and Debugging System Using a Desktop Computer

*Development of a microprocessor-controlled instrument is really two projects, one to develop the instrument hardware and another to develop the system software.*

*Hardware/software trade-offs during system development can be evaluated conveniently only if there exists a fast and simple way to write and change the software. An interpreter such as BASIC is ideal, but the time required to write the interpreter for the specific microprocessor may not be justifiable.*

*A better solution is to interface the microprocessor to a computer that already has an interpreter. The interface will consist of hardware and software and must make it possible for all of the microprocessor functions to be controlled by the external computer.*

*We have developed such a system of hardware and software to interface the 6800 microprocessor to HP desktop computers. The hardware consists of one 6820 Peripheral Interface Adapter (PIA), a few gates, and one interface card to the specific computer (see Fig. 1). The software is relocatable, making it independent of the specific memory allocation for the 6800 microprocessor.*

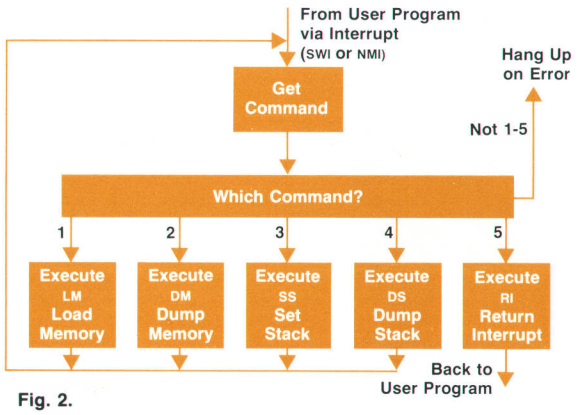



Fig. 2.

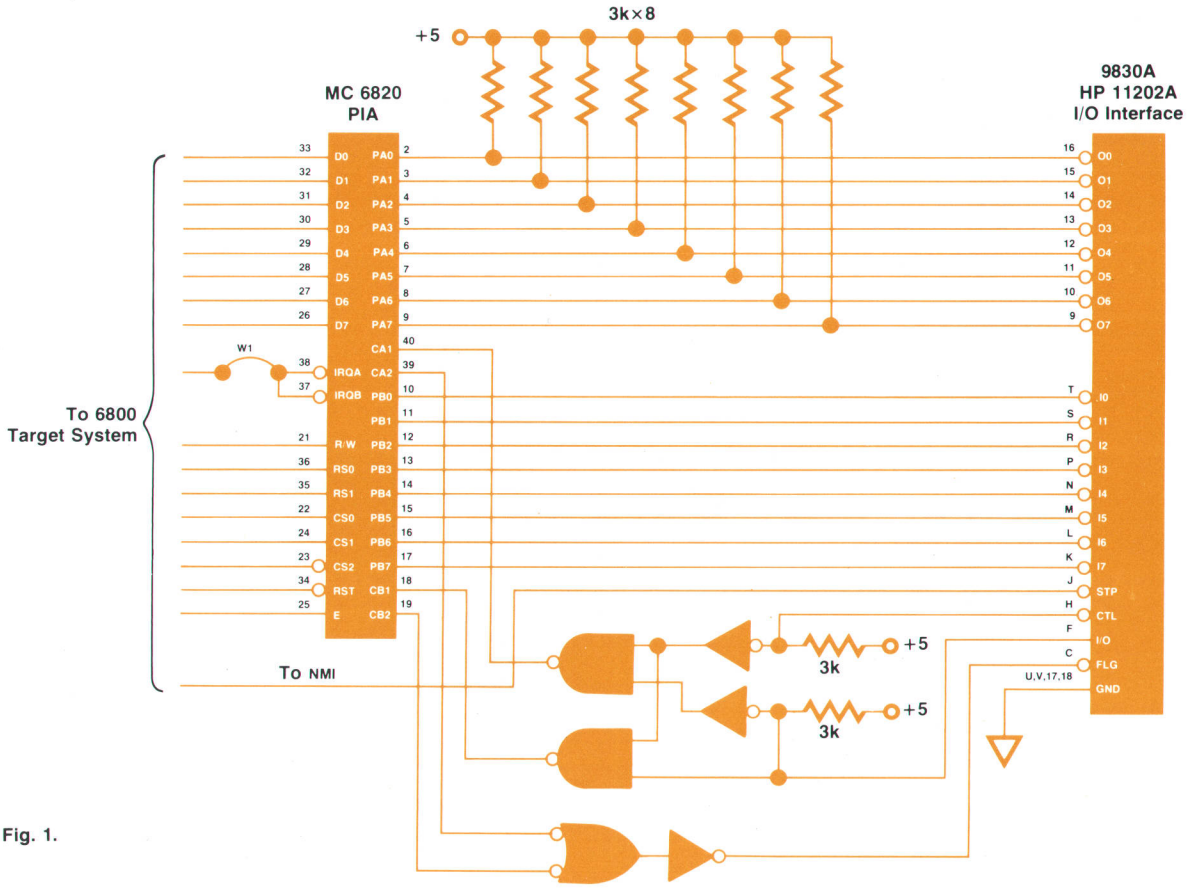



Fig. 1.

*Our system uses the BASIC language and an HP 9830A Desktop Computer. We have included a breakpoint register and a comparator that generates a non-maskable interrupt to the 6800 microprocessor when the contents of the microprocessor bus match those the user has placed in the register. This makes it possible to stop the program at any desired point.*

*The software is in two parts. The microprocessor runs a firmware monitor stored in its read-only memory (ROM). The computer runs a debug program written in BASIC. Shown on the next page is a listing of the monitor, written in 6800 assembly language. Given this program, any 6800 assembler will produce the code to be stored in the microprocessor's ROM. It is independent of the specific computer being used.*

*Fig. 2 is a flow chart of the monitor. It is organized to get a command, execute it, and get the next command. Each command is represented by a number from 1 through 5. The interchange of data between the 6800 and the computer is controlled by two subroutines: GETBY (get byte from computer) and WRTBY (write byte to computer). During power up, the PIA used to link the 6800 and the computer is initialized and the user program is executed.*

*Either a software interrupt instruction (SWI) or a non-maskable interrupt (NMI) is used to enter the get-command (GETCM) phase.*

*The computer software works in exactly the same way. Its get-command instruction requests an input from the computer keyboard and sends it to the 6800 for execution. The specific form of this program depends on the computer being used and for this reason the program is not shown here. However, because it can be developed interactively using a high-level language, it is not difficult to write. For example, it took us only three days to write the debug program in BASIC for the 9830A Computer. Later, another debug program was written for the HP 9825A Desktop Computer in only one day.*

*We have used this technique to develop and test the hardware and software for the 5370A Time Interval Counter, the 5359A Time Synthesizer, the 5342A Microwave Counter, and other instruments. Once the system is proven functional, we begin replacing the computer software by 6800 software. In the instruments mentioned, the hardware and software were modified to work through the HP-IB (IEEE 488) for troubleshooting purposes. We have also found this technique useful for collecting statistical data on an instrument's operation and for discovering failure modes during overnight runs.*

*We wish to thank Tom Coates and Mark Allen for the use of their cross-assembler and simulator system.*

*-Allen Foster*
*-Luiz Peregrino*

```
*PROGRAM FOR PIA INTERFACE TO HP 9830A (OR ANY OTHER) COMPUTER
*RAM ADDRESS $00 TO $FF WITH HOLES FOR PIA AND I/O INTERFACE
*ROM $7FFF TO $7C00; $XXXX TO $XXXX
*PIA ADDRESS 0000 TO 0007
*ADDRESS 0000 TO 0003 FOR INTERFACE
*ADDRESS 0004 TO 0007 FOR BREAK POINTER SET BY 9830A COMPUTER
*PIA RS0=NOTA0 ; RSI=NOTA1
*PIA A CONTROL REGISTER              A1=1;A0=0;(0000+2)
*PIA A PERIPHERAL DATA DIRECTION     A1=1;A0=1;(0000+3)
*PIA B CONTROL REGISTER              A1=0;A0=0;(0000+0)
*PIA B PERIPHERAL DATA DIRECTION     A1=0;A0=1;(0000+1)
*INTERRUPT AREA
        ORG $7FF8
        FDB GETCM   IRQ INTERUPT
        FDB GETCM   SOFTWARE INTERRUPT
        FDB GETCM   NMI NOM MASKABLE INTERRUPT
        FDB START   RESET POINTER
*
*  IRQ MUST BE GETCM IF HARDWARE INTERRUPT DESIRED
*  START MUST INITIALIZE PIA
*
***** INTIALIZE PIA  *****
        ORG $7F00
START LDS #STACK   STACK POINTER
*
*
STACK EQU $FF   STACK POINTER
PICRA EQU $0002
PICRB EQU $0000
PIDRA EQU $0003
PIDRB EQU $0001
*
*
        CLRA
        STAA PICRA
        STAA PICRB
        STAA PIDRA SET PA0 TO PA7 AS INPUT
        COM A
        STAA PIDRB SET PB0 TO PB7 AS OUTPUT
        LDAA #%00101100 NEG TRANS. NO INTERRUPT PULSE MODE
        STAA PICRA
        STAA PICRB
        LDAA PIDRA    CLEAR CRA7
        LDAA PIDRB    CLEAR CRB7
*
*  USER PROGRAM BEGINS HERE
*     SWI    TRANSFER TO GETCM
*
*  ENDS HERE
*
GETCM BSR GETBY    GET COMMAND
EXCM  CMPA #$1
        BEQ LM    LOAD MEMORY
        CMPA #$2
        BEQ DM    DUMP MEMORY
        CMPA #$3
        BEQ SS   SET STACK POINTER
        CMPA #$4
        BEQ DS   DUMP STACK POINTER
        CMPA #$5
        BEQ   RI   RETURN FROM INTERRUPT
        BRA * HANG UP ON ERROR
*
LM      BSR GETAD    LOAD MEMORY
        BSR GETBY
        TAB  B=#BYTES     0<B<256   IF B=0 LOAD 256 BYTES
LM1     BSR GETBY    GET BYTE TO STORE
        STAA X
        INX
        DECB
        BNE LM1     NOT FINISHED
        BRA GETCM
*
DM      BSR GETAD    DUMP MEMORY
        BSR GETBY
        TAB  B=#BYTES TO DUMP 0<B<256   IF B=0 THEN 256
DM1     LDAA X
        BSR WRTBY
        INX
        DEC B
        BNE DM1
        BRA GETCM
*
SS      BSR GETAD    SET STACK POINTER
        INX
        TXS
        BRA GETCM
*
DS      TSX   DUMP STACK POINTER
        DEX
        DEX
        STS X
        DES
        DES
        PULA
        BSR WRTBY
        PULA
        BSR WRTBY
        BRA GETCM
*
RI      RTI   RETURN FROM INTERRUPT
*
GETAD   BSR GETBY   GET ADDRESS
        TAB       B=ADH
        BSR GETBY A=ADL
        PSHA
        PSHB
        TSX
        LDX X
        PULB
        PULA
        RTS
*
GETBY   TST PICRA   GET BYTE FROM COMPUTER
        BGE GETBY
        LDAA PIDRA
        COM A
        RTS
*
WRTBY   TST PICRB   WRITE BYTE TO COMPUTER
        BGE WRTBY
        PSHA
        LDAA PIDRB     CLEAR CRB7 READY FOR NEXT REQUEST
        PULA
        COM A
        STAA PIDRB
        RTS
*  END OF MONITOR
```

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

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**Technical Information from the Laboratories of Hewlett-Packard Company**

Hewlett-Packard Company, 1501 Page Mill Road
Palo Alto, California 94304 U.S.A.
Hewlett-Packard Central Mailing Department
Van Heuven Goedhartlaan 121
Amstelveen-1134 The Netherlands
Yokogawa-Hewlett-Packard Ltd., Suginami-Ku
Tokyo 168 Japan

**Editorial Director • Howard L. Roberts**
**Managing Editor • Richard P. Dolan**
**Art Director, Photographer • Arvid A. Danielson**
**Illustrator • Susan E. Wright**
**Administrative Services, Typography • Anne S. LoPresti**
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On-line curator: John Miles, KE5FX

jmiles@pop.net