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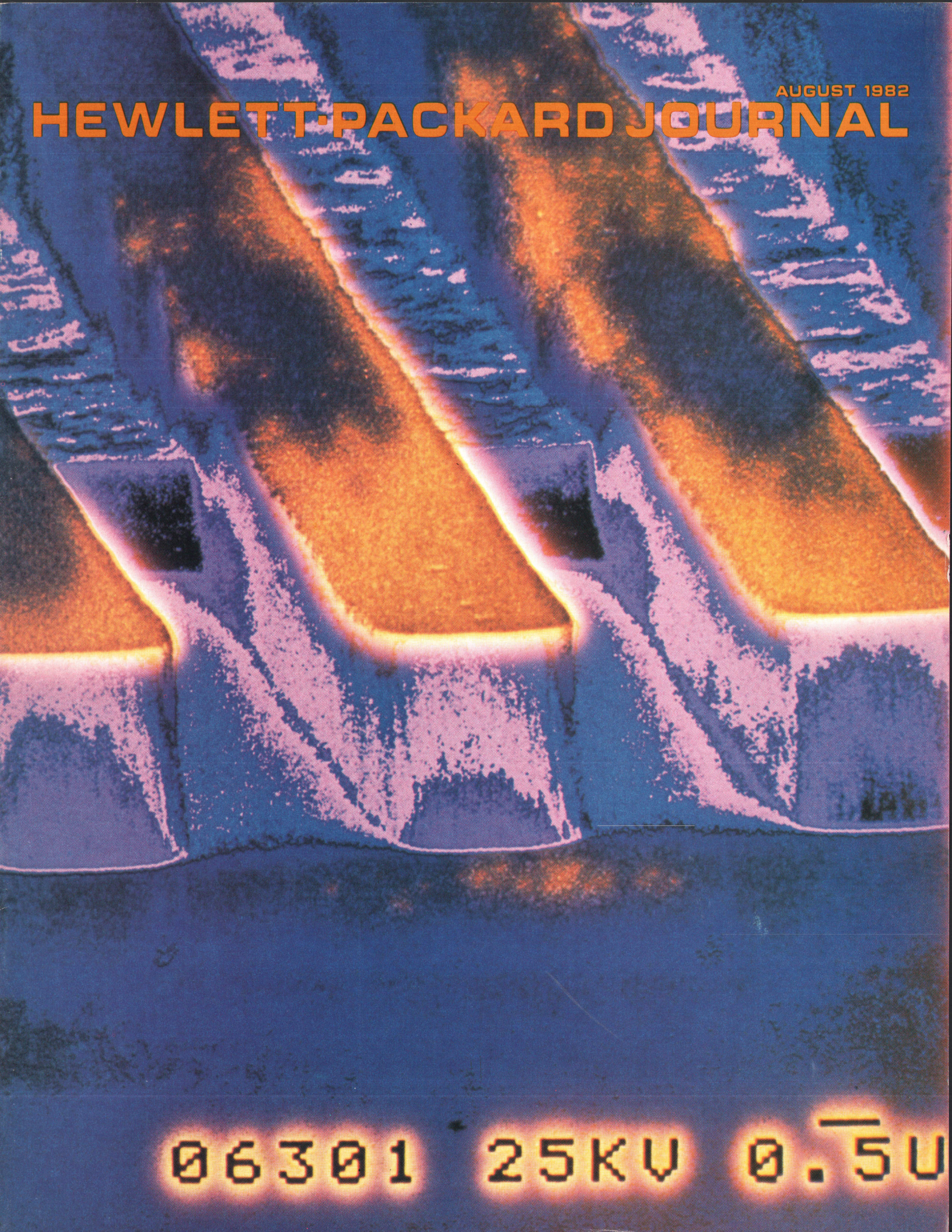

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Technical Information from the Laboratories of Hewlett-Packard Company

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The application of silicon integrated circuits has become pervasive in almost all human activities. It is expected that this pervasiveness will continue to expand at least through the end of this century, characterized by higher and higher levels of integration—more and more transistors in the same silicon area. We are entering the era of VLSI—very large-scale integration—which means hundreds of thousands of devices on a single chip of silicon. One of the key driving forces behind this trend is the rapid, exhilarating development of the process technologies required for fabricating VLSI circuits. Remarkable advances have been implemented in manufacturing that were believed to be impossible a few short years ago.

In this issue, a number of the process technologies currently being explored at Hewlett-Packard are described. The strong interdisciplinary nature of these evolving technologies is readily apparent and will be more extensive in the future. With critical dimensions in some cases approaching several atomic layers, the intricacy of these processes is increasing and we will in the next 5 to 10 years begin to see the limits of some technologies defined and perhaps approached. Until then, the cramming of more features on a chip to get higher performance with less power dissipation will continue at a rapid pace.

Cover: A solarized version of Fig. 8, page 8.

-Frederic N. Schwettmann, Guest Editor

IC Process Technology: VLSI and Beyond

by Frederic N. Schwettmann and John L. Moll

THE VLSI ERA is here. Integrated circuits containing over 100,000 devices with 1-to-2-micrometer feature sizes have become a manufacturing reality. A prime example of the power of this technology is the demonstration of a 450,000-device, 32-bit microcomputer operating at a clock rate of 18 MHz.[1] This remarkable accomplishment is the result of the congruence of advances in design automation, process technology, packaging and testing. In the field of process technology, significant achievements have been demonstrated in lithography, etching, interconnections, materials and low-temperature processing. Now that VLSI has become a reality, where and how far the technology can be extended are key questions facing researchers the world over.

Device Scaling

The presently available processing capability of defining dimensions as small as 1 to 1.5 micrometers will be driven down to even smaller sizes. The general device performance guideline of constant-field scaling* has been followed as metal-oxide-semiconductor (MOS) device dimensions are reduced, but with significant violations. The average voltage drop per micrometer along the device channel has increased somewhat, and the maximum electric field in the gate dielectric has increased. In addition, the channel length has decreased faster than the junction depths for the source and drain regions. The result is that from time to time new physical phenomena need to be included in describing device operation and electrical characteristics, and in determining the sensitivity of circuit operation to process variations.

Up to this time, scaling of both lateral and vertical dimensions has been advantageous, both to functional integration and to circuit performance. As the dimensions become less than one micrometer the performance advantage will become more difficult to maintain. Parasitic resistance will increase, and as chips become more complex, parasitic capacitance will be more difficult to control. A lower operating voltage tends to reduce noise margin and places greater demands on process control. There is in fact a probability that at some minimal dimension, performance will peak, limited by parasitic effects and unscalable parameters such as operating temperature and subthreshold conduction.

An often asked question is "What are the minimum usable line and space sizes for silicon VLSI?" A proposed answer for the minimum feature, both in an MOS device and in interconnect lines, is approximately 0.25 micrometer. Thermodynamic and quantum-mechanical effects begin to limit device and circuit performance at sufficiently small dimensions. There are more pragmatic considerations, such as the previously mentioned parasitic effect on performance, and limitations in the perfection and control of fabrication processes. The cost of building and maintaining a facility to achieve the necessary degree of control for submicrometer VLSI will certainly far exceed present-day factory costs.

There are still a number of "aces in the hole" that make the ultimate scaling and performance of silicon VLSI a moving target. The discussion to this point has centered around MOS switches built in the self-aligned silicon gate configuration. There are possible process inventions that could, for example, significantly reduce the parasitic and interconnect limits (see article on page 31 and box on page 33). Device inventions such as multilevel films of active devices could also affect system architecture. There is so much activity in both new processes and new device configurations that any attempt to report all of the efforts would fall far short of the mark.

*Constant-field scaling means that if, when the physical dimensions of a device are reduced, the operating voltages and currents are also reduced so that the electric fields within the device remain constant, performance should remain the same. In practice this is difficult to do because of the need for a standard operating voltage.

Lithography

The dominant lithographic technology currently used in IC manufacturing is the 1:1 optical projection printer. This tool allows geometries as small as two micrometers and affords high wafer throughput. Below two micrometers, the trend has been to step-and-repeat exposure systems. In addition to better resolution, these tools provide greater alignment accuracy. As a general guideline, the layer-to-layer registration is targeted to be no worse than 0.25 times the minimum resolvable feature size. Therefore, for a 1-μm technology, the layer-to-layer registration should be better than ± 0.25 μm, a value well within the capability of a state-of-the-art step-and-repeat system. It is expected that as the numerical aperture of the lenses used in the optical system is increased and the wavelength of the exposing light is decreased, a real limit of 0.5 μm for refractive optics will be approached. Crucial to the success of optical systems in the submicrometer regime is the use of a multilayer resist technology (see article on page 5). Much effort is being expended in this area to extend the usable range of optical systems. Higher contrast resists such as those using inorganic materials may ultimately replace the organic photoresists now in common use.

At 0.5 micrometer and smaller, X-ray and electron beam lithography are the contenders. Electron beam has demonstrated fine-line capability and possesses excellent alignment potential. However, throughput is currently lower than for optical systems and the cost is considerably higher. X-ray, on the other hand, has excellent resolution capability and the potential for higher throughput (see article on page 14). For dimensions less than 0.5 micrometer, step-and-repeat systems would be required to achieve the desired overlay accuracy. This eases the mask fabrication problems, but requires that a more intense source of X-rays be used and/or a more sensitive resist developed. Clearly, much technological progress is required.

Etching

Once a pattern has been defined in the resist, it must be faithfully reproduced in the underlying layer. Before the advent of VLSI, etching was usually done with wet chemistry. This technology almost always has the virtue of nearly infinite selectivity (ability to etch one material without affecting another material), but is isotropic. For geometries greater than two micrometers, this is not a significant problem. However, when etching a 1-μm-wide pattern in a layer that is 0.5-μm thick, the lateral portion of isotropic etching completely destroys the pattern. For most VLSI applications and all future submicrometer work, anisotropic etching will be essential. The use of dry plasma processes has emerged as the primary etch technology (see article on page 19).

The transition from wet to dry etching has been difficult. The required equipment (see box on page 22) is more complex, more expensive and has lower wafer throughput when compared to wet etching. In addition to anisotropy and good selectivity, sloped sidewalls are required to provide conformal step coverage for subsequent layers. The task is to find the right combination of gases and process conditions to match the requirements. An enduring significant problem is the lack of understanding of the mechanisms associated with anisotropy, etch rate and selectivity. Much work is

required in this area.

Interconnections

As the speed of individual devices increases, the time delays associated with the interconnections begins to play a significant role in circuit performance. As the minimum feature size is decreased, the area of the interconnect and the contact area become smaller. The time delay is dependent on the resistance of the interconnections and the capacitance controlled primarily by the dielectric layer. The dielectric material in most cases is either silicon dioxide or silicon nitride.

For the device interconnections, a variety of materials are available. Refractory metal silicides on top of polysilicon are gradually replacing polysilicon as a first-level interconnect material. An order-of-magnitude decrease in resistivity is gained by this approach. More emphasis is now being placed on two levels of metallization on top of the polysilicon or polycide layer. This provides greater flexibility for the circuit designer, but adds to the manufacturing difficulty. Three or more levels of metallization are expected to become more common as experience is gained. Aluminum alloy metallization is currently used in almost all VLSI applications. As contacts to diffused areas with shallower junctions are required, barrier layers such as tungsten will be added to prevent spiking* through the junctions. To decrease the contact resistance (contact area decreases, and hence resistance increases as the square of the scaling factor), silicide layers such as platinum silicide may be required.

An additional factor, electromigration (see article on page 28), becomes important for circuit reliability as the conductor cross-sectional area decreases and current density increases. This requirement may result in the replacement of aluminum alloys with materials such as tungsten. However, the higher resistivity of tungsten, about four times higher, results in another tradeoff between performance and reliability.

Materials

Another area expected to be of great concern in the submicrometer region is the silicon material itself. Already great care is being given to tighter control on the specifications of substrates. The amount, distribution and chemical bonding of silicon impurities such as oxygen and carbon are being carefully monitored and their effect on device performance evaluated. The coupling of these species to the defects generated during processing is a major concern. A variety of gettering schemes are being studied and implemented where needed. The tools for characterizing defects on a near-atomic level, such as scanning transmission electron microscopy (STEM), are now available and are being brought to bear on the problems with remarkable results. There is much optimism on being able to understand and control the location of defects in silicon.

One novel approach to forming a substrate, discussed in the article on page 10, is the use of an intense laser or electron beam to melt a polysilicon layer and then let it cool and recrystallize into large-grain polysilicon suitable for device fabrication.

Low-Temperature Processing

The requirements of shallow junctions in scaling and the need for the minimum lateral motion of dopants requires that processing temperatures be kept as low as possible. Instead of applying energy to deposition and growth processes by thermal means alone, plasma excitation will be used (see article on page 24). Already, deposition of silicon dioxide and silicon nitride by plasma techniques is available for manufacturing processes. Films deposited using plasma excitation tend to exhibit better step coverage than purely thermally deposited films. Interest is now high in being able to deposit conducting materials such as aluminum and tungsten using plasma techniques.

The growth of thin films in a plasma as opposed to deposition is a new and exciting area. Gate dielectrics of silicon nitride and nitrided silicon dioxide show promise for scaled devices requiring dielectric layers less than 10 nm thick (see box on page 26). They exhibit better physical durability, lower etch rates and lower defect densities. Much work needs to be done to understand the growth mechanisms and implement these films in the manufacturing environment.

Another approach that will be useful in lowering processing temperatures is high-pressure oxidation (see article on page 34). This could be a useful tool in the submicrometer regime.

In summary, while design tools are still lagging the available process technology, the march toward smaller devices and circuits continues at a furious pace. It is expected that by the turn of the century, the ultimate limits in silicon will have been clearly demonstrated and maybe attained. Many challenges remain and opportunity exists for contribution and innovations in almost all engineering disciplines in reaching this goal.

*Enhanced diffusion of the contact metal in a localized area of the underlying semiconductor material resulting in an electrical short across a device junction.

Reference

1. J. Beyers, et al, "A 32b VLSI Chip," Digest of Technical Papers, Vol. 24, IEEE International Solid-State Circuits Conference, February 1981, THAM 9.1.

Frederic N. Schwettmann

Fred Schwettmann is the director of HP's Integrated Circuit Laboratory. His work has resulted in over 20 publications and presentations related to IC technology, and three patents, two on semiconductor technology, the other on petrochemical processing. He joined HP in 1976 with several years of experience in semiconductor and petrochemical R&D. Fred is the national vice chairman of new technologies for the Electrochemical Society and a member of the VLSI program committee of the IEEE. He was born in Brooklyn, New York and studied chemical engineering at the City College of New York, earning a BS degree in 1961, at New York University, earning an MS degree in 1964, and at City University of New York, earning a PhD degree in 1969. Fred is married, has two children, and lives in San Jose, California. He enjoys running, playing racquetball and basketball, and sports in general. During his college days, Fred was voted "All-American" in lacrosse and was selected as most-valuable player for two years.

John L. Moll

John Moll has been with HP since 1974, first as the director of technology for the IC lab, and most recently as the manager of the ICSR lab and a senior scientist with HP Laboratories. He is well-known to circuit designers for the Ebers-Moll model of the large-signal behavior of transistors, has been on the faculty of Stanford University, and has extensive experience researching solid-state devices and the physics of solids. John's contributions have resulted in over 100 papers, ten patents, and a book, *Physics of Semiconductors*. He was a Guggenheim Fellow in 1964 and received the Howard N. Potts award from the Franklin Institute in 1967 and the Ebers award from the IEEE in 1971. He is a Fellow of the IEEE and a member of the American Physical Society, National Academy of Engineering, and Sigma Xi.

Optical IC Lithography Using Trilayer Resist

A composite photoresist layer reduces exposure effects that degrade pattern definition and reduce resolution in optical IC lithography.

by Michael M. O'Toole, E. David Liu, and Gary W. Ray

THE DENSITY AND PERFORMANCE of devices contained in today's VLSI circuits are primarily determined by the resolution capability of the lithographic technique used for the circuits' manufacture. The dominant technology uses an optical projection system to form an image of the desired pattern on the photoresist-covered surface of a silicon wafer. The theoretical image resolution limit of the lens systems in modern projection aligners is in the submicrometer range. However, the resolution obtainable in normal IC production is much poorer because of various resist and substrate surface effects.

To achieve dimensional control closer to the theoretical resolution limit of the projection system, a trilayer resist process has been developed. Before describing this process, it is useful to discuss the effects that degrade image resolution in conventional processing.

In an ideal situation, the image projected on a planar, nonreflective surface covered with positive resist will consist of perfectly dark lines, corresponding to the desired features, surrounded by evenly illuminated areas where the resist is exposed and later developed away. In typical IC fabrication, however, the image is projected onto a nonplanar reflective surface that is unevenly covered with resist. The nonplanar reflective surface provides the conditions for two effects that limit the usable resolution of a projection aligner. The bulk effect is caused by large thickness variations of the resist near abrupt changes (steps) in the surface topography. The standing-wave effect is caused by multiple reflections of the exposure illumination from the substrate surface.[1]

The bulk variation in the resist thickness as it covers a step is shown in Fig. 1. The resist layer on top of the step is thinner than it is next to the step and, in general, requires less exposure to be developed to the desired linewidth. As a result of the standing-wave effect, variations in the thickness of the resist or any thin semitransparent layers under the resist can cause large variations in the exposure energy coupled into the resist. This effect is periodic within the thickness of a layer. The period is $\lambda/2n$, where λ is the wavelength of the illumination and n is the index of refraction of the layer material. Even a small thickness variation of 0.65 micrometer can cause a major exposure variation. Both effects are most evident for resist feature dimensions approaching the resolution limit of the projection lens.

The standing-wave and bulk effects may be studied by using a computer program for the simulation of optical projection printing.[2] The program assumes diffraction-limited optics, considers the numerical aperture of the imaging lens, the imaging wavelength, the partial coherence factor of the illumination system, and the focus error, and calculates the image intensity pattern for a specified feature on the surface of the resist. The exposure and development of the resist are calculated by using the model described by Dill, et al.[3] This model considers the substrate's topography and the characteristics and thickness of the resist. The final output is a simulated line edge profile in positive resist.

A sample output of the simulation program is given in Fig. 2, which shows the nominal exposure required for a periodic 1-μm-wide line-and-space pattern as a function of positive resist thickness on (a) a silicon substrate, and (b) an aluminum substrate. The nominal dose is defined as the exposure energy density required to replicate the mask linewidth in the resist. The bulk effect causes the gradual rise of the curve, and the standing-wave effect causes the periodic variation. The period $\lambda/2n$ is 128 nm for an exposure wavelength of 436 nm and a resist refractive index of 1.69. To compensate the standing-wave effect caused by a 64-nm thickness variation in a 1-μm-thick layer of positive resist on a silicon substrate, a 25% exposure difference is required. A similar exposure difference is required to cor-

Fig. 1. *Resist step coverage: 1-μm-thick resist pattern over 0.5-μm-high step.*

*Some of the data presented in this article has been previously discussed by the authors at the 1981 Symposium on VLSI Technology in Maui, Hawaii and in articles published in the November, 1981 issue of the IEEE Transactions on Electron Devices and the May, 1982 issue of Solid State Technology.

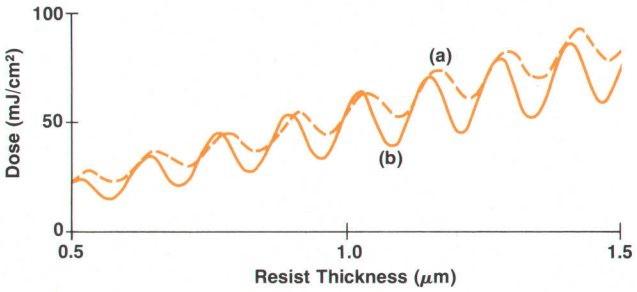

Fig. 2. *The exposure energy density (dose) required at a wavelength of 436 nm to achieve 1-μm-wide lines and spaces in HPR 204 positive resist on (a) silicon and (b) aluminum surfaces for numerical aperture NA=0.28, perfect focus, and partial coherence factor σ=0.7.*

rect for the bulk effect caused by a 250-nm resist thickness variation. From curve b of Fig. 2, a bulk thickness variation of about 420 nm is equal to a standing-wave thickness variation of 64 nm. Both effects can combine near a step to produce a significant variation in the nominal exposure dose required, causing severe linewidth control problems. Fig. 3 shows a microphotograph of 1-μm-wide lines and spaces patterned in a 1-μm-thick layer of positive resist over two 0.5-μm-high polysilicon lines. The resist linewidth is very unstable near the edge of the steps and narrower on top of the polysilicon lines than in the lower field areas around them.

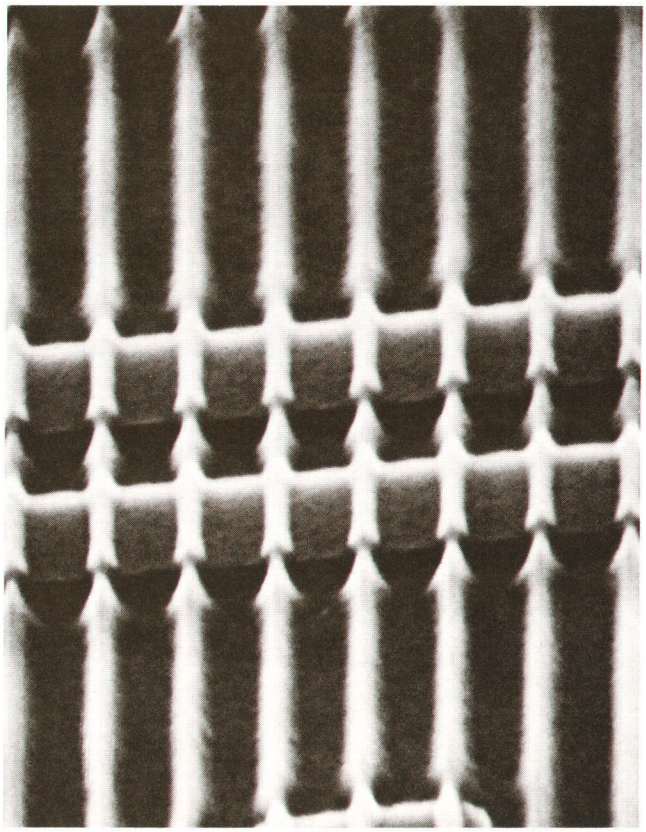

Fig. 3. *1-μm-wide lines and spaces in 1 μm of resist over 0.5-μm-high polysilicon steps.*

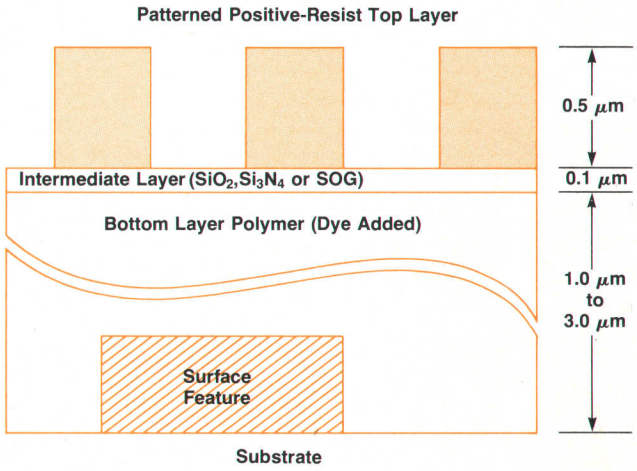

Fig. 4. *Trilayer resist system.*

Trilayer Resist Process

To realize the maximum resolution from a projection aligner, the surface of a wafer must behave as if it were planar and nonreflecting. In an attempt to achieve this condition, several multilayer resist processes have been recently proposed and demonstrated.[4-9] In a multilayer system, the substrate's topography is planarized by a thick bottom polymer layer. Optical reflections from the underlying surface topography can be eliminated by choosing an absorptive material for the bottom layer.

Fig. 4 illustrates the trilayer structure studied by Hewlett-Packard Laboratories. An absorbing polymer, one to three micrometers thick, is used to planarize the substrate topography. The planarized surface can be coated uniformly by the top resist layer, thus suppressing the bulk effect. The absorption of the exposure illumination by the bottom polymer layer eliminates reflections from the substrate topography and reduces the standing-wave effect. An intermediate inorganic layer serves as a mask during reactive-ion-etching to transfer the top resist layer pattern to the bottom layer. The intermediate layer also prevents mixing of the top and bottom layer polymers.

Suitable materials for the bottom layer are polymers that planarize well. Transparent polymers may be made absorbing by adding dye. The dye must dissolve in the polymer and absorb strongly at the exposure wavelength. To simplify processing, the dye should be transparent at the alignment wavelength, allowing easy detection of the alignment mark through the thick bottom polymer layer.

Several materials have been used for the intermediate layer. Plasma-enhanced chemical-vapor deposition (PECVD) of silicon nitride done at room temperature is suitable (see article on page 24). Spin-on glass (SOG) has also been used as a suitable intermediate layer.[10] Because SOG can be applied by IC production equipment very similar to that used to apply resist, the use of SOG for the intermediate layer makes it easier to incorporate the trilayer process into an IC production facility. Both PECVD nitride and SOG permit rework of the top resist layer without having to strip the intermediate and bottom polymer layers.

Pattern transfer from the top resist layer to the inter-

mediate layer is achieved by plasma etching. If SOG is used for the intermediate layer, a CHF_3/CO_2 gas mixture is used. The SOG pattern is transferred to the bottom polymer layer using an anisotropic oxygen plasma etch process.

The trilayer process was analyzed and optimized using simulations generated by the computer program mentioned earlier. Positive resist was used for the top and bottom layers and was developed using a conventional batch process. The exposure and development parameters for the positive resist were measured at Hewlett-Packard Laboratories[11] using equipment similar to Dill's for the exposure parameters and to Meyerhofer's[12] for the development parameters.

In addition to the optical parameters of the aligner and the exposure and development parameters of the resist, the computer simulation of the trilayer system considers the refractive indexes of the materials and thicknesses of the various layers. Fig. 5 shows the calculated nominal dose required to print 1-μm-wide lines and spaces as a function of the thickness of the bottom polymer for the trilayer system of Fig. 4 on an aluminum substrate. Curve a assumes the absorption of HPR 204 positive resist and curve b assumes the absorption of this resist with dye added.

If the bottom polymer layer does not sufficiently planarize the substrate surface, the top layer of resist will disperse nonuniformly. Curves a and b of Fig. 6 show the calculated linewidth as a function of top resist thickness for two bottom polymer thicknesses of 1.03 μm and 0.95 μm. These two thicknesses represent the two extremes near 1 μm of curve a in Fig. 5. In both cases, the simulated exposure dose has been adjusted to produce a 1-μm-wide line for a 0.5-μm-thick top resist layer. Both the bulk and standing-wave effects are clearly seen. If the top resist layer is uniformly 0.5-μm thick, the nominal exposure required to maintain a one-micrometer dimension changes from 16 mJ/cm² for a 0.95-μm-thick bottom layer to 25 mJ/cm² for a 1.03-μm-thick bottom layer. This exposure variation is too great to achieve sufficient linewidth control over the entire wafer surface.

Adding dye to the bottom polymer of the trilayer process suppresses the standing-wave effect. Curve c of Fig. 6 shows the linewidth variation versus top resist layer thickness for a 1-μm-thick bottom resist layer with dye added. The linewidth variation is caused entirely by the bulk effect. Because positive resist used for the bottom polymer has been shown to planarize well,[13] the top resist thickness can be held to close tolerance, and good linewidth control is expected.

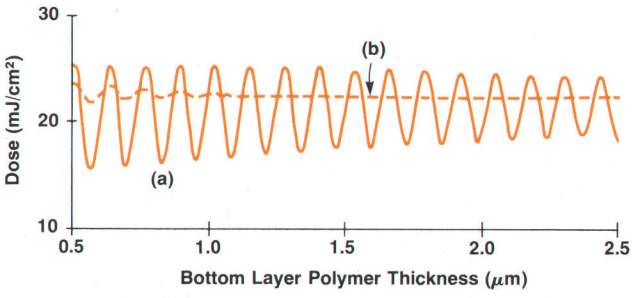

Fig. 5. *Nominal dose versus bottom polymer thickness for the trilayer system of Fig. 4 on an aluminum substrate using (a) HPR 204 positive resist and (b) HPR 204 containing 1.5% dye for the bottom polymer. Simulations are for 1-μm-wide lines and spaces under perfect focus conditions.*

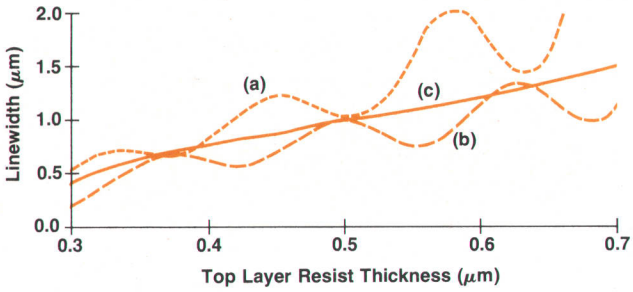

Fig. 6. *Simulated linewidth versus top resist layer thickness for 1-μm-wide lines and spaces for (a) a 0.95-μm-thick bottom layer of HPR 204 positive resist and an exposure dose of 16 mJ/cm² for the top layer of resist. (b) A 1.03-μm-thick bottom layer of HPR 204 and a 21-mJ/cm² dose for the top layer. (c) When dye is added to a 1.0-μm-thick bottom layer, the standing-wave effect on the linewidth in the top resist layer is eliminated.*

Experimental Results

A resolution test mask was used to print lines and spaces over topography using the trilayer system and a direct-

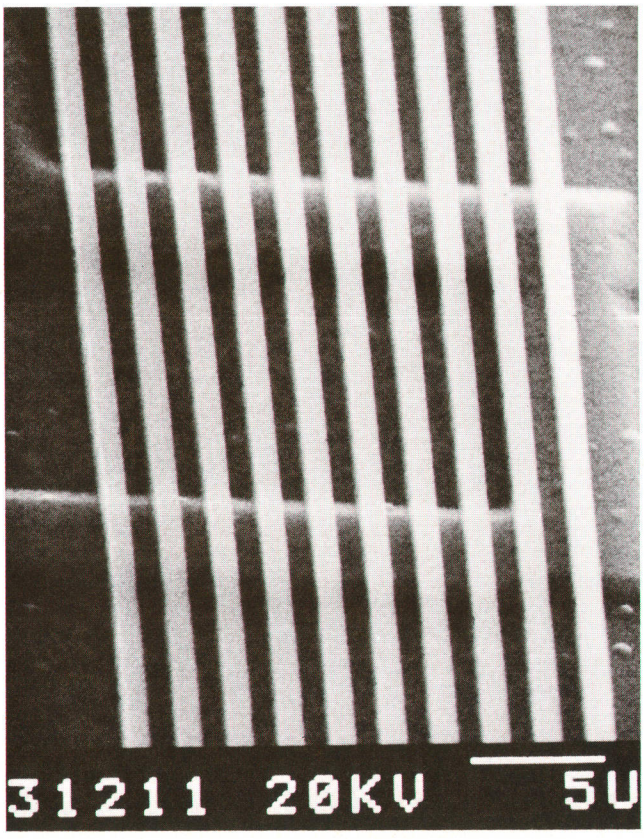

Fig. 7. *1-μm-wide lines and spaces in trilayer resist over 0.5-μm-high aluminum steps after reactive ion etch. 2.0-μm-thick HPR 204 positive resist containing 1.5% dye is used for the bottom polymer layer.*

step-on-wafer (DSW) 10:1 optical projection aligner with a numerical aperture of 0.28 and an imaging wavelength of 436 nm. Fig. 7 shows a scanning-electron-microscope (SEM) microphotograph of 1-μm-wide lines and spaces patterned with a trilayer process over 0.5-μm aluminized topography. Because the 2.0-μm-thick bottom resist layer planarizes the topography well, the thickness of the top resist layer is controlled to about ± 0.03 μm. The bulk effect is minimized and the standing-wave effect is eliminated. Because the wafer surface appears planar and nonreflective, excellent linewidth control of 1-μm-wide features over 0.5-μm-high steps is achieved.

Fig. 8 shows the straight sidewalls that are possible with this process. The bottom and intermediate layers in Fig. 8 were etched in a single pumpdown using a reactive-ion-etch system.

Future of Optical Lithography

Optical lithographic technology continues to evolve, both in equipment and in resist materials and techniques. Projection aligners with large numerical apertures, shorter imaging wavelengths, and better alignment capability are being designed. Future aligners[14] should have a theoretical resolution limit well into the submicrometer range and use sophisticated site-by-site autoalignment systems. In addition, new materials such as the inorganic resists[6,7,15] may be used in a multilayer resist system to further enhance the practical resolution of optical lithography.

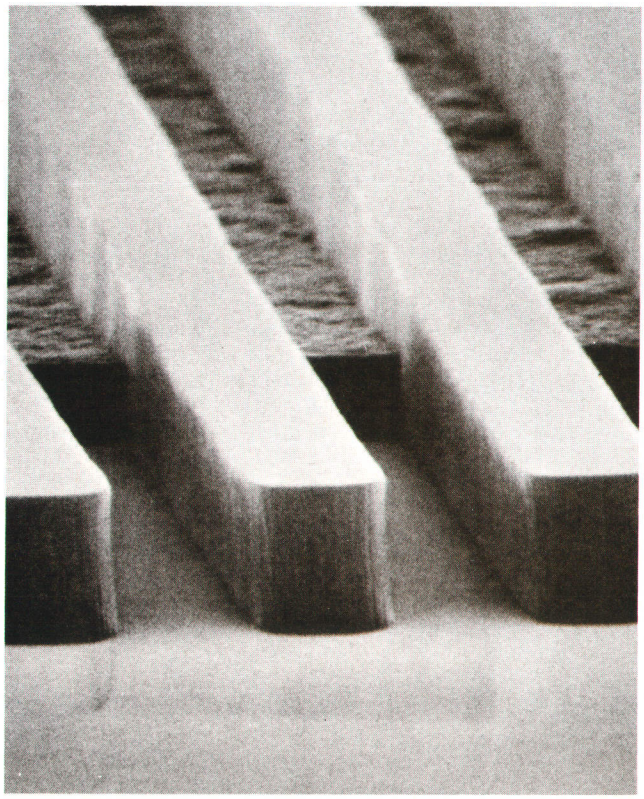

Fig. 8. *Edge profile of trilayer process using spin-on glass for the intermediate layer covering 1.0-μm-high aluminum steps. Profile is shown after reactive ion etching of bottom polymer layer.*

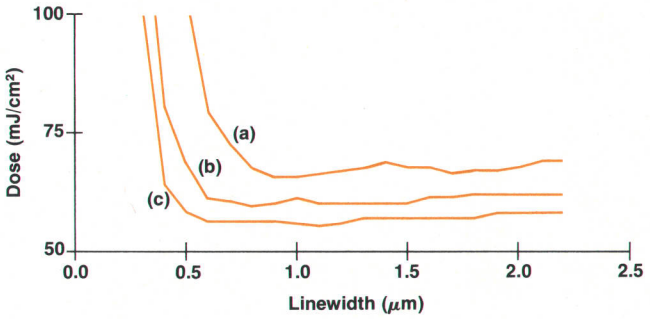

Fig. 9. *The nominal exposure dose as a function of linewidth in micrometers for (a) λ=436 nm, NA=0.28; (b) λ= 405 nm, NA =0.35; and (c) λ= 240 nm, NA=0.25 (σ=0.7, all cases). Simulation parameters (see reference 11): $A=0.57\ \mu m^{-1}$, $B=0.08\ \mu m^{-1}$, $C=0.01\ cm^2/mJ$, $F_1=0.179$, $F_2=-0.346$, $F_3=0.168$.*

In an ideal multilayer resist system, one where planarization is complete and substrate reflections are completely suppressed, the limits of optical lithography can be explored through computer simulation. The nominal exposure dose as a function of linewidth under perfect focus conditions for three combinations of numerical aperture and exposure wavelength is shown in Fig. 9. Curves a and b use parameters that roughly correspond to existing projection equipment. Curve c simulates a ficticious projection aligner that has an imaging lens with a numerical aperture of 0.25 and an imaging wavelength of 240 nm. The sudden rise in exposure dose for the smaller linewidths indicates a regime where IC process latitude degrades sharply. Operation in the crook of this regime is possible if a set of linewidth compensation rules for the larger linewidths is used.

A more explicit view of process latitude is given by Fig. 10 and Fig. 11, which give the fractional linewidth variation as a function of linewidth for a $\pm 5\%$ and a $\pm 10\%$ variation in exposure energy. Curves a, b, and c in Fig. 10 and Fig. 11 correspond to curves a, b, and c in Fig. 9. The calculated nominal dose for each linewidth in Fig. 9 was used to generate Fig. 10 and Fig. 11. The curves in Fig. 10 and 11 were calculated assuming a focus error equal to one-half of a "depth of field."

Current optical systems in conjunction with multilayer processing can probably achieve an effective exposure stability in this range. From curve b in both Fig. 10 and Fig. 11,

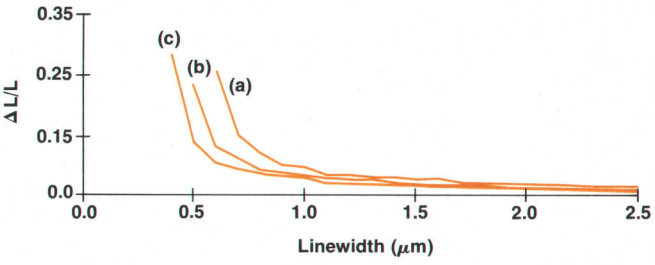

Fig. 10. *The fractional linewidth variation ($\Delta L/L$) as a function of linewidth in micrometers for a $\pm 5\%$ variation in exposure energy for the curves of Fig. 9. Each optical system was degraded by $\lambda/[4(NA)^2]$ of focus error.*

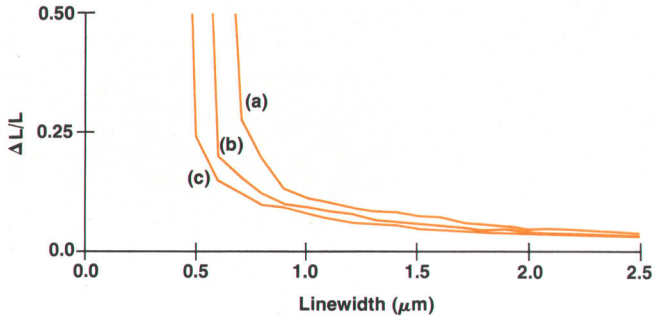

Fig. 11. *The fractional linewidth variation as a function of linewidth for a ±10% variation in exposure energy for the curves of Fig. 9.*

a projection aligner with a numerical aperture of 0.35 and an imaging wavelength of 405 nm should be able to print a 0.8-μm linewidth with 8% to 12% variation in size, using current microfabrication processes. Such an imaging system is commercially available today. As the imaging and alignment systems of optical lithographic equipment improve during the 1980s, production of VLSI circuits with submicrometer design rules should become a reality.

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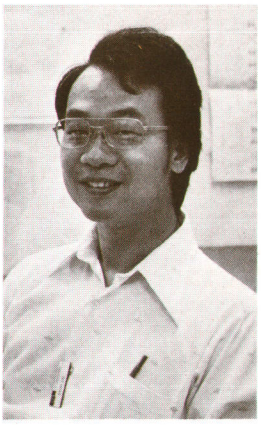
Gary W. Ray

Gary Ray received a PhD degree in chemical physics from Michigan State University in 1978 and did postdoctoral research at the Jet Propulsion Laboratory of the California Institute of Technology. His research work resulted in several papers on stratospheric chemical kinetics. He joined HP in 1981 and is studying plasma etching. Gary is married, has a daughter, and lives in Mountain View, California. His interests include backpacking, classical music, and early musical instruments.



E. David Liu

David Liu joined HP in 1979 with two years of experience in IC photolithography processing. He is now working on electron beam lithography and has co-authored three papers related to microlithography. David received a BS degree in chemistry from National Taiwan University in 1970 and a PhD degree in chemistry from the University of Chicago in 1976. He is a member of the American Vacuum Society, the Electrochemical Society and the Society for Photo-Optical Instrumentation Engineers. He is married, lives in Mountain View, California, and enjoys reading.

Michael M. O'Toole

Mike O'Toole is the leader of HP Laboratories' trilayer resist implementation project. He came to HP in 1979 after receiving a PhD degree in electrical engineering from the University of California at Berkeley. He has authored or co-authored nine papers on optical lithography and is a member of the IEEE and the Optical Society of America. Mike was born in Los Angeles, California, and now lives in San Jose, California. He has a private pilot's license and enjoys scuba diving.

Silicon Integrated Circuits Using Beam-Recrystallized Polysilicon

Melting a polysilicon layer by using an intense laser or electron beam can significantly improve the properties of the layer for semiconductor device fabrication. Novel vertical device structures can also be formed with this technique.

by Theodore I. Kamins

THE RECENT FABRICATION of metal-oxide-semiconductor (MOS) devices in layers of laser- or electron-beam-recrystallized polysilicon[1,2,3] offers the possibility of freeing integrated circuit structures from the constraints of conventional, single-crystal silicon technology.

While transistors fabricated in fine-grain polysilicon have marginally useful characteristics,[4] the behavior of devices in recrystallized polysilicon can approach that of transistors in single-crystal silicon. The new technology offers the promise of high-performance integrated circuits (ICs) fabricated on potentially inexpensive or insulating substrates,[5] as well as the possibility of additional levels of devices on monolithic silicon ICs. Combining levels of recrystallized polysilicon with single-crystal silicon can lead to novel vertical structures,[6] as well as increased component density.

This paper describes the characteristics of recrystallized polysilicon that make it useful for transistor fabrication and the behavior of the resulting devices. A recently fabricated complementary metal-oxide-semiconductor (CMOS) structure that incorporates these transistors is discussed along with potential future applications in three-dimensional integrated circuits and other uses.

Transistors in Recrystallized Polysilicon

During the past decade sporadic efforts have been made to fabricate MOS transistors with their active channels in layers of polysilicon[4,7] to allow additional flexibility in IC design and fabrication. However, transistors in fine-grain polysilicon have limited application because their threshold voltages are high and their carrier mobilities are low.[4] The transistor characteristics are limited by defect states primarily associated with the many polysilicon grain boundaries. If the number of grain boundaries and associated defect states can be greatly reduced, the transistor properties also improve. To reduce the number of boundaries, the grain size can be increased by melting the fine-grain polysilicon with a scanning, continuous-wave (CW) laser or electron beam (Fig. 1) so that it recrystallizes into large-grain material upon cooling.[8] The transistors fabricated in such material have characteristics approaching those of transistors in single-crystal silicon.

Hewlett-Packard's transistor-fabrication efforts in beam-recrystallized polysilicon have used techniques compatible with high-density, high-performance, MOS IC technology. Consequently, the transistors are fabricated with a state-of-the-art isolation process using local oxidation of silicon (LOCOS) suitably modified to account for the large-grain structure of the polysilicon.[2,3]

In the most straightforward demonstration of the transistor characteristics, devices are fabricated in polysilicon films deposited on silicon wafers uniformly covered with

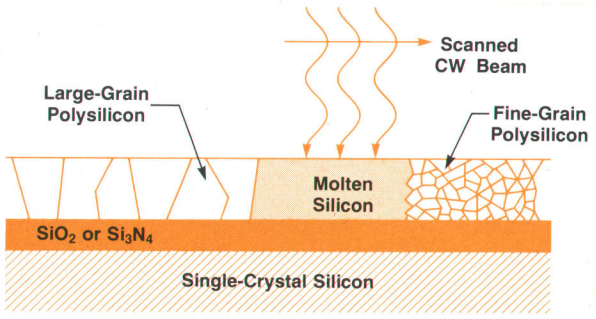


Fig. 1. *As an intense laser or electron beam scans across fine-grain polysilicon, the material melts, and then, as it cools, recrystallizes into large-grain polysilicon.*

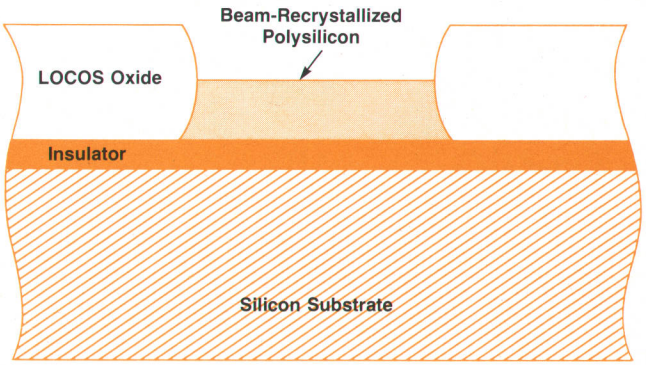


Fig. 2. *By oxidizing through the entire thickness of the exposed polysilicon areas, the recrystallized polysilicon is separated into isolated device regions surrounded by insulating films.*

insulating layers. The polysilicon is melted using an argon-ion CW laser to convert the initial fine-grain polysilicon to large-grain material (Fig. 1). A layer of silicon nitride is deposited over a thin stress-relief oxide layer and patterned to retain the nitride in the active device regions. The exposed polysilicon areas are oxidized until the growing oxide reaches the insulating layer beneath the polysilicon. Each device island of polysilicon is thus completely isolated from adjacent islands and from the substrate by insulating layers (Fig. 2). Alternatively, the polysilicon between device islands could be removed by etching.

The remaining steps of the transistor-fabrication process are similar to those used to form silicon-gate transistors in single-crystal silicon. A schematic cross section of a finished transistor is shown in Fig. 3. In some cases, the threshold voltage is adjusted by implanting boron or phosphorus through the gate oxide before the gate polysilicon is deposited. Ion-implanted source and drain regions are used and the heat treatment after these implantations is limited to avoid excessive diffusion.

Fig. 4 shows the source-drain characteristics of large- and small-geometry, n-channel, recrystallized polysilicon transistors, as well as single-crystal-silicon and fine-grain polysilicon devices. The kink in the current-versus-voltage characteristic arising from the presence of the insulator under the channel region is clearly seen for the large-geometry transistor. Some p-channel transistors have also been fabricated, and transistors with effective channel lengths as short as 1 μm have been obtained. Transistors in polysilicon recrystallized using an electron beam have characteristics similar to those in laser-recrystallized polysilicon.[3]

Use of Beam-Recrystallized Devices in Silicon ICs

The characteristics of recrystallized polysilicon transistors can be useful in many IC applications that normally use single-crystal-silicon transistors. The carrier mobilities are generally about half those of single-crystal transistors, but about five to twenty times larger than those of transistors in fine-grain polysilicon (Table I). The threshold voltages of the recrystallized transistors are only slightly greater than those of single-crystal transistors, rather than being 10 or

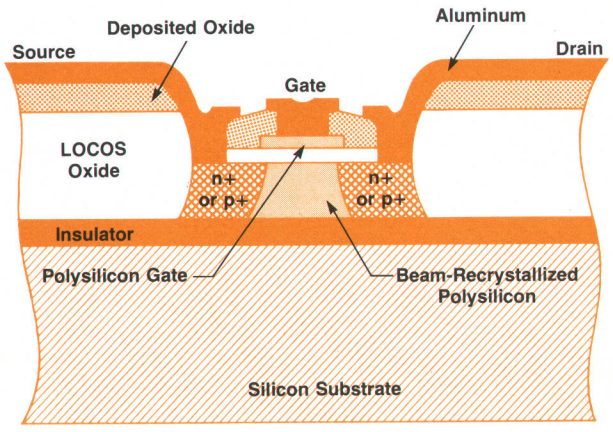


Fig. 3. *Schematic cross section of a transistor fabricated in recrystallized polysilicon.*

Table I
Characteristics of MOS Transistors Fabricated in Single-Crystal Silicon and Polysilicon

	n-Channel		p-Channel	
	Mobility (cm^2/V-s)	V_T (V)	Mobility (cm^2/V-s)	V_T (V)
Single-crystal silicon	670	1	180	−1.5
Laser-recrystallized polysilicon	300	1 to 2	120	−2
Fine-grain polysilicon	≈10 to 20	≈10 to 20	≈20	≈−10 to −20

20V higher, as in fine-grain polysilicon transistors. In addition, the source-to-drain leakage current of transistors with short (1 to 2 μm) channels is in the range of 10^{-13} amperes per micrometer of channel width, not very different from that of single-crystal transistors.

Once discrete transistors and simple ring oscillators had been fabricated in recrystallized polysilicon on silicon wafers uniformly covered with insulating layers, we wanted to combine the polysilicon transistors with those fabricated in adjacent regions of single-crystal silicon. In one potentially beneficial application, p-channel transistors can be fabricated in recrystallized polysilicon and combined with high-performance, n-channel transistors in adjacent regions of the single-crystal silicon substrate to form a CMOS integrated circuit.

CMOS ICs are becoming increasingly important for the realization of low-power, high-speed functions. While CMOS is generally easy to use, the possibility of latch-up (undesirable large lateral current flow between adjacent complementary devices triggered by some circuit conditions), and the resulting loss of circuit control, may restrict its use. The various techniques that have been used to minimize latch-up may significantly increase the chip size and are, consequently, less than ideal.

Completely separating the two polarities of devices by use of oxide layers totally avoids latch-up, but such complete oxide isolation previously required very difficult processing. Using the new, recrystallized-polysilicon approach, both process simplification and control can be obtained. One type of transistor is fabricated in the single-crystal substrate, and the other type is formed in a layer of recrystallized polysilicon separated from the single-crystal substrate by an insulating oxide layer.

Placing one type of device in the single-crystal substrate and the other in the polysilicon layer provides the additional advantage of optimizing the characteristics of the most critical transistor. For optimum circuit performance p-channel transistors are fabricated in a layer of laser-recrystallized polysilicon while n-channel transistors are constructed in adjacent regions of the underlying single-crystal substrate. To simplify the processing and allow the use of existing masks, the transistors are separated laterally, rather than being stacked with a common gate. Fig. 5 schematically shows the cross section of such a transistor

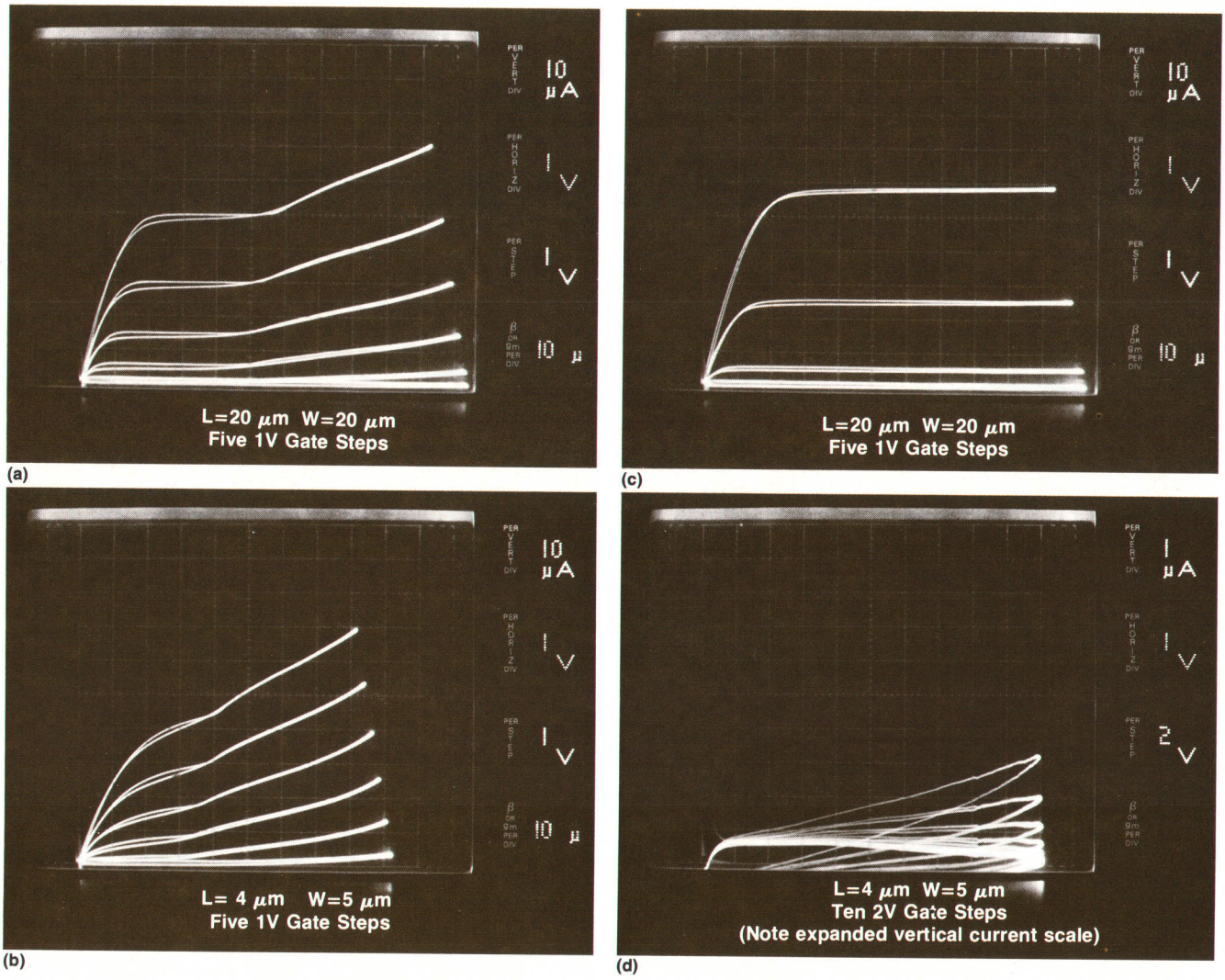


Fig. 4. *Source-drain characteristics of (a) large-geometry and (b) small-geometry transistors fabricated in recrystallized polysilicon, along with the characteristics of (c) single-crystal-silicon and (d) fine-grain-polysilicon transistors (see reference 2).*

pair.

Both n-channel and p-channel, large-geometry transistors exhibit well behaved saturation regions with square-law characteristics. Threshold voltages are approximately 1V for the single-crystal, n-channel transistors and −2V for the recrystallized-polysilicon, p-channel transistors. Carrier mobilities are 670 and 120 $cm^2/V\text{-}s$, as expected for the two types of transistors.

Several different, fifteen-stage ring oscillators were fabricated. Their oscillation periods agree well with the times calculated to charge the capacitance associated with switching a stage. These switching times were calculated from the transistor geometries of each different ring oscillator and the characteristics of discrete transistors. Some of the capacitances that must be charged are markedly lower than in single-crystal circuits because the oxide under the p-channel transistors has a dielectric constant one-third that of silicon.

Future Trends

Future efforts can be directed along several paths. Demonstration of integrated circuits with transistors in the single-crystal silicon substrate and in layers of recrystallized polysilicon opens the possibility of significantly increased component density, as well as removing some circuit performance limitations (e.g., eliminating the possibility of latch-up in CMOS structures). In addition to improved density, novel structures can be obtained by using interactions in the vertical direction. For example, CMOS gates have been fabricated with a single gate electrode controlling a transistor of one type in the underlying single-crystal substrate and a transistor of the opposite type in recrystallized polysilicon above the gate electrode.[6] The extension to other novel, vertical IC structures offers exciting possibilities for "vertical integration."

Although the transistors in recrystallized polysilicon have characteristics approaching those of single-crystal transistors, the few remaining grain boundaries can limit device performance. Removing these grain boundaries by seeding the regrowth of the silicon layer through periodic contact between the polysilicon and the underlying single-

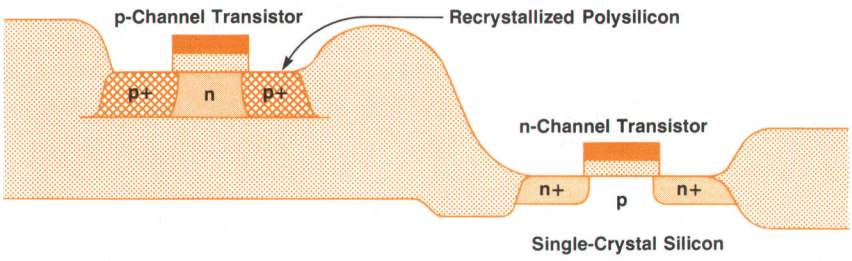


Fig. 5. *Schematic cross section of a CMOS transistor pair used in an integrated circuit. Any possibility of latch-up is avoided by completely surrounding one type of transistor by insulating silicon dioxide.*

crystal substrate (Fig. 6) can enhance the transistor performance.[9,10]

Fabricating MOS transistors with their channels in recrystallized polysilicon offers the most exciting and potentially useful application of beam-recrystallization technology. However, several more-straightforward applications should be mentioned. The ease of implementing these would lead to a more immediate impact on IC technology. For example, recrystallization of polysilicon may make the resistivity of high-valued resistors used in static RAMs less sensitive to slight variations in dopant concentration.[11] Melting only the top region of a polysilicon layer may smooth its surface, allowing the formation of higher-quality thermal oxides for double-level polysilicon-gate MOS ICs.[12] Finally, the use of other heat sources to melt the polysilicon, such as black-body radiation,[13,14] may simplify recrystallization.

Acknowledgments

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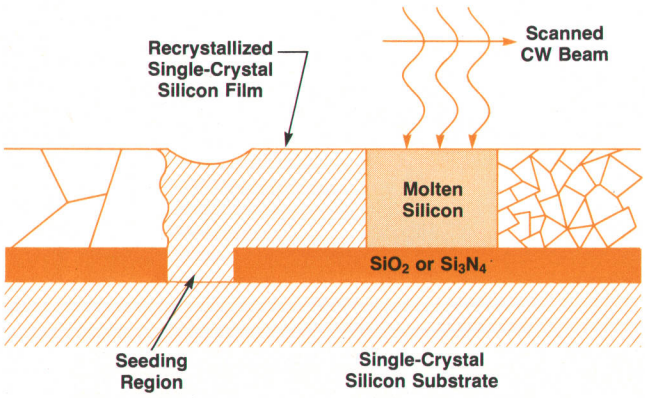

Fig. 6. *Single-crystal regions of silicon are formed by "seeding" the regrowth of a polysilicon layer using periodic contact between the layer and the underlying, single-crystal substrate.*

Theodore I. Kamins

Ted Kamins is an author or co-author of 52 articles, many on polycrystalline silicon. He is a co-author of a book, *Device Electronics for Integrated Circuits*, and is named inventor on five patents related to IC technology. Ted joined HP in 1974 with several years of experience in materials and device R&D work. He is a project leader in the Integrated Circuit Laboratory of HP Laboratories. Ted holds BS (1963), MS (1964), and PhD (1968) degrees in electrical engineering awarded by the University of California at Berkeley, where he has held the position of acting assistant professor. He has also served as a visiting lecturer at Stanford University. Ted is a member of the Electrochemical Society and a Senior Member of the IEEE.

X-Ray Lithography

The shorter wavelengths of soft X-ray radiation make the definition of even smaller dimensions for VLSI circuits possible.

by Garrett A. Garrettson and Armand P. Neukermans

X-RAY LITHOGRAPHY is proximity printing using a quasi-point source of soft (0.25 to 3.0 keV) X-rays. The important elements of an X-ray exposure system are illustrated in Fig. 1. X-rays are generated in an evacuated area by electron bombardment and penetrate a thin (25 to 50 μm) beryllium window. They are shadowed by a mask consisting of an absorber pattern supported on a flat membrane (5 to 10 μm thick) that is relatively transparent to the radiation. The mask is accurately positioned parallel to the wafer and in close proximity (typically 10 to 100 μm) with it. The wafer is coated with an X-ray-sensitive resist. The space between the X-ray source and the mask (working distance D) is evacuated or filled with helium to reduce attenuation of the radiation.

X-Ray Source

High-energy (10 to 30 keV) electron bombardment sources are commonly used to generate the required soft X-ray radiation. Other sources such as synchrotron radiation, plasma pinch, and laser plasmas are being considered, but presently their application to integrated circuit lithography is either prohibitively expensive or needs further development.

A typical measured spectrum from 20-keV electron bombardment of palladium (Pd) is illustrated in Fig. 2. The desired characteristic radiation under the peak (2.84 keV) is caused by electronic transitions in the L_α shell of a palladium atom. The remaining continuum spectrum is caused by the deceleration of electrons interacting with the Pd target atoms. Although the continuum spectrum does provide some additional exposure energy, its predominantly higher-energy X-rays are weakly absorbed, tending to produce an undesirable reduction of exposure contrast. Maximum source brightness (maximum power and minimum spot size) are factors determined by the electron optics, the characteristics of the anode (melting point, vapor pressure, elastic strength), and the performance of the cooling system.

Mask and Resist

The X-ray mask is the most critical structure in the system. The membrane (pellicle) supporting the absorber pattern must be made of a thin, low-atomic-number material to minimize X-ray attenuation, and yet must remain stable to minimize distortions caused by stresses in the absorber pattern. Typically the pellicle is stretched across a stiff, flat ring whose expansion coefficient matches that of silicon. This is essential to achieve good gap control between the mask and the wafer and to alleviate the requirement for absolute temperature control. To first order, the absorber pattern and the wafer should expand and contract at the same rate.

A typical mask structure is shown in Fig. 3. Factors important to mask fabrication are pattern accuracy, absorber line-edge profile, and defect density.

Whereas for optical masks the transmission through clear and opaque areas may differ by orders of magnitude, for X-ray masks the transmission may only differ by approximately a factor of ten. For good contrast the absorber material is made as thick as possible (typically 0.1 to 1.0 μm of gold). Hence submicrometer linewidths result in absorber pattern aspect ratios (thickness divided by lateral dimension) approaching unity, which require considerable expertise in fabrication. A careful tradeoff must be made among the source energy spectrum, mask transmission and contrast, and absorption in the X-ray resist.

Presently, for state-of-the-art integrated circuit lithography (minimum feature size of 0.5 to 1.0 μm), the combination of Pd-L_α radiation, a boron-nitride mask pellicle, a gold absorber pattern, and a resist containing chlorine appears most effective. The fortuitous position of the Pd-L_α peak with respect to the chlorine absorption edge (Fig. 4) and the symbiotic effect of this halogen, which increases both absorption and resist speed, make a powerful combination.[1] For higher-resolution lithography, characteristic radiation softer than Pd-L_α can be used to reduce the required absorber thickness and increase absorption in the resist at the expense of reduced X-ray energy at the wafer.

Alignment

Given an accurate mask pattern there must be a consistent mechanical means for positioning it with respect to the wafer to insure level-to-level alignment accuracy. This requires position references on the mask and on the wafer, as well as an alignment scheme. As illustrated in Fig. 1b, the mask-to-wafer gap can be adjusted to compensate for linear distortion of the wafer or the mask caused by process-induced strain. This is a significant advantage that allows good layer-to-layer alignment over larger fields than would be possible otherwise. Reproducible mask-to-wafer gap control is essential for accurate alignment. For this reason the mask plane must be flat to better than a micrometer and the wafer topography must be kept consistent each time the wafer is pulled down on the vacuum chuck. Dirt between the chuck and the wafer can result in surface bumps unless the chuck is designed to minimize the contact area. For this

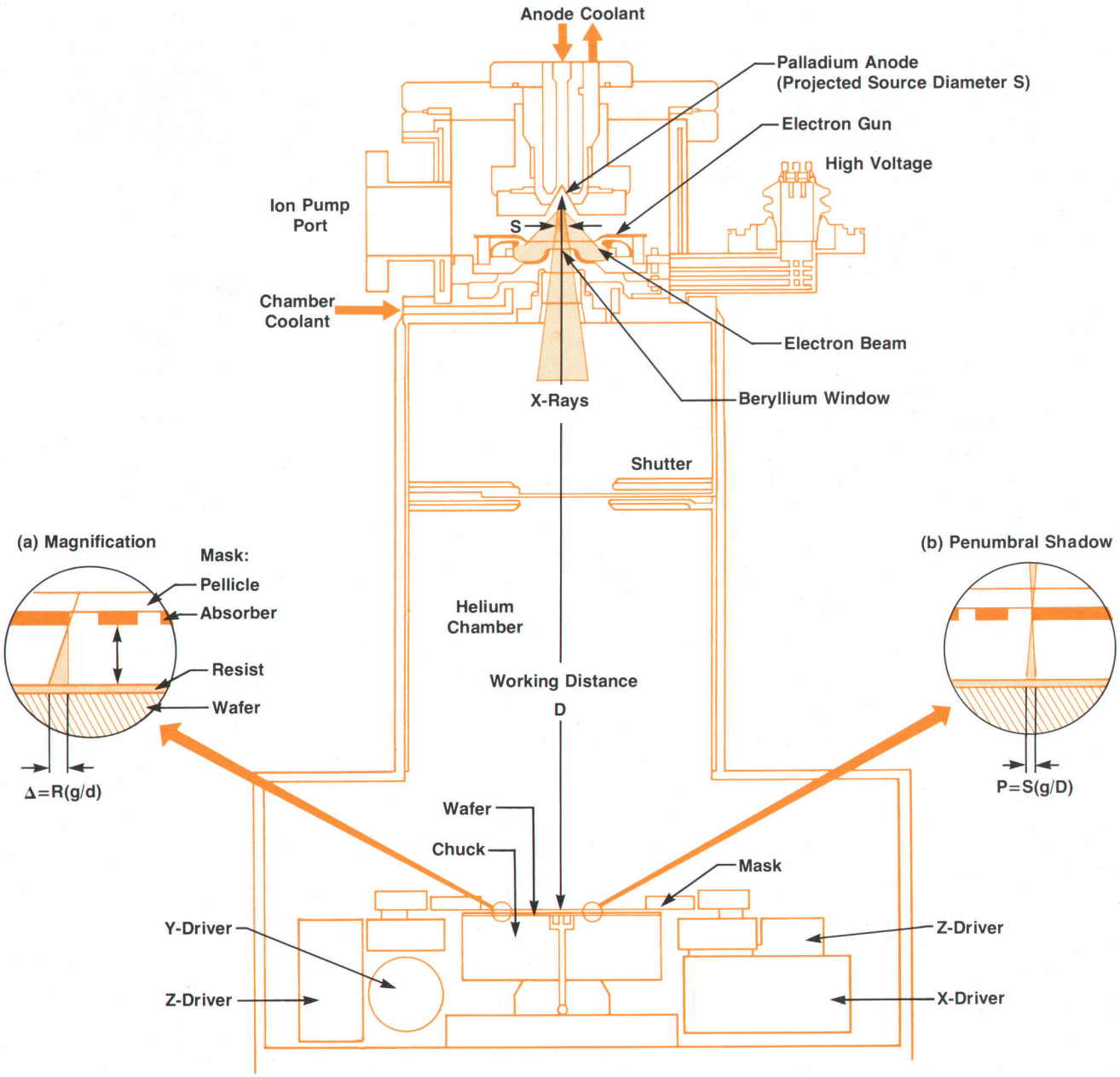

Fig. 1. *Basic X-ray lithography system. Close-up views of mask-to-wafer cross section showing (a) magnification and (b) penumbral shadow errors.*

reason a "bed-of-nails" design using many small contact areas is preferred.[2]

Tradeoffs

The perceived advantages of X-ray lithography have been its extreme fine-line capability (because of the absence of diffraction and proximity effects[3]), uniform resist exposure that allows high resist aspect ratios, good linewidth control, and insensitivity to dirt. As the field develops the perception of the strengths of X-ray lithography relative to other microlithographic technologies is evolving.

There have been dramatic improvements in the last five years in the performance of optical lithography, principally through the use of projection/reduction steppers and multilevel resist technologies. This performance comes, however, at considerable capital expense, reduced throughput, and increased processing complexity. The investment for an X-ray system is projected to be a fraction of that required for an optical stepper. Although many of the technologies involved are not easy to master, they are not necessarily expensive in their execution. High throughput is projected (20 to 100 wafer levels an hour), because of large subfields and relatively short exposure times (down to 20 seconds using a 4-kW source).[4] Less stringent environmental requirements and the potential for using single-level resists are additional advantages.

In a recent study, Lepselter computed a figure of merit for various lithographic systems, which included such factors

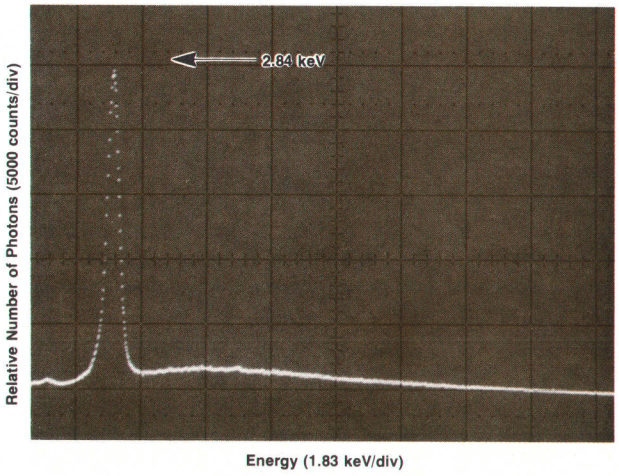

Fig. 2. *X-ray spectrum for palladium target excited by 20-keV electrons.*

as useful resolution, throughput, cost, and clean room footprint (floor space required). He concluded that X-ray lithography's potential merit is at least ten times that of any other submicrometer lithographic technology.[5] His study, however, does not take into account the various difficulties in making appropriate masks, which are crucial. Fabrication of accurate, defect-free 5× and 10× recticles is easier than fabrication of the 1× masks required for X-ray lithography. The physical barriers inherent in pushing optical systems to their limits are traded for the technological problems of X-ray-mask fabrication. Many steps in X-ray-mask fabrication are similar to those used in wafer processing, but the inherent defect densities of these processes must be decreased. On the other hand, considerable progress is being made in improving mask stability, formerly the principal concern.[6]

X-ray lithography also requires new sensitive resist systems that are just beginning to become available. Source brightness and resist sensitivity will determine the system throughput capability.

Initially, X-ray lithography will complete with optical projection direct-step-on-wafer (DSW) technology. Optical DSW performance is limited by cost, throughput, susceptibility to the environment, and by tradeoffs among resolution, field size, and depth of focus. Registration for X-ray lithography appears easier to do than for optical lithography because of the magnification correction and the close proximity of the mask to the wafer.

As linewidths continue to shrink a regime will be reached where only X-ray stepper and electron beam technologies are viable. X-ray lithography can be considered a complementary extension of the electron beam pattern generator. It can accurately replicate submicrometer patterns with good linewidth control, which is necessary for consistent MOS device thresholds.

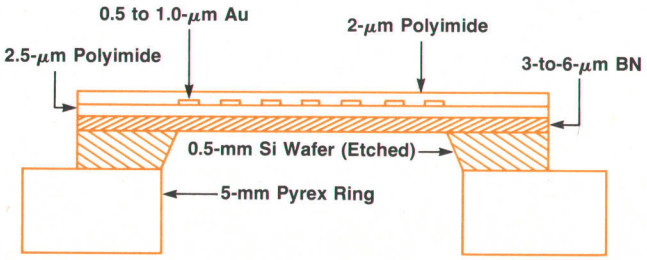

Fig. 3. *Cross section of typical X-ray mask structure.*

Hewlett-Packard X-Ray Program

The objective of the present Hewlett-Packard Laboratories program is to demonstrate a complete X-ray lithography technology that will be simple, high-performance, and cost-effective for submicrometer devices in VLSI circuit production. The current goal is to establish a state-of-the-art capability at HP Laboratories for mask technology and process development so that X-ray lithography can mature to a level suitable for use in HP's production facilities.

In order of priority, HP has been developing an X-ray-mask fabrication and precision mask-to-wafer alignment

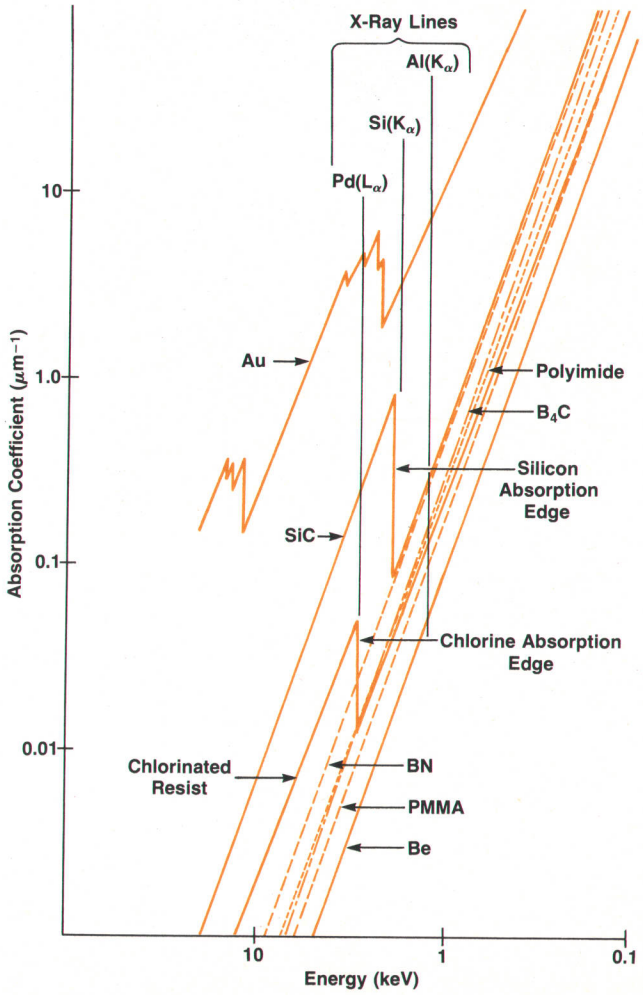

Fig. 4. *Absorption coefficient versus X-ray wavelength for several materials.*

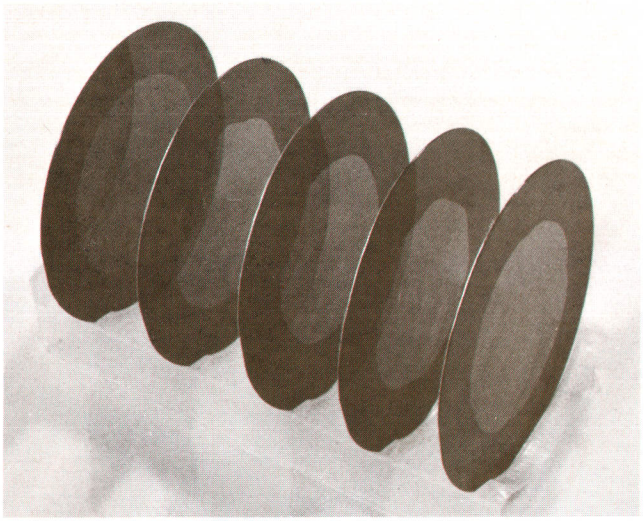

Fig. 5. *Photo of boron-nitride pellicles.*

capability, fast resist systems, a bright X-ray source, and laboratory exposure tools. The first-generation mask technology uses a pellicle of chemical-vapor-deposited boron nitride and polyimide supporting a sputter-etched gold absorber pattern (Fig. 3 and Fig. 5). This is bonded to a Pyrex™ ring for mechanical and thermal stability. Initial tests indicate that presently the stability is adequate for design rules down to one micrometer. Other materials such as silicon carbide and boron carbide have been investigated for the mask pellicle and they show considerable promise for future applications.

Defect density remains a critical problem. With careful process control, defects have been reduced around two orders of magnitude in the past year. Two orders of magnitude more will be required for VLSI.

A number of fast, chlorinated, negative resists have been evaluated. Fig. 6 (page 18) shows submicrometer features in 0.6 to 0.8 μm of remaining resist material that has been exposed about 4 minutes using a 4-kW source at a working distance of 35 centimeters. A fixed anode source of a modified Gaines design[7] has been built (Fig. 1). With a proprietary cooling technology it appears that power densities greater than 40 kW/cm^2 may be accommodated.

Several laboratory exposure systems have been built for evaluating resists, for mask development, and ultimately for IC applications. The latest is a very compact automatic-alignment exposure system employing a novel mask-to-wafer positioning system with six degrees of freedom. A proprietary alignment scheme can resolve misalignments as small as 20 nanometers consistently, but the level-to-level alignment accuracy of the system has yet to be determined under realistic operating conditions.

Acknowledgments

The authors acknowledge the support of their colleagues in the Physical Electronics and Solid-State Laboratories of Hewlett-Packard Laboratories and thank them for their contributions to the work described in this article.

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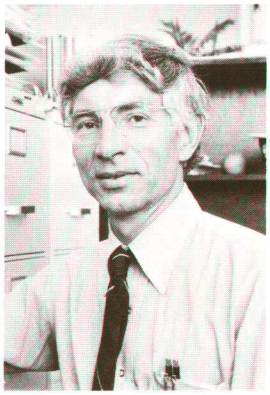
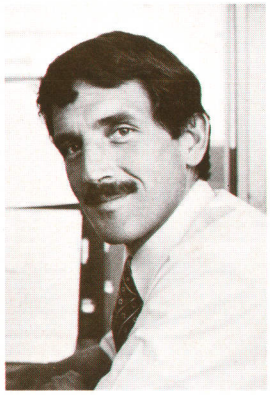
Armand P. Neukermans



Armand Neukermans is a project manager for X-ray lithography at HP Laboratories. Born in Okegem, Belgium, he received his BSME and BSEE degrees from Louvain University in 1962, did engineering work for the next five years, and then returned to school, receiving his MSEE degree from Arizona State University (1967) and PhD degree in applied physics from Stanford University (1970). After three years of xerographic research, Armand joined HP in 1973. Among his contributions are a cesium iodide X-ray imaging screen, an electron capture detector for gas chromatography, and work on Monte Carlo simulations for electron beam exposures. His work has resulted in ten patents and 13 papers. He is a member of the IEEE and Sigma Xi. Armand is married, has four children, and lives in Palo Alto, California. He teaches religious education and enjoys jogging, swimming, and hiking.

Garrett A. Garrettson



Garry Garrettson is a native of California born in San Francisco. He attended Stanford University, earning the BS (1965) and MS (1966) degrees in engineering physics and the PhD (1969) degree in mechanical enginering. After a few years as an assistant professor at the U.S. Naval Postgraduate School, Garry joined HP Laboratories in 1973. Since then he has worked in areas of metrology, medical instrumentation, and photoconductor development. Garry presently is a department manager in the Physical Electronics Laboratory of HP Laboratories and has responsiblity for lithography strategy and X-ray technology development. He is the author or co-author of six publications related to transport theory and lithography. Garry served several years in the U.S. Navy, attaining the rank of lieutenant. He is a member of the American Physical Society and the American Association for the Advancement of Science. He is married, has two children, and lives in Los Altos Hills, California. Outside of work, Garry coaches soccer and baseball and supports a Cub Scout group. He enjoys running, skiing, carpentry, and flying (he has a commercial pilot's license with an instrument rating).

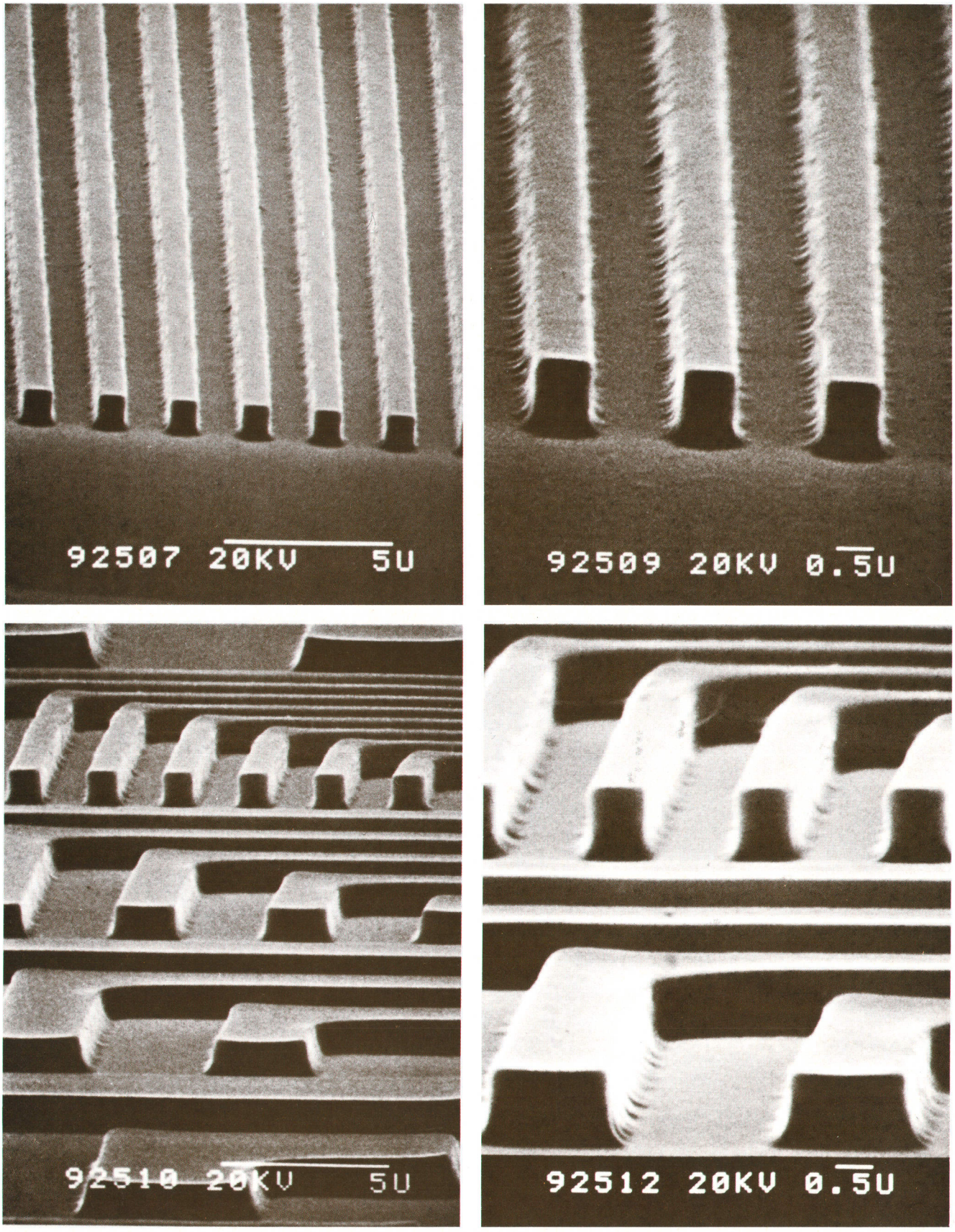


Fig. 6. *Patterned results in fast negative resist using X-rays from Pd anode excited by 10-keV electrons, a 25-μm-thick beryllium window, and a mask-to-wafer gap of 25 μm.*

Dry Etching: An Overview

Plasma etching technology has several advantages for IC processing compared to wet-chemical etching methods. Anisotropic etching and automatic endpoint detection are two of the advantages discussed in this article.

by Paul J. Marcoux

ONE OF THE BASIC TRENDS in silicon integrated circuit process technology is the shrinking of device geometries. Recent advances in lithography allow the patterning of feature sizes sufficiently small that conventional methods of etching are inadequate. During the past several years dry etching has evolved to the point where this etch process can transfer the lithographic pattern to the device structure with high fidelity.

The process technique of dry etching has many variations. This technology ranges from processes in which the etching proceeds by a purely physical mechanism to cases in which chemical interactions dominate the etch. The most versatile dry etch processes for pattern replication are those in which chemical etching is enhanced by the physical component of the process. Ion milling and sputter etching techniques use momentum transfer from inert-gas ion bombardment as the physical etch mechanism. Reactive ion beam etching (RIBE, also reactive ion milling), reactive ion etching (RIE, also reactive sputter etching) and plasma etching all use reactive ions to transfer momentum to the sample and add a chemical component to the etching process. Table I provides a qualitative comparison of the dry etch technologies and conventional wet etch processing.

The key process characteristics associated with the plasma etch process are anisotropy and etch selectivity with respect to the photoresist mask and the underlying materials (etch stop). Fig. 1 shows a representation of a typical cross section of an etched sample.

The after-etch profile of a feature is the critical result of the plasma etch process. This profile indicates whether or not a particular etch process gives an isotropic (uniform in all directions) or anisotropic (direction-dependent) etch. In

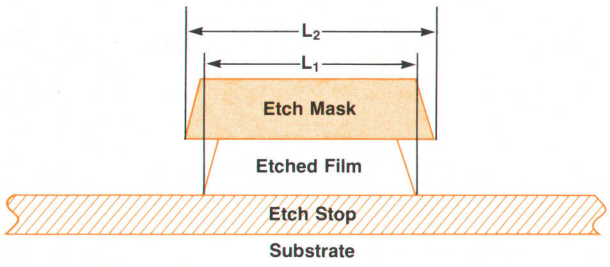


Fig. 1. *A typical cross section of an integrated circuit feature. For an anisotropic etch $L_1 = L_2$ and L_2 is not altered by the etch process. In most processes the ratio of the film etch rate to the etch-stop-material etch rate varies from 5:1 to 10:1. The ratio of the film etch rate to the mask etch rate is similar.*

Table I

A Qualitative Comparison of Etching Methods for Silicon Integrated Circuit Fabrication

	Physical Etching	Plasma-Assisted Etching	Wet Etching
Process:	Ion milling, sputter etching	RIBE, RIE, plasma	Wet chemical
Mechanism:	Momentum transfer	Ion-assisted chemical reaction	Chemical reaction
Selectivity:	Poor (≈2 to 3:1)	Fair (≈5:1) to excellent (>30:1)	Excellent
Directionality:	Anisotropic	Anisotropic/isotropic	Isotropic

Fig. 2 isotropic and anisotropic etch profiles are compared. For processes that produce an isotropic etch profile the reduction of linewidth is at least twice the film thickness. Since the linewidths of minimum-size features are typically two to four times the film thickness it is obvious why an isotropic etch is not useful. The only way to reproduce fine-line lithography is to use an anisotropic etch. Another important feature of an anisotropic etch is that generally there is no increased loss of linewidth control with overetching. This is important because overetching is required in routine processing to ensure that all wafers in a load have been completely cleared during the etch process.

In ion milling and sputter etching, inert gas ions bombard the surface of the wafer and sputter away the surface atoms via momentum transfer. In ion milling, ions are extracted from an ion source, accelerated, and deionized before impacting the surface being milled. In sputter etching, ions that bombard the surface are extracted from the gas glow discharge in which the wafers are immersed. In both of these methods the etching is quite anisotropic because the motion of the ions follows electric field lines that are perpendicular to the substrate. The etch selectivity for these processes is generally poor because the sputter yields for materials used in integrated circuit fabrication are similar. In addition, there is often redeposition of the sputtered material along the sidewalls of the lithographically defined pattern. In spite of these disadvantages these technologies are useful, particularly in the laboratory, because they can be used to pattern fine lines in a wide range of materials.

Reactive ion beam etching is an emerging technology that

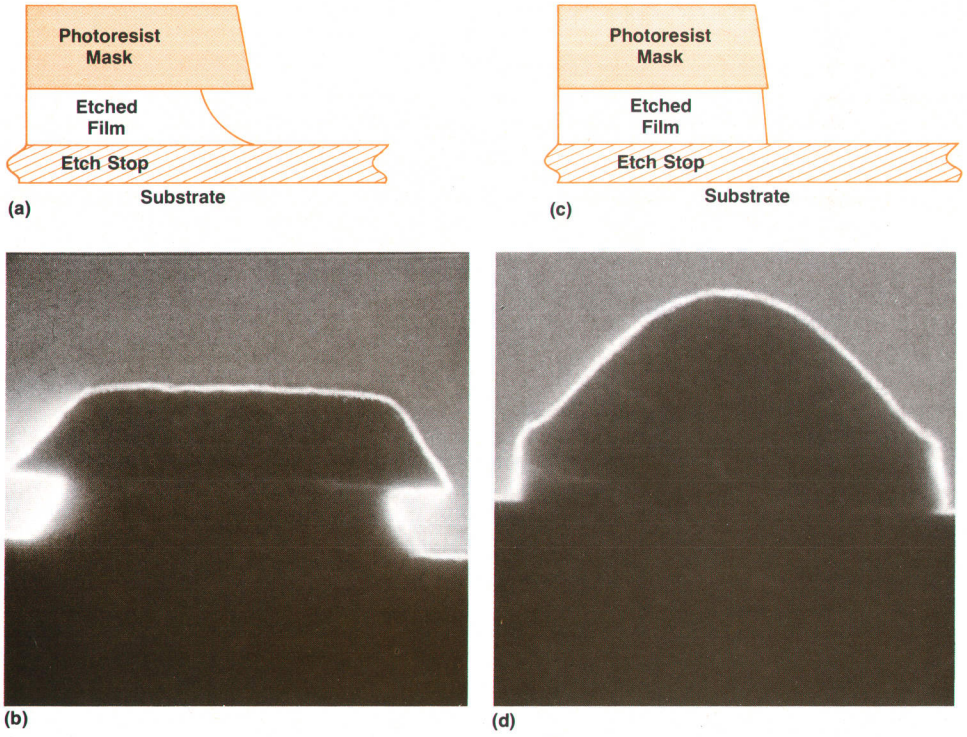


Fig. 2. *Comparison of the etch profiles for isotropic and anisotropic etching. (a) Diagram of isotropic etch profile. (b) SEM photograph of actual isotropic profile. (c) Diagram of anisotropic etch profile. (d) SEM photograph of actual anisotropic profile.*

is similar to ion milling except that the ions responsible for the sputtering action are also reactive. This approach has the advantage that the material being etched can be converted to a volatile compound as well as sputtered. At this time this technology is mainly a laboratory tool. However, if the numerous equipment problems can be overcome it may see broader application.

The techniques of reactive ion etching and plasma etching have the widest range of commercial and laboratory applications. Both etching methods make use of a glow discharge to create the reactive etch species and the ions responsible for the etch process from the input gases. These reactive species and ions diffuse to the substrate surface where they react with the thin film to be etched. This etch reaction must produce a compound that is volatile; otherwise the etch process will be quenched by a residue coating on the surface. It is also very important that the etch reaction be selective with respect to the mask material and the materials under the layer being etched. The principal hardware differences between these two technologies are that in reactive ion etching the substrates are placed on the cathode and the gas pressure is low, while in plasma etching the wafers are placed on the anode and the gas pressure is somewhat higher. In most cases this results in higher ion energies and hence more momentum transferred to the surface in reactive ion etching. Table II lists materials that have been etched using plasma etching at Hewlett-Packard Laboratories. It shows the versatility of this technology and indicates the possible reactive etch species and corresponding volatile etch product for each material.

Reactors

Commercially available plasma etch reactors range from laboratory apparatus to highly automated reactors suitable for use in integrated circuit manufacturing. These reactors are available in two basic configurations: barrel or parallel plate. The selection of the configuration depends upon the user's application. All reactors have the following basic components: reaction chamber, vacuum system, gas flow control, an RF power supply, and in most cases, automatic gas pressure control. In the more sophisticated reactors a microprocessor controls the gas flows, total pressure, and the vacuum values associated with the reactor. In many systems the wafer handling is also automated. An increasing number of reactors have automatic process endpoint detection to determine when the etch process is complete (see box on page 22).

Table II

Summary of Plasma Etch Processes

Material Etched	Etch Gas Composition	Reactive Species	Principal Etch Products
Resist	O_2	O	O_2, H_2O, CO_2
Si	CF_4+O_2	F	SiF_4
	CCl_4 + He	Cl	$SiCl_4$
SiO_2	C_2F_6+He	CF_3, F	SiF_4, CO, CO_2
Si_3N_4	CF_4+O_2	F	SiF_4, N_2
W	CF_4+O_2	F	WF_6
Mo	CF_4+O_2	F	MoF_6
	CCl_4+O_2	Cl, O	$MoOCl_4$
Ti*	CF_4+O_2	F	TiF_4
Cr*	O_2	O	CrO_3
	CCl_4+O_2	Cl, O	CrO_2Cl_2
Al	CCl_4/He	Cl	$AlCl_3$

*Proceeds at elevated temperatures (T >100°C).

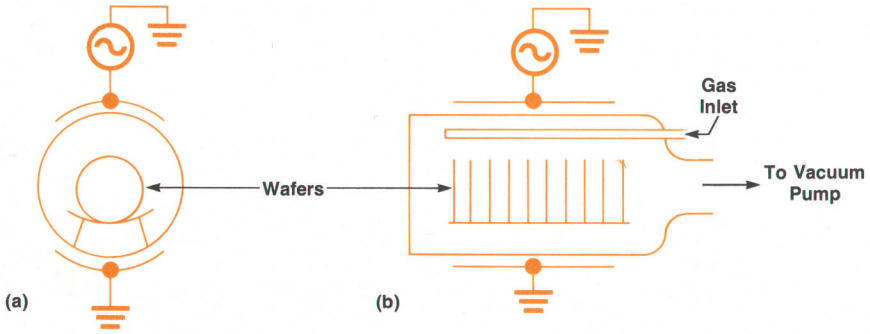


Fig. 3. *Diagram of barrel plasma reactor. (a) End view. (b) Side view.*

A typical barrel reactor (Fig. 3) has the advantage that large wafer loads are possible in a quite small reactor volume. Plasma etch processes in these reactors generally result in an isotropic etch. Hence the main application for these reactors is noncritical etching.

Two principal configurations for parallel plate reactors are shown in Fig. 4. In the plasma etch mode the wafers are placed on the anode. Plasma reactors typically operate in the gas pressure range of 100 to 1500 millitorr, the total gas flow rates are on the order of 38 to 1520 torr-liter/s and the RF power densities range up to 0.7 watts/cm². The vacuum system required by these reactors has a rather high base pressure of approximately 10 millitorr.

In the reactive-ion-etch mode the wafers are placed on the cathode and the power densities range up to 2 watts/cm². These reactors generally use low total gas flow rates of 0.76 to 7.6 torr-liter/s and the operating pressures are in the range of 10 to 50 millitorr. The vacuum system used by these reactors generally is capable of reaching an ultimate vacuum of 0.001 millitorr.

Fig. 4 shows parallel plate reactors in the batch configuration. It is obvious that, as the wafer size increases, the throughput (wafers/hour) will decrease, and the total wafer area per load will decrease slightly. In response to this negative effect on throughput, a relatively new type of parallel plate reactor has become available—the single-wafer cassette-to-cassette reactor. This reactor has the advantage that wafer throughput is independent of wafer size, and hence there is an increasing wafer area throughput as the wafer size increases. To achieve adequate wafer throughput, however, the etch rates for materials must be quite high. This demands that the etch selectivity and anisotropy be higher in this single-wafer design than in a batch reactor to achieve comparable process performance. Thus the overall process control must be tighter in a single-wafer reactor than in a batch machine.

Processing Parameters

Plasma etching is in general a very complex process. One main reason is that there is a large parameter space that must be well controlled. Furthermore, despite an intense research effort by many laboratories, the interaction among different parameters is not well understood. However, one can make some generalizations about the effects of these parameters.

In a typical plasma etch system the parameters include gas mixture composition, RF power, total flow rate, gas pressure, and substrate temperature. The most important parameter is the composition of the etch gas. This parameter determines whether a process will etch a given material, etch the material with the desired selectivity, and etch anisotropically. It is true that the other parameters can have a substantial effect on the particular process characteristics, but without the correct etch gas these properties cannot be achieved.

The RF power level has a strong influence on the etch rate. It is often observed that the etch rate increases with a linear to quadratic dependence on RF power. Increasing the RF power tends to result in an increased ionization of the etch gas and increases the sheath voltage. This increases the average energy of ions bombarding the wafer surface and thereby increases the anisotropy of the etch. The RF power level also controls the particular chemistry of an etch gas. This occurs because the RF power strongly influences the distribution of energy of the electrons and this determines what particular atoms, ions, and free radicals will be produced from a given etch gas.

The total gas flow rate and pressure determine the residence time of an ion or reactive species in the discharge. The residence time t is approximately given by the following equation:

$$t = (V/F)(P/760)$$

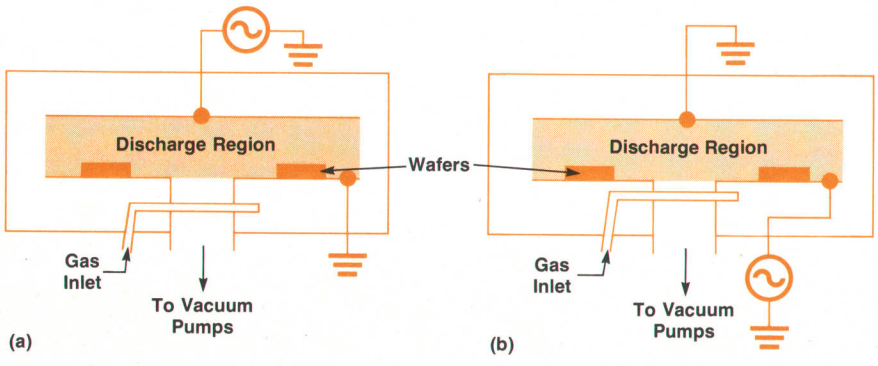


Fig. 4. *Diagram of side view of parallel plate reactors in (a) the plasma mode and (b) the reactive-ion-etch mode. The gas flows radially inward over the wafers that are in intimate contact with the plasma.*

An Automated Plasma Reactor

With the advent of computers having a higher performance-to-cost ratio and the need for more complex, tightly controlled IC processing steps there has been an increase in the use of automated processing equipment. Several years ago, a team of engineers in Hewlett-Packard's Integrated Circuits Processing Laboratory (ICPL) initiated a project to develop an automated plasma reactor to be integrated into the process control system (PCS). PCS is a network of computers involved in process control and wafer tracking.[1] The project has built two reactors for use in ICPL.

Functional control for these systems is provided by memory-based HP 1000 Computers interfaced to the plasma reactors through digital-to-analog controllers. Operational command sequences are downloaded from a central user-created data base and then sequentially executed by the local control computer. Five major software routines (wafer handling, pressure, gas flow, RF power, and temperature) provide closed-loop control of wafer loading and the necessary plasma processing parameters. Throughout the processing sequence, system performance is monitored and can be displayed in either a text or graphic format at intervals of 5 to 60 seconds. Also available is a TRACE function that allows sequential sampling of up to 16 of the monitored parameters and storage of this information in central data files. The data accumulated by TRACE can then be recovered in list or graphical form. In addition, an automatic endpoint detection system has been installed which uses either laser interferometry or optical emission spectroscopy to determine etch completion. The system then calculates and executes the desired overetch before extinguishing the plasma.

The design philosophy behind these reactors has been to build systems that provide a simple-to-operate, repeatable production tool flexible enough to be used for new process development. For routine processing, standard operations are automatically downloaded from the PCS central data base to the local controller when wafers are tracked into the reactor. The etch sequence is initiated by simply pressing the **START** button. All process gases are automatically purged from the reactor upon etch completion for user safety. Wafer handling by personnel is minimized by the system's automated cassette-to-cassette wafer loading capability. A load-lock chamber houses the loading mechanism. This isolates the main reactor chamber and thus minimizes process variations caused by atmospheric contamination. Operating sequences and parametric setpoints can be edited through the display keyboard to provide the flexibility required for development purposes.

Acknowledgments

Among the many who have contributed their efforts to making the automatic plasma reactor a working reality are Bill Goodman, John Youden, Mary Dryden, Gary Modrell, Ulrich Kaempf, Dennis Harding, Subhash Tandon, Chris Clare, Bob Schuchard, Mel Jennings, and Bob Starkovich. Recognition also goes to Pat Castro and Fred Schwettmann for their support of the project.

Reference

1. C.R. Clare, "A Process Control Network," Hewlett-Packard Journal, Vol. 32, no. 6 June 1981.

-Susan Okada

where V is the reactor volume, F is the flow rate and P is the pressure in torr. The residence time determines the flat zone of a reactor, that is, the region over which the concentration of reactive species is nearly constant. The magnitude of this distance will determine the etch uniformity for a particular etch condition. The chemistry of the discharge is altered by the total gas pressure because pressure changes alter the gas phase chemistry. It is in the gas phase that the reactive etch species are produced, hence the influence of pressure on the chemistry of the etch process.

The substrate temperature has an influence on etch rate and selectivity, and if allowed to go as high as 150°C, will cause photoresist degradation. The etch rate R can be described by the following expression:

$$R = A \exp(-E/kT)$$

where A is a constant, E is activation energy, k is the Boltzman constant and T is the absolute temperature (K). The activation energy in this expression represents an average over the important kinetic process and typically lies in the range of 0.05 to 0.5 eV. It is clear from the above expression that temperature should be well controlled because of the exponential dependence.

Endpoint Detection

Besides the large number of parameters discussed above that must be well controlled, there are other parameters that are difficult to control in a routine processing environment (e.g., condition of the reactor walls). The variations in both the well controlled and poorly controlled variables lead to variations in the performance of the process, particularly in the reproducibility of the etch rate. The use of endpoint detection to determine when the etch process is complete eliminates the effects of these variations on the process performance. In addition, there is an increase in throughput because the tedious procedure of calibrating etch times can be eliminated.

Many different techniques have been used for endpoint detection. A summary of the methods, principles of operation, and measured values that have been investigated by Hewlett-Packard Laboratories is presented in Table III. Ob-

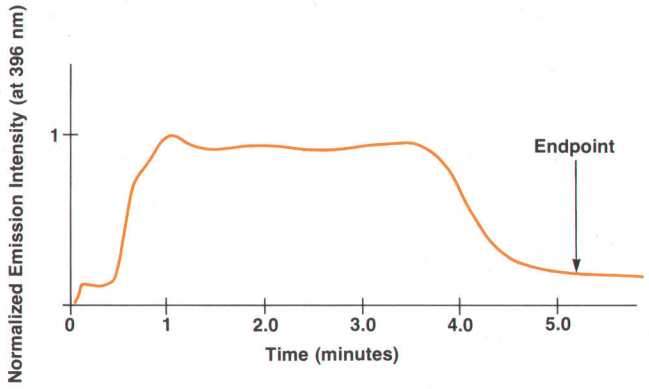


Fig. 5. *A plot of the emission intensity of the 396-nm-wavelength line of aluminum in normalized units versus time. The period of time before etching begins (inhibition period) is about one minute and the endpoint occurs at 5.2 minutes.*

Table III

Summary of Methods for Endpoint Detection in Plasma or Reactive Ion Etching

Method	Measuring	Monitoring	Endpoint
Emission spectroscopy	Light emitted from discharge	Emission from reactive species and/or etch products	Average for all wafers*
Optical reflection	Interference phenomena or changes in reflectivity	Changes in film thickness	For one wafer only
Mass spectroscopy	Gas composition	Etch products	Average for all wafers
Impedance monitoring	Impedance mismatch	Voltage change	Average for all wafers
Langmuir probe	Changes in electron density and average energy	Current from probe	Average for all wafers
Gas pressure	Total pressure	Changes in total pressure	Average for all wafers

*Dependent on optics.

viously from the endpoint data, all of the techniques provide an average etch rate. The optical reflection method, which monitors the change in film thickness, also serves as an in-situ etch-rate monitor for dielectric films.

Emission spectroscopy has the longest history of the methods described in Table III. There are many variations of the experimental apparatus using emission spectroscopy for endpoint detection. The essential feature of such an apparatus is that it be able to detect the particular wavelength of light emitted by either a reactive etch species or a volatile etch product. For purposes of endpoint detection, it can be assumed that the intensity of the emission line is proportional to the concentration of the reactive etch species or volatile etch product in the plasma. If one monitors a reactive etch species the intensity of the emission from the species should be less in the presence of the film to be etched than in its absence. Hence at endpoint there is an increase in the signal when monitoring a reactive etch species. Conversely there is a decrease in the signal when monitoring etch products. In most cases monitoring of an etch product is preferred, because one need only determine the presence or absence of the material responsible for the signal.

To demonstrate the usefulness of endpoint detection, consider the use of emission spectroscopy for endpoint detection and process monitoring of aluminum etching. The optical emission wavelength monitored is that of elemental aluminum at 396 nm. The intensity of this line is proportional to the amount of aluminum being etched. A typical endpoint trace is given in Fig. 5. The rise of the aluminum signal indicates the start of the etch process. It does not occur at t=0 because there is an inhibition period with this process. The inhibition period occurs because of residual moisture and oxygen in the reactor, photoresist scum, and the presence of a native oxide layer on the aluminum film. One cause of irreproducibility in an aluminum etch process is variation in the inhibition period from run to run. The magnitude of the emission signal is proportional to the etch rate of aluminum. The length of the plateau region is determined by the etch rate and the thickness of the aluminum layer. The decrease in the signal is a result of clearing the wafer; the steeper the descent the more uniform the etch process. The arrow indicates the endpoint of the etch process. As is typically the case some overetching is done to insure a complete etch. From this example it is clear that, in addition to endpoint data, detailed information on the performance of the process is obtained. This type of information is invaluable in a routine processing environment. A summary of emission wavelengths that have been found useful for endpoint detection is presented in Table IV.

Table IV

Summary of Emission Wavelengths and the Emitting Species Monitored for Endpoint Detection

Film Etched	Species Monitored	Wavelengths (nm)
Resist	CO	483.5, 519.8
Polysilicon	F	704
Silicon nitride	F	704
Aluminum	Al	396
	AlCl	261
Tungsten	F	704

Acknowledgments

The author would like to thank his colleagues, Dragan Ilic, Glenn Rankin, Pang Dow Foo, Bob Gleason, and Susan Okada for their help and stimulating discussions. Thanks are due to Fred Schwettmann, Pat Castro, and Bob Grimm for their support and encouragement during the course of this work. Special thanks are due to Frank Perlaki for the microphotographs that appear in this paper.

Paul J. Marcoux

Paul Marcoux is the manager of HP Laboratories' multilevel metallization IC project. He previously managed a dry etching project. His contributions have resulted in 12 papers on gas phase kinetics and plasma processing. Paul came to HP in 1978 after doing post-doctoral research in chemistry. He was awarded a BS degree in chemistry by Villanova University in 1970 and a PhD degree in chemistry by Kansas State University in 1975, and is a member of the American Chemical Society, the American Vacuum Society, and Sigma Xi. Born in Pawtucket, Rhode Island, Paul is married, has one child, and lives in Mountain View, California.

Thin Films Formed by Plasma Enhanced Chemical Vapor Deposition

Electrically exciting the gases used in a chemical vapor deposition process can reduce the sensitivity to temperature variations and allow deposition at lower temperatures. Some films produced by this technique are discussed.

by Dragan B. Ilic

PLASMA ENHANCED (PE) deposition of thin films has important advantages over conventional techniques used in silicon integrated circuit processing. Conventional atmospheric- or low-pressure (AP or LP) chemical vapor deposition (CVD) techniques form thin films by using the nucleation of atoms and molecules from the gas phase at the substrate (wafer) surface. This nucleation reaction is thermally driven, and thus is a very sensitive function of the wafer temperature. By contrast, in a gaseous plasma the chemical reactions are no longer thermally controlled so that effective film deposition can take place at temperatures far below those needed for APCVD or LPCVD.

Hence, one important advantage of PECVD is a relative insensitivity to wafer temperature. Depositions can take place in a wide temperature range from 20°C to the temperatures used in conventional CVD processes. However, PECVD films often are not stoichiometric, and have been found to contain large quantities of hydrogen incorporated from the process gases (usually hydrogen-based compounds of silicon, nitrogen, and carbon). These characteristics are manifested by large residual stresses built into these films as they are deposited. It is not unusual to have compressive or tensile stresses as large as 1000 atmospheres (10^9 dynes/cm^2), depending on plasma characteristics, process gas mixture, and wafer temperature. For good adhesion and crack resistance, a compressive stress is desirable.

There are numerous PECVD systems available commercially that produce good quality films suitable for IC passivation (silicon nitride) or dielectric intermediate levels (silicon oxide or nitride) in multilevel interconnection schemes. For VLSI production applications, a high wafer throughput, good uniformity, and low particle density are all important requirements. Reported here are the results of initial applications of films developed in a modern PECVD reactor, whose design is an outgrowth of the standard LPCVD systems. Uniformity of the deposited film thickness and the refractive index of the film material were checked by ellipsometry and spectrophotometry. The stress built into each deposited film was deduced by comparing the wafer curvature before and after film deposition (see box, next page).[1,2] All of the deposited films studied were found to have compressive stresses.

*Some of the data presented here has been previously discussed by the author in the April 1982 issue of Solid State Technology.

PECVD System

The PECVD system used at Hewlett-Packard Laboratories (HPL) was made by a commercial vendor of semiconductor manufacturing equipment. This system has been operating since July 1980, and proven to be sufficiently flexible to accommodate a wide range of different thin-film-deposition experiments. The system contains two completely independent thin-film-deposition systems, housed in a single frame.[3]

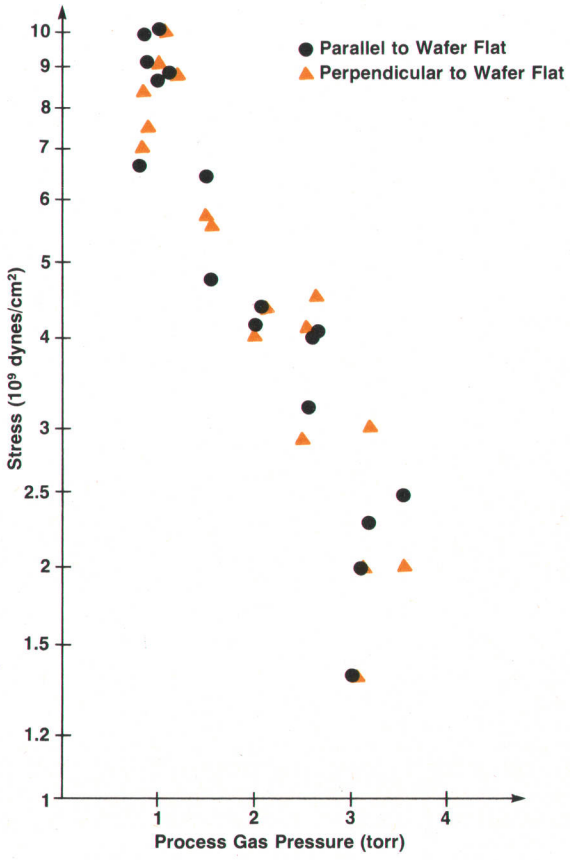


Fig. 1. *The variation of stress measured in standard silicon-nitride films as a function of process gas pressure.*

The plasma-enhanced deposition processes operate in the pressure range of 2 torr or less, using an RF power density on the order of one watt per wafer, given a full reactor load of 108 75-mm-diameter wafers.[1] The process gas flow rates are controlled separately by using mass flow controllers. An automatic throttle valve with a closed-loop control maintains the desired pumping speed or system pressure. This allows a wide range of pressures for a given gas flow. Furnace tubes are made of quartz, and the boats carrying the wafers are made of graphite plates connected by stainless steel and quartz pieces. A cleaning cycle to etch off accumulated deposits is available by running an intense discharge in a C_2F_6/O_2 plasma at a pressure of 1 torr.

Deposition and plasma-etch-clean experiments have been performed in this machine on a variety of different deposited films (Table I), using process recipes supplied by the manufacturer (standard films) or internally developed by HPL (developmental films).

Standard Films

Several standard films were deposited using process parameters recommended by the PECVD system manufacturer. The simplest and most reliable process is the deposition of silicon-nitride films.

These films are deposited at a rate of about 35 nm/minute using a mixture of ammonia (NH_3) and silane (SiH_4), at a pressure of 2 torr. The film thickness and refractive index are uniform within ±5% over a whole load of wafers and over any single wafer. This process is not sensitive to wafer temperature variations as mentioned earlier, an advantageous characteristic compared to nonplasma CVD processes.[3]

Pinhole densities were measured using an electrolytic (bubble) tester. Less than 0.3 defects/cm² were observed in 600-nm-thick silicon-nitride films, provided care was taken to clean the wafers adequately before the deposition. Auger surface scans have shown a film composition of 40% silicon, 54% nitrogen and 6% oxygen. A large percentage of hydrogen is also present in these films.[4] The silicon-nitride films have large compressive stresses that decrease with pressure (Fig. 1) and increase with RF power, but do not seem to change predictably with changes in the process gas mixture. Plasma etch tests, Fig. 2, show a change in etch rate as the ratio of the oxygen gas flow to the total etch process gas flow (oxygen plus C_2F_6) is varied from 0 to 1 at a gas pressure of one torr (Fig. 2). A maximum etch rate of 110 nm/minute was observed for an oxygen mole fraction of 0.35.

The silicon-nitride films exhibited excellent resistance to cracking, even over metal pads after a 450°C alloy temperature cycle. Film coverage over 1-μm-high aluminum steps was very conformal as observed through the use of a scanning electron microscope.

Silicon oxynitride films were deposited at a rate of 55 nm/minute using a gas mixture of silane, nitrous oxide (N_2O), and oxygen at a pressure of 1.1 torr. The refractive index of these films is about 1.52. Auger surface scans show the composition to be 26% silicon, 66% oxygen and 8%

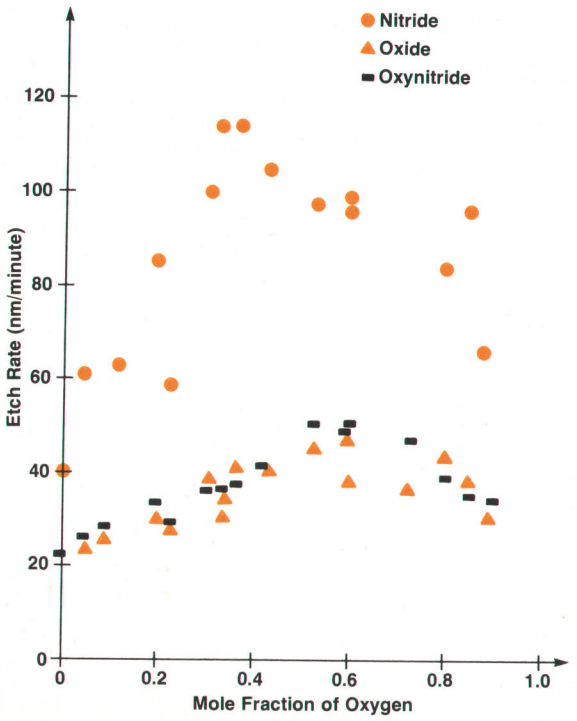


Fig. 2. *The etch rate of standard silicon-nitride, silicon-oxynitride, and silicon-dioxide films in C_2F_6/O_2 plasma.*

Determining Thin-Film Stress

The stress in thin films deposited on circular silicon wafers can be determined by measuring the change d in surface curvature, assuming a parabolic shape, before and after deposition as shown in Fig. 1. Then the stress can be calculated according to the formula:

$$S = ABdw^2/f$$

where S is the stress in dynes/cm², A and B are constants as listed in Table I for different crystal orientations and measuring apertures, w is the wafer thickness in μm, f is the film thickness in μm, and d is also in μm. For example, a <100> wafer, 450-μm thick, changes its curvature by 19 μm after deposition of a 0.63-μm-thick film. The measuring aperture on the wafer flatness tester is 63.5 mm in diameter. Thus the stress in the deposited film is 3.65×10^9 dynes/cm².

Table I
Wafer Stress Constants

Wafer orientation	A	B versus measuring aperture (mm)			
		75	63.5	57.2	51
<100>	6.03×10^{11}	415.4	598.2	738.5	934.7
<111>	7.68×10^{11}	529.4	762.3	941.1	1191

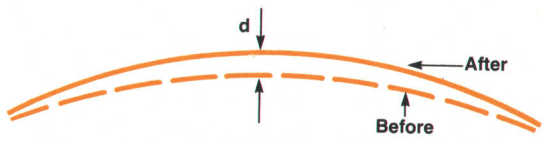


Fig. 1. *Deposition of a film at an elevated temperature on a wafer causes a small change d in surface curvature because of stresses induced by cooling to room temperature.*

Thin Gate Dielectric Films for VLSI MOS ICs: Thermal Silicon Oxynitride

In scaling down the lateral feature sizes of integrated circuit devices to VLSI dimensions, the scaling of the vertical features must also be considered. In particular, the gate dielectric thickness in MOS devices must be reduced substantially to maintain constant power density and increase circuit speed. As the channel length of an MOS transistor is reduced to less than one micrometer, the appropriate gate dielectric thickness becomes as thin as 10 nanometers (approximately 30 to 40 atomic layers of material).

Severe demands will be placed on this very thin gate dielectric film. It must demonstrate a high degree of uniformity and consistency in its chemical, physical and electrical properties among devices, wafers and production runs. It must remain electrically stable and relatively nonconductive even when stressed with high electric fields. It must act as a strong diffusion barrier to contaminants that would otherwise diffuse from the gate electrode into the active channel region and degrade transistor performance. Finally, the film must be intrinsically defect-free (on a per-area basis) and remain defect-free during the rigors of IC processing so that a high device yield can be maintained.

Traditionally, thermally grown silicon dioxide has been used as a viable gate dielectric material at thicknesses down to about 25 to 30 nanometers. There is evidence, however, that when scaled down to 10 nanometers, thermal oxide will not meet the requirements of a good gate dielectric material, particularly in the areas of intrinsic defect density, durability during processing, and resistance to contaminant diffusion. Therefore, other potential gate dielectric materials have been investigated as replacements for thermal oxide in scaled devices.

The most promising new gate dielectric material is thermally grown silicon oxynitride, which is typically produced by reacting ammonia and oxygen with the silicon substrate. A variety of chemical compositions can be produced, primarily dependent on the ratio of ammonia to oxygen. (Note: The oxygen is often unintentionally added because of a finite background level of O_2 in the reaction chamber. Oxygen is always observed in the grown films.) Thermal oxynitrides have been produced in the thickness range from 5.0 to 7.5 nanometers that do not show the shortcomings of thin thermal oxides. The primary drawback of thermal oxynitrides is the extreme thermal cycle required to produce even the extremely thin films mentioned above. Typically the films are grown at temperatures above 1100°C for durations of several hours. Such harsh conditions are not appropriate for VLSI processing.

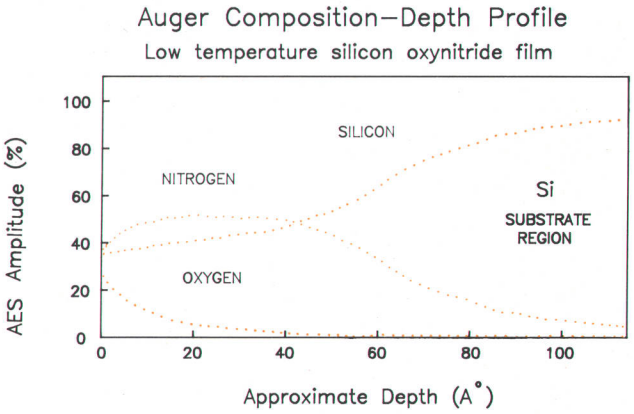


Fig. 1. *Profile of oxynitride film composition versus depth obtained by Auger analysis. Film was grown by plasma-enhanced nitridation at 400°C using NH_3 gas at 0.5 torr and a power level of 400 W for 2 hours.*

To reduce the temperature and time required for the production of oxynitrides, two approaches are being studied. The first involves plasma activation of the growth ambient by coupling RF energy into the reaction chamber to induce a discharge at the wafer sites. A composition-versus-depth profile of a film grown at 400°C using this technique is shown in Fig. 1, demonstrating that a nitride-like composition was achieved. The second approach performs a relatively mild nitridation on an already existing thin (10 nm) thermal oxide film, thereby creating a very thin oxynitride cap on the oxide. Substantial improvement in diffusion resistance against impurities has been observed in films produced in this manner. Further investigation is required to ascertain which of these low-temperature oxynitride schemes will produce the most nearly optimal gate dielectric material.

-Tom Ekstedt
-Hugh Grinolds

nitrogen (again probably containing a considerable quantity of hydrogen). The film thickness uniformity is ±10%, somewhat worse than that observed for the silicon-nitride films. Stress measurements indicate a compressive stress of 10^9 dynes/cm². Cracking, pinhole density, and step coverage measurements show values similar to those observed for the silicon-nitride films. Plasma-etch tests show a maximum etch rate of 51 nm/minute using an oxygen-C_2F_2 gas mixture where the mole fraction of oxygen is 0.6 (Fig. 2).

A process for depositing a silicon-dioxide film with a refractive index of 1.46 was developed using a mixture of silane, oxygen, and argon at a pressure of about 0.85 torr. The film thickness varies more than ±10%, and careful process control must be maintained to avoid particle generation. The equipment vendor offers an increased pumping speed option on the system for improving the quality of this film, but it has not been evaluated. Stress data is similar to that for oxynitride, as are cracking resistance, deposition rate, and plasma-etch data (Fig. 2).

Development Films

PECVD processes have been developed for depositing a variety of films needed to meet different IC fabrication requirements. Among these films are:

- Room-temperature silicon-nitride films

Table I
Thin Films Deposited by HPL PECVD System

Standard films:	Deposition Temperature (°C)	Refractive Index
Nitride	300-400	1.9
Oxynitride	300-400	1.52
Oxide	300-400	1.46
Development films:		
Room temp. nitride	20	1.7-2.2
Very thin nitride	300-400	1.9
Silicon carbide	300-450	2.5-2.7
Amorphous silicon	20-500	—
Polycrystalline silicon	>600	—

- Very thin silicon-nitride films
- Silicon-carbide films
- Amorphous and polycrystalline silicon films

The silicon-nitride film deposited at room temperature has been used successfully in the HPL trilayer resist process[5] described in the article on page 5. Because it has a faster wet etch rate this film appears to be more porous than the standard silicon-nitride film deposited at a higher temperature. Although the thickness uniformity is not as good, step coverage was very conformal, like all the other PECVD films tested. The deposition rate for this film is about 30 nm/minute.

The very thin nitride layer was used for capping polysilicon films which are then laser-beam recrystallized (see article on page 10).[6] The film properties are similar to those of standard silicon-nitride films, except for a much reduced deposition rate (about 10 nm/minute) to obtain better thickness control. Fig. 3 shows the film thickness versus deposition time, and clearly shows the initial thin (roughly 3 nm) native oxide layer as the y-intercept in the curve.

Very smooth, amorphous silicon-carbide films have been deposited over a range of temperatures from 20 to 450°C, using silane and methane (CH_4) as process gases.

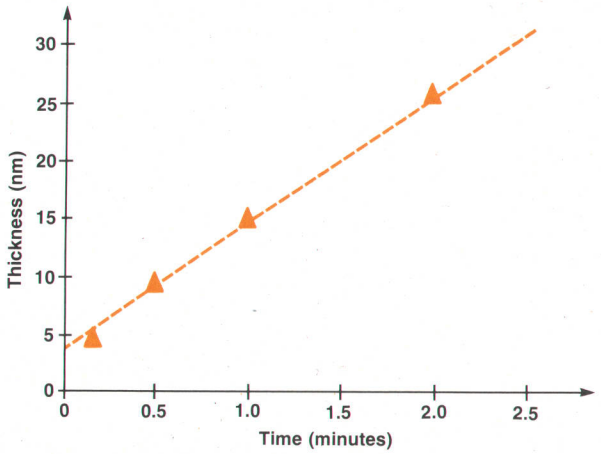


Fig. 3. *The deposited thickness of a very thin silicon-nitride film on a polycrystalline silicon surface versus deposition time. The y-intercept is caused by the very rapid formation of a 3-nm-thick native oxide layer before the deposition cycle.*

Using a gas mixture of silane diluted by argon, silicon films were deposited on silicon-dioxide, silicon, and sapphire substrates at various temperatures up to 630°C. Below 500°C the deposited films were amorphous. Above 600°C the films exhibited a polycrystalline structure as derived from measurements of the light absorption edge by an ultraviolet (UV) spectrophotometer. The typical uniformity of these films is equal to that of the standard silicon-nitride films. It was also observed that the adherence of the silicon film to a sapphire substrate was much improved if an etch clean was performed just before deposition.

Acknowledgments

Useful discussions with R. Rosler of ASM/America and P. Marcoux and F. Schwettmann of HPL are gratefully acknowledged. I. Leal of HPL performed the experiments that provided the data in the figures.

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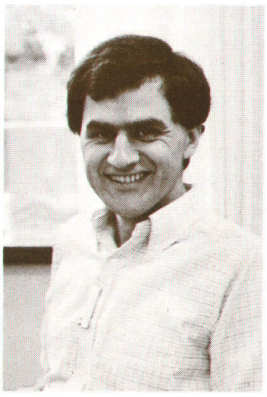


Dragan B. Ilic

Dragan Ilic is a native of Belgrade, Yugoslavia where he attended the University of Belgrade, earning a Dipl. Ing. degree in electrical engineering in 1967 and an MSc degree in physics in 1969. He was awarded the PhD degree in electrical engineering by Stanford University in 1973. Before joining HP in 1980, his professional experience included research work in plasma physics, acoustics, and nondestructive testing. Dragan is a department manager for process technology in the Integrated Circuit Laboratory of HP Laboratories. He is a Senior Member of the IEEE, and author or co-author of over 60 articles and conference papers on plasmas, acoustics, materials testing, and plasma IC processing. He is married, has two children, lives in Palo Alto, California, and enjoys bicycling and eating his wife's gourmet food.

Electromigration: An Overview

The lifetime of the very thin and narrow conductors used in VLSI circuits is largely determined by the operating current density and metallic composition. The predicted lifetimes for various alloys are discussed.

by Paul P. Merchant

THE SHRINKAGE OF IC DIMENSIONS places increased loads on the current-carrying capability of metallization systems. At large current densities electromigration damage can be a major reliability problem because this current-induced metal migration can lead to open-circuit failures in interconnect lines. Because electromigration resistance is a material-dependent property, the type of metallization system used in a particular IC depends on interactions between processing, design and reliability considerations.

Although electromigration phenomena in bulk metals have been studied since the early part of this century, only in the past 15 years has attention been focused on thin polycrystalline metal films used for IC conductors.[1] Transmission electron microscopy, radioactive tracer techniques and marker motion experiments have demonstrated that electromigration occurs because of a current-induced migration of metal atoms along a conductor. Models of the phenomenon begin with a calculation of the average force on a metal atom as the vector sum of an electrostatic force on a screened ion and a carrier "wind" effect resulting from carrier-atom scattering. In aluminum alloys the scattering term dominates and material transport proceeds from cathode to anode as shown in Fig. 1. Under conditions typically encountered in IC metallization systems (10^3 to 10^6 A/cm^2 current densities and temperatures much less than the melting temperature of the conductor) most metal atoms migrate along grain boundaries. If inhomogeneities exist in the conductor, arising for example from temperature gradients or grain-size divergences along the conductor, then the current-induced atom flow is nonuniform and material pile-up and voids occur in the conductor. As the current stressing continues, voids can coalesce to form cracks. This creates smaller cross-sectional areas of the conductor and thus leads to higher local current densities that accelerate the process. Eventually the cross-sectional area becomes so small that the conducting region melts and electrical continuity is lost. Regardless of whether the atom acted on by the current is a lattice atom neighboring a vacancy, or an interstitial or a solute impurity, this model predicts the same behavior for the time to failure (t_f):[1]

$$t_f = \frac{BA^{n+1}}{I^n} \exp\,(E_a/kT)$$

where I is the current, A is the cross-sectional area of the conductor, E_a is an activation energy (typically close to that of grain-boundary diffusion) and T is the absolute temperature. B is a material-dependent proportionality constant which is a lumped parameter containing effects of other

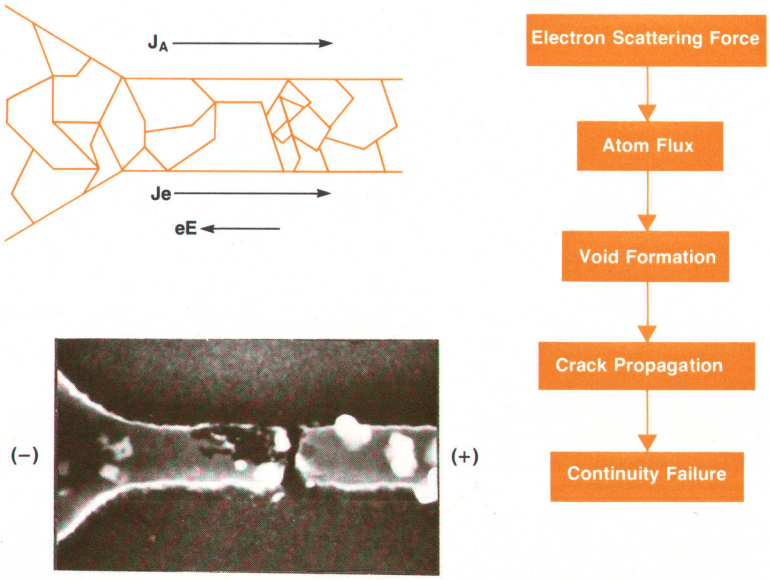


Fig. 1. *Electromigration mechanism showing an idealized conductor (upper left) with directions of electron flux J_E, electrostatic force eE and resultant atomic flux J_A. Scanning electron microscope photograph (lower left) of void formation to the left of the break and accumulation of material in the form of hillocks to the right. The right half of this figure outlines the failure process.*

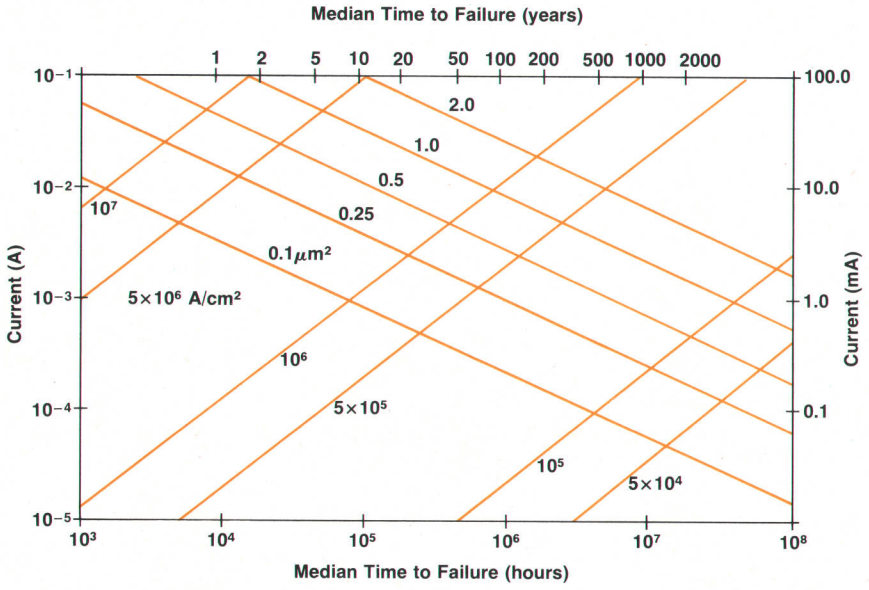


Fig. 2. *Design rules for sputtered Al-Si(2%)-Cu(4%) metallization alloyed at 450°C and operating at 90°C. The axes give median time to failure t_{50} and current. Constant-current-density and conductor cross-sectional-area contours allow easy selection of desired conductor size or current density.*

parameters not explicitly included in the model. The parameter n depends on the type of inhomogeneity responsible for atom flux divergences. For example, n=3 for temperature gradients and n=1 for diffusion barriers or grain-size divergences. Typically, measured values for n are in the range of 2 to 3. Thus t_f is very sensitive to linewidth, which is the principal problem when metallization dimensions are scaled down.

While the more classical diffusion experiments are used in modeling electromigration, most reliability data in the semiconductor industry is obtained from accelerated life testing. A group of about 15 to 20 similar conductors is subjected to constant-current stressing at an elevated temperature and the failure time of each conductor link is recorded. Usually the failure distribution is log-normal and is characterized by a median time to failure t_{50} (at which 50% of the lines have failed) and a parameter $\sigma=\log(t_{50}/t_{16})$ that characterizes the spread of the distribution. When tests are done at several temperatures, with care taken to include corrections for joule heating at large current densities, Arrhenius plots of t_{50} versus link temperature yield the activation energy E_a. Testing at a fixed temperature, using various current densities, yields the exponent n. If tests are done using links with different grain structures, geometries, and substrate conditions, an empirical expression for B can be obtained. The scaling parameters E_a, n, and B are then used to predict the failure distribution for a similar group of conductors under normal operating conditions. Given the constraints of desired reliability, this data allows an IC designer to set design rules for metallization systems with a fair degree of confidence. An example of design rule constraints for sputtered Al-Si(2%)-Cu(4%) metallization is given in Fig. 2.

Although gold is far superior to aluminum in its electromigration resistance, it is not compatible with silicon MOS devices. Aluminum, typically containing 1 to 2% silicon to prevent pitting of contact areas, is the industry standard for such devices. However, circuit dimensions have now reached the size where aluminum can no longer meet the reliability constraints placed on ICs. Several methods have been developed to extend the electromigration resistance of aluminum, such as passivating the surface of the metal with a hard dielectric overcoat or lightly doping the material with impurity metals. The coatings prevent material accumulation and cause stress-generated atom fluxes that oppose the current-driven atom flux, resulting in improvements in lifetime of about 10 times. Impurity doping with metals such as chromium, titanium, magnesium or copper tends to "plug up" the grain boundaries and can extend the lifetime of the metallization system by as much as 200 times with only about a 20% increase in the film's

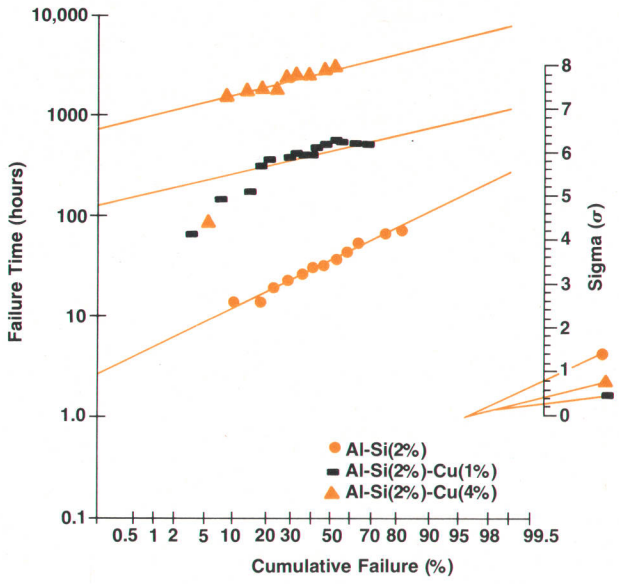


Fig. 3. *Accelerated electromigration life-test plots (log-normal paper) of Al-Si(2%) alloys for different copper concentrations; (●) 0%, (▬) 1%, and (▲) 4% Cu. Test done at 220°C and a current density of 10^6A/cm². t_{50} is found from the intersection of the 50% cumulative failure line and the straight-line fit of the data points.*

resistivity. Copper is a common dopant in production processes where wet chemical etching is used to pattern the metal. However, further development is still needed to obtain a suitable dry etch process for narrow lines. At the present time, such development has generated considerable interest in determining the effect of copper concentration of the electromigration resistance of aluminum alloys because dry etching processes can only successfully pattern aluminum films with less than 1% copper content. Comparative life-test data for sputtered Al-Si(2%) films having 0%, 1%, and 4% Cu added are shown in Fig. 3.

Another approach uses layered structures of aluminum with a transition element such as chromium or titanium, or with oxygen, which after heat treatment can form a hard layer within the metal that blocks crack propagation into neighboring layers.[2] However, the intermetallic formation may in some cases (e.g., $CrAl_7$) cause formation of voids and large tensile stresses that lead to increases in resistivity and lifting of narrow conductor lines.

Even more robust electromigration resistance can be obtained by using refractory metals such as tungsten and molybdenum which are compatible with silicon IC processing and have fairly low resistivities and high melting temperatures. The latter property results from a large activation energy for diffusion. Recent tests of sputtered tungsten films have yielded a t_{50} of 1200 hours under stress at a current density of 4×10^6 A/cm² and a link temperature of 415°C. (If the Al-Si(2%)-Cu(4%) film data is scaled to these stress conditions, the extrapolated t_{50} is only 1.7 hours.) Sputtered molybdenum films have also shown high electromigration resistance that is comparable to that of tungsten. However, the use of tungsten metallization does not allow a complete disregard of current-limit design rules, because at current densities of 1.3×10^7 A/cm² the same sputtered tungsten film glows yellow-white and fails in less than 10 minutes as a result of severe self-heating effects.

Electromigration resistance is also affected by several processing and design parameters. Steps in the underlying topography can result in losses of cross-sectional area in metal lines. Either poor step coverage during metal deposition or a loss of linewidth control during subsequent photomasking can lead to early failures at step edges. Processing goals should include gradual wall slopes and minimum step heights. Circuit layout should strive to minimize metal crossovers at severe steps. Planarization before metal deposition is desirable to prevent these effects. A tradeoff to be considered, however, is that as the underlying insulator thickness is increased, the thermal sinking to the silicon substrate decreases, which leads to earlier failures as a result of the higher link temperature. Accelerated life-test plots illustrating these effects are shown in Fig. 4. If a diffusion barrier is not used, impurity dopants in the metal may also be driven into the substrate. This can result in semiconductor junction poisoning. Another design consideration is the duty cycle, because between pulses, film stresses tend to relax electromigration effects. Obviously, symmetrical ac conditions are desirable for maximizing the lifetime of a given metallization system.

The final choice of a metallization system for a particular type of IC depends on interactions between several constraints imposed by processing ease, and compatibility, circuit design, layout and reliability requirements. Accurate predictions of a metallization system's reliability can only be made from accelerated test data on realistic simulations of target vehicles. To achieve this goal it is important that all persons involved in processing and design be aware of the effects of their decisions on the reliability of the finished product.

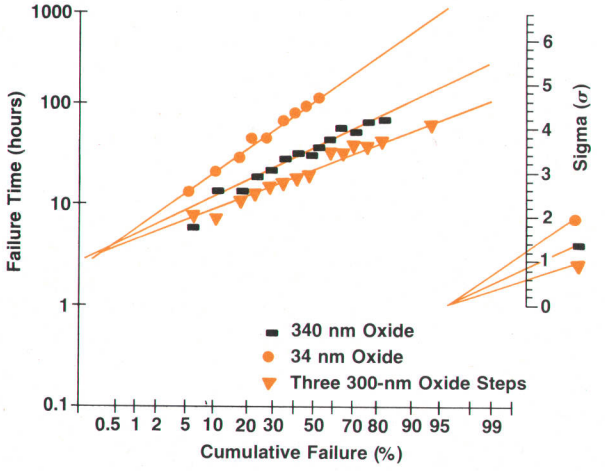
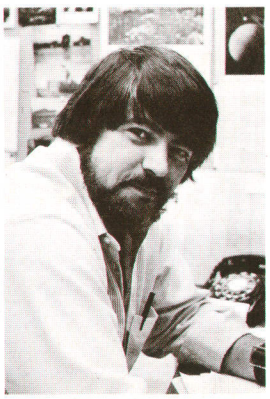


Fig. 4. *Accelerated electromigration life-test plots of sputtered Al-Si (2%) 2-μm² conductors, 100 μm long. The stress conditions are a current density of 1×10^6 A/cm² and a temperature of 220°C. The different underlying substrate surfaces are (●) 34-nm-thick planar SiO_2, (▬) 340-nm-thick planar SiO_2 and (▼) the same surface as (▬) with three vertical-walled, 300-nm-high SiO_2 steps.*

Acknowledgments

The test structures used in evaluating the electromigration properties of candidate metallization systems are the result of the combined efforts of several persons in HP's IC



Paul P. Merchant

Paul Merchant was born in Burlington, Vermont, and attended the University of Vermont for a BS degree in physics (1972) and Brown University for the ScM (1974) and PhD (1978) degrees, also in physics. He did postdoctoral work in photoelectrolysis at Brown University for one year and in stoichiometric laser materials at Centre Nat'l de la Recherche Scientifique, Bordeaux, France, for one year. Paul then joined HP in 1979 and has done R&D work related to electromigration, dry etching, and silicide contacts and interconnects. His contributions have resulted in several papers on II-VI compounds, transition metal oxides, and laser materials. He is a member of the American Physical Society, Sigma Xi, and the American Vacuum Society, and has taught classes on IC metallization technology. Paul is married, lives in Menlo Park, California, and enjoys playing softball, racquetball, chess, keyboards, and guitar.

Processing Lab (ICPL) for standard processing and Integrated Circuits Lab (ICL) for unit processes currently under development. In particular, Joyce Sum of ICPL has provided the bulk of the metal depositions necessary for these studies. Assistance in testing and sample preparation and in metal film structural analysis was provided by Gladys Koke and Tom Cass, respectively, of ICL. The Systems Technology Operation at HP's Fort Collins, Colorado division kindly supplied the sputtered tungsten films.

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SWAMI: A Zero-Encroachment Local Oxidation Process

Lateral oxidation limits density in oxide-isolated VLSI circuits. This process removes this limit by using a novel sequence of conventional processing techniques.

by Kuang Yi Chiu

AS DEVICE DIMENSIONS continue to shrink in the drive toward productivity and performance improvements, processing technology improvements will be of major importance in achieving these goals. Electron beam and X-ray lithography, dry etching, and ion implantation processes make it possible to fabricate devices with compatible interdependent requirements for image resolution, edge definition, step coverage, and functionality at geometries at or below the one-micrometer level. However, the limits of certain aspects of the technology still exist. Device isolation is one of the major issues to consider for achieving high device packing density for VLSI. Local oxidation of silicon (LOCOS)[1] has been widely used for the isolation of active components of silicon LSI circuits because it offers several advantages over other isolation technologies, such as surface planarity, improvement in packing density, and compatibility with existing LSI processing techniques. However, reducing LOCOS device dimensions for VLSI aplications is limited by severe encroachment resulting from the lateral oxidation, or bird's beak (see Fig. 1), under the edge of the isolation mask and diffusion of the channel-stop doping into the active device area.

The channel narrowing resulting from the LOCOS process, approximately two to three times the field oxide thickness, has been small enough that it has only a small effect at minimum widths of 4 to 5 μm and is almost unnoticeable for channel widths greater than 5 μm. When devices are scaled down to micrometer and submicrometer levels, the field oxide has to scale down in thickness to control the lateral encroachment to an amount reasonable for dense layout ground rules. However, because of the

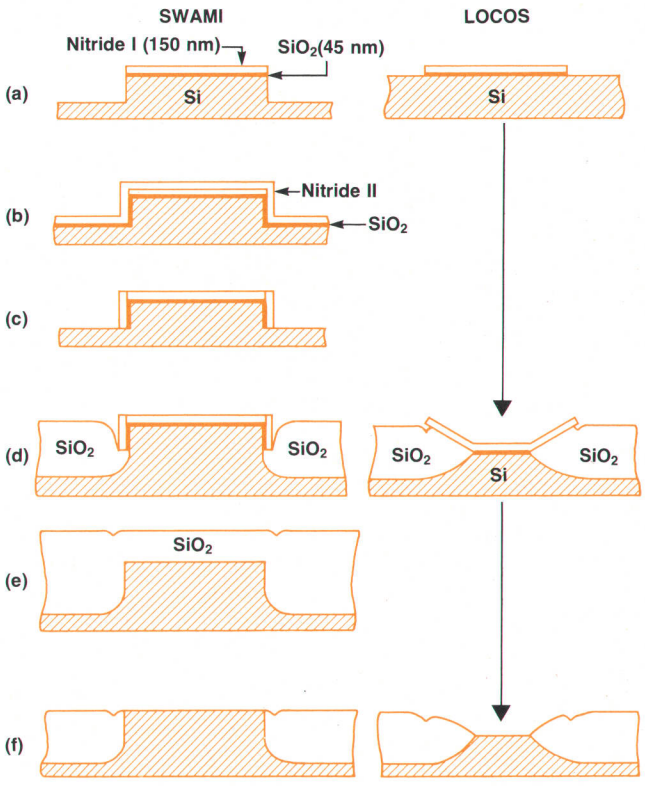

Fig. 1. *Comparison of SWAMI process with conventional LOCOS process. (a) After island patterning and etching. (b) After nitride II deposition (SWAMI only). (c) After nitride II etching (SWAMI only). (d) After field oxidation. (e) After nitride removal and LPCVD oxide refill step (SWAMI only). (f) Finished isolation structure before gate oxidation.*

Table I
SWAMI Process (see Fig. 1)

1. Grow stress-relief oxide (SROI)
2. Deposit silicon nitride (nitride I)
3. Pattern island region (masking)
4. Plasma etch Si_3N_4 and SiO_2
5. Plasma etch silicon step
6. Grow stress-relief oxide (SROII)
7. Deposit silicon nitride (nitride II)
8. Plasma etch nitride II
9. Grow isolation field oxide
10. Strip nitride (wet etch)
11. Deposit and densify LPCVD SiO_2
12. Etch back SiO_2

reduced field oxide thickness, the interconnect capacitance increases proportionately and VLSI circuit performance is degraded. Experiments have been reported in which this undesirable feature caused by the LOCOS approach is minimized. However, either the bird's beak still exists (to a reduced degree) or the approach requires the use of complex or unconventional processing techniques.

A side-wall-masked isolation (SWAMI) process using anisotropic plasma etching of silicon and silicon nitride/oxide was developed to form a zero-encroachment and fully recessed isolation structure. The SWAMI process almost completely eliminates the reduction in effective channel width from defined mask dimensions. The process uses only conventional LSI processing techniques and no additional masking step is required. Table I outlines the sequence of steps in the fabrication process to form the isolation structure. The process is similar to the conventional fully recessed oxidation process except that steps 6, 7, 8, 11, and 12 are needed to form this encroachment-free isolation scheme. Fig. 1 illustrates schematically the major processing steps that deviate from the conventional LOCOS approach. The stress-relief oxide is thermally grown at 1000°C in a dry ambient followed by nitrogen annealing for 20 minutes. The silicon-nitride films are low-pressure chemical-vapor deposited (LPCVD) at 800°C in a 4:1 volume ratio of NH_3:SiH_2Cl_2. Positive photoresist and direct-step-on-wafer (DSW) projection were used throughout this study for pattern definition. The nitride and oxide are etched by C_2F_6 plasma[2] and the silicon step is etched by CCl_4/C_2F_6 plasma.[3] A boron channel-stop implant is performed after the silicon step etching. A second stress-relief oxide is grown and the nitride II layer is then deposited.

A strongly unidirectional plasma nitride etch is then used to remove the nitride II lying on the planar surface such that the edge of the island is covered by nitride II and the top island surface is protected by nitride I. The field oxide is then grown in a wet environment and the nitride films are stripped in boiling phosphoric acid. A layer of 500-nm-thick LPCVD oxide is deposited and etched back by plasma oxide etching such that a thin layer, approximately 50 nm thick, of oxide is left on the gate region. A short, wet oxide etch is then performed to remove the remaining thin oxide to prevent possible contamination of the gate region by the plasma and to avoid reformation of the notch at the edge of the silicon island. A comparison of conventional LOCOS and SWAMI isolation structures before gate oxidation is illustrated in Fig. 2.

Experimental results and detailed analysis of MOSFET devices fabricated using this newly developed SWAMI process have been presented in other publications.[4,5]

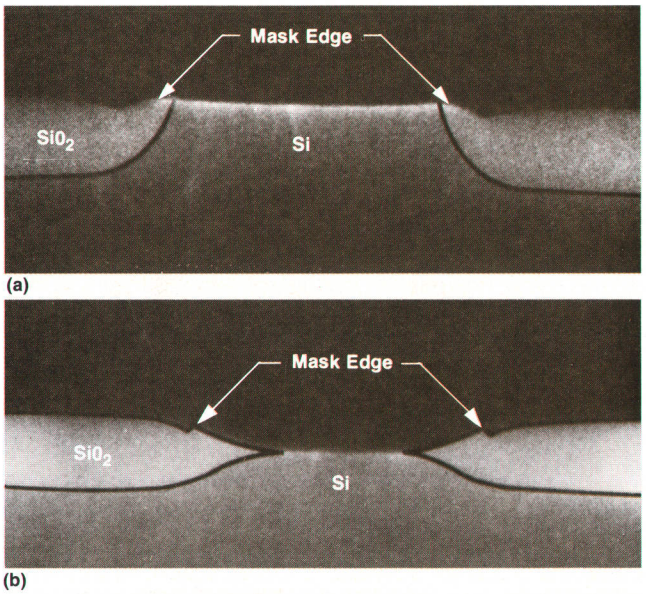

Fig. 2. *Microphotograph of (a) SWAMI structure compared to (b) LOCOS structure before gate oxidation.*

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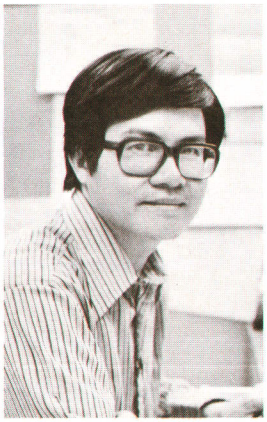

Kuang Yi Chiu

Kuang Chiu was born in Taiwan and educated at the University of Sourthern California where he received a PhD degree in material science in 1974. He joined HP in 1979 with six years experience related to InSb infrared sensor arrays and radiation effects on MOS devices. Kuang is currently working on MOS/VLSI process development. He is a co-author of nine articles related to the areas he has worked in and is a member of the IEEE. Kuang enjoys fishing, camping, playing bridge, and sports. He lives in Palo Alto, California, is married, and has a son and a daughter.

Trench Isolation Technology

In recent years, there has been increasing interest in complementary metal-oxide-semiconductor (CMOS) technology for its low power dissipation, large operating voltage margin and superior noise immunity. As the density of integrated circuits continues to grow, the power dissipation advantage makes it clear that CMOS will be a major VLSI technology. However, there is one factor working against CMOS in scaling device dimensions down, the latch-up problem.

Fig. 1 illustrates the cross section of a CMOS inverter with the two-transistor (pnp and npn) equivalent circuit superimposed. Latch-up can be created in the parasitic pnpn path by the positive feedback between two coupled bipolar transistors, producing a regenerative switching and allowing large currents to flow. Certain minimum spacing between n- and p-channel transistors is required to prevent this latch-up. Therefore, the spacing cannot be reduced as much as the transistor dimensions.

The trench isolation technology provides a possible solution to this scaling problem. As shown in Fig. 2, when a deep and narrow trench is etched into the silicon substrate and refilled with dielectric material, the spacing between two transistors can be minimized without increasing the potential for latch-up.

Besides the CMOS latch-up prevention, dielectric refilled trenches can also be used for general device isolation in bipolar and MOS integrated circuits.

For circuit density, the trenches need to be as narrow as possible. The current optical lithography technology limits their width to no less than 1 μm. The trench depth is approximately 5 to 8 μm, depending upon device structures and doping profiles.

To form such deep and narrow trenches, the etching must be highly anisotropic, forming vertical sidewalls with no lateral undercuts. This characteristic has been demonstrated by reactive ion etching. The cross section of a refilled trench taken with a scanning electron microscope (SEM) is shown in Fig. 3. The refill technique depends upon two processes: conformal coating and etching back anisotropically. The low-pressure chemical-vapor deposition of the dielectric material results in equivalent deposition rates on the trench sidewalls and the silicon surface. Trenches 1 μm wide can be sealed with a 0.5-μm-thick deposition. The deposition is followed by an anisotropic etch of the surface-deposited layer. Thus, a reasonably planar surface can be obtained as shown by the SEM view.

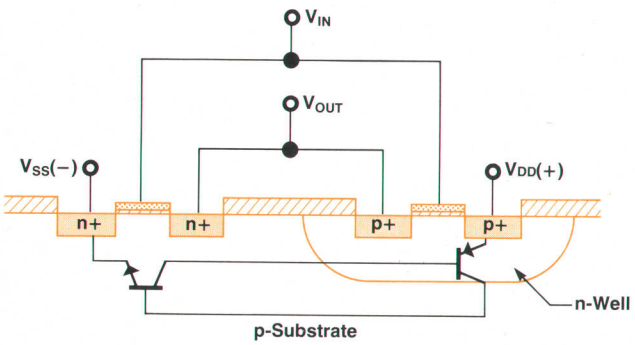

Fig. 1. *Cross section of CMOS inverter structure with the two-transistor equivalent circuit superimposed. This transistor combination can act as a lateral SCR structure that will turn on when large currents are passed, if the spacing between the transistors is small enough to permit regenerative feedback.*

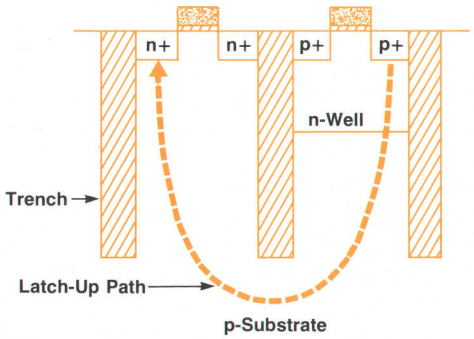

Fig. 2. *By etching a deep trench between the two transistors in Fig. 1 and refilling the trench with a dielectric material, the transistors can be spaced closer together, but the path for regenerative feedback will still remain long enough to prevent latch-up.*

Potential problems that may be introduced by trenches are trench sidewall inversion and surface topography. The former can cause MOS transistors to be leaky or to short through the inversion path. The latter can cause a nonplanar surface on the top of the refilled trench, creating the potential problem of breaks in any conductive lines that run across the trench.

Some MOS transistors surrounded by trenches have been successfully fabricated. These devices have electrical behavior very similar to devices without trenches, showing no residual leakage currents above the 1-pA range. The yield was also about the same as for the nontrench devices after a large number of devices were tested.

-Shang-yi Chiang

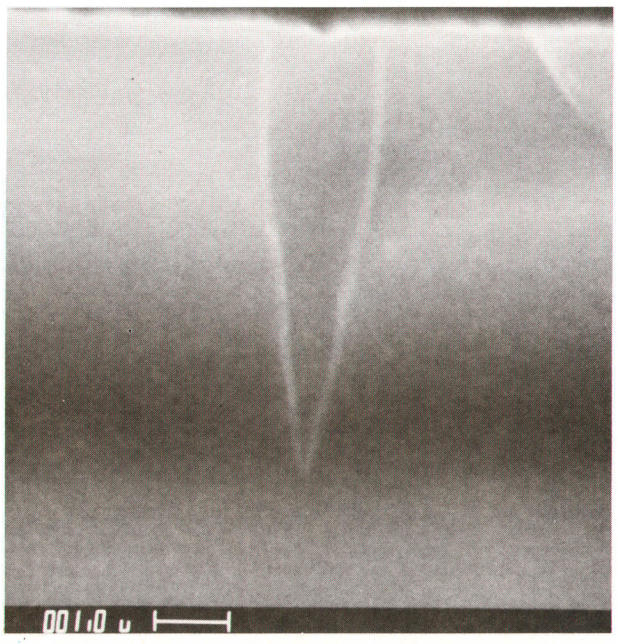

Fig. 3. *Cross-sectional microphotograph of a refilled trench.*

High-Pressure Oxidation

Oxidation of silicon at atmospheric pressure requires considerable time and high temperatures that can be detrimental to the results of previous process steps. Increasing the oxidant gas pressure allows reduction of time and/or temperature for a desired oxide thickness.

by William A. Brown

THE THERMAL OXIDATION OF SILICON is the most basic, and typically the most often performed process in many of today's fabrication technologies used to build integrated circuits and discrete devices. This is confirmed by the presence of high-temperature furnace systems and associated support equipment usually occupying between 30% and 40% of the area in most clean rooms dedicated to silicon IC manufacture. Until recently, the various processes for the oxidation of silicon were exclusively performed at atmospheric pressure. Starting in 1960[1] a number of investigators began to study the influence of pressure on the growth of thermal oxides on silicon. Their studies were performed on R&D-size systems and while their findings were technically significant, high-pressure silicon oxidation was not seriously considered for integrated circuit fabrication.

In 1977, however, Tsubouchi and coworkers[2] at Mitsubishi in Japan reported on a production-size system developed jointly with an affiliate of an American equipment vendor. Since then there has been a renewed interest in high-pressure oxidation and the introduction of full-scale production systems by two American equipment manufacturers. The new popularity of high-pressure oxidation as applied to silicon processing is based on the influence of pressure on the kinetics of the thermal oxidation of silicon, allowing pressure to be substituted for temperature in growing silicon-dioxide films. (A general lowering of temperatures of most furnace operations is considered essential to move from LSI to VLSI levels of device integration.) To explore the application of high-pressure processing to various integrated circuit development programs under way at Hewlett-Packard, a commercial high-pressure oxidation system was installed (Fig. 1) in HP's Integrated Circuit Laboratory (ICL).

Theory

In general, pressure oxidation kinetics can be explained by a model developed in 1965.[3] Equation (1) shows one form of the so-called general relationship for the thermal oxidation of silicon.

$$t = \frac{x^2 - x_o^2}{B} + \frac{x - x_o}{B/A} \qquad (1)$$

Here, the time t to grow a film of thickness x is related as indicated, where x_o is the oxide thickness at time zero. This relationship describes the oxidation of silicon as occurring in two overlapping regimes—linear and parabolic—characterized by rate constants B/A and B, respectively. B/A is related to the chemical bonding that occurs at the oxide-silicon interface during the growth of an SiO_2 film, whereas B is related to the diffusion of the oxidant through the growing oxide film. The key to pressure oxidation lies in the relationship between B and C*, the equilibrium concentration of oxidant (O_2 and H_2O) in the SiO_2 layer. This relation is

$$B = 2DC^*/N_i$$

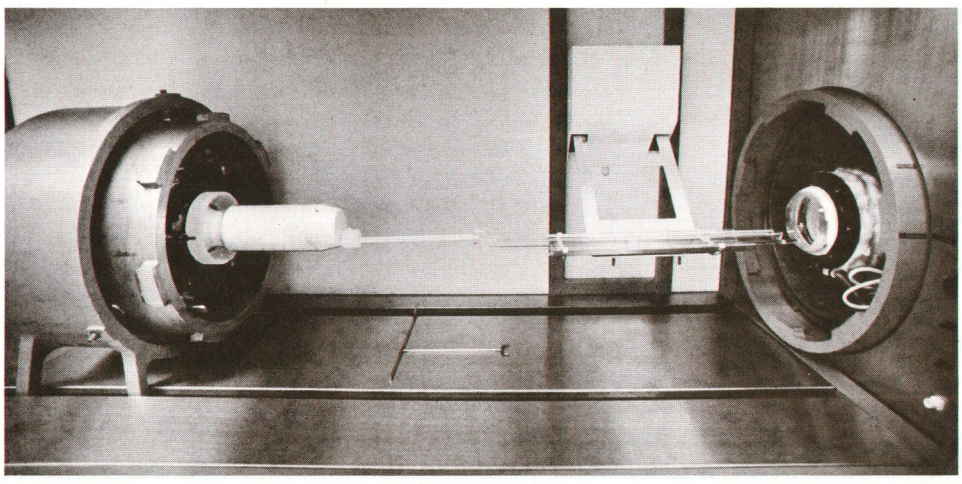

Fig. 1. *Operator's view of HP's high-pressure oxidation system. After the quartz carrier (center) is loaded with wafers to be oxidized, it is inserted into the chamber on the right and the chamber is sealed with the end cap shown on the left.*

where D is the diffusivity of the oxidant and N_i is the number of oxidant molecules per unit volume of the oxide. C* is directly proportional to the partial pressure p_{ox} of the oxidant in the surrounding ambient atmosphere; therefore as p_{ox} increases, so does C*.

An example of the effect of steam pressure on the parabolic rate constant B is shown in Fig. 2. It is seen that B can increase by 5 to 10 times its value at atmospheric pressure, given a very moderate increase in the pressure of the oxidation ambient gases. As shown in Fig. 3, B/A is likewise influenced by pressure. At 900°C, for example, B/A increases by a factor of 20 when the pressure is increased from 1 atmosphere (1.033 kg/cm²) to 15 kg/cm².

Applications

What does high-pressure oxidation offer for integrated circuit fabrication? Some features of this technology are itemized in Table I. An acceleration in the growth rate of the thermal oxide film provides the process designer two options. First, one can retain the temperature and time of an existing atmospheric-pressure process and take advantage of the enhanced growth rate associated with high pressure. It has been observed that, compared to atmospheric-oxidation conditions, the growth rate at an elevated pressure P increases nearly linearly with P. Second, one may choose to lower the temperature of an existing oxidation process by performing it at elevated pressure while retaining the atmospheric pressure growth rate so as not to impact the throughput of a given operation. Typically, for every one-atmosphere increase in pressure it is possible to lower the oxidation temperature by up to 30°C without changing an established oxidation. It is this latter option that has prompted the current interest in high-pressure oxidation.

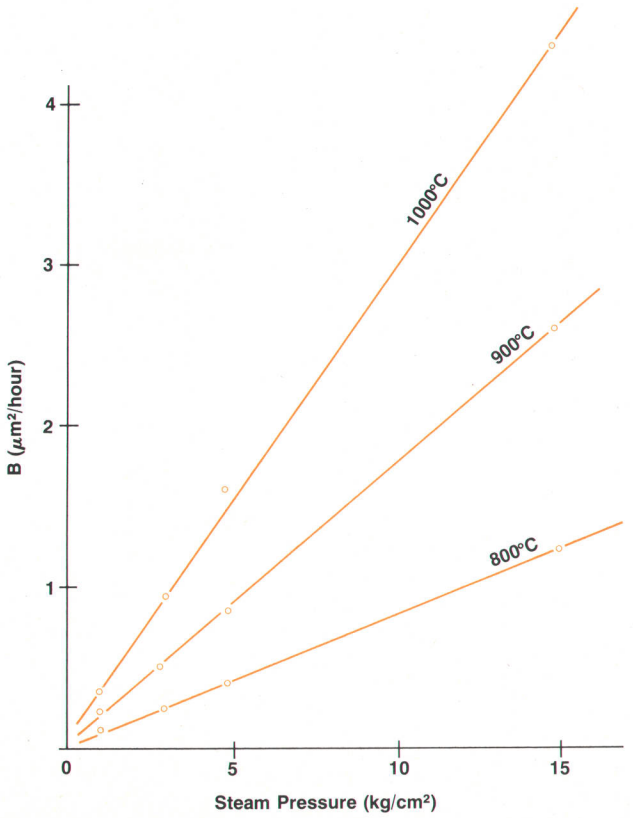

Fig. 2. *Effect of steam pressure on the parabolic rate constant B for <100> silicon surface orientation.*

Table I
Features of High-Pressure Oxidation

1. Accelerated oxidations
2. Low-temperature processing:
   - Less warping of large-diameter wafers
   - Less effect on pn junction location
     - x_j (vertical and lateral)
   - Fewer oxidation-induced stacking faults[4]
   - Denser oxides (higher refractive index)
   - Reduced dopant segregation at the Si/SiO_2 interface
3. Offers a new dimension in silicon processing

Low-temperature oxidations provide the benefits outlined in item 2 of Table I. Of particular significance to circuit yields has been the reduction in various oxidation-induced stresses and structural defects in the underlying silicon that has been observed as a result of high-pressure oxidation.[4] As device densities and chip size increase toward VLSI levels of integration, structural perfection will be required of both the oxide and the silicon. Lastly, adding a third dimension to the oxidation process will permit the development of new device structures in the future.

Equipment

The high-pressure oxidation system in HP's Integrated Circuit Laboratory (Fig. 1) is capable of establishing operating pressures up to 25 atmospheres in a variety of ambients. For oxidation, either dry oxygen or water-injected steam environments may be established at any temperature between 500 and 1000°C. The system uses a quartz paddle for wafer transport (shown supported by an elevator mechanism in Fig. 1) attached to a quartz end cap inside a movable sealing door. Wafer oxidation takes place inside a quartz tube that resides within a heating element that is enclosed within a water-cooled pressure vessel. During processing the pressure in the quartz tube is always positive with respect to the vessel (to minimize wafer contamination) and gases continuously flow through both vessel and tube. A microcomputer is dedicated for control of all process parameters as well as operation sequencing. Safety of operation is assured through hardwired alarms that can automatically abort a process and return the system to atmospheric pressure. The pressure vessel is outfitted with rupture discs to relieve any unintended overpressurization. The system is capable of processing up to 250 75- or 100-mm-diameter wafers.

Status

In the last few years an increasing number of reports dealing with various aspects of high-pressure silicon oxidation have appeared in the technical literature. At present sufficient data on high-pressure oxides has been developed to permit their use at most of the oxide growth steps found in a typical integrated circuit process. In addition, some

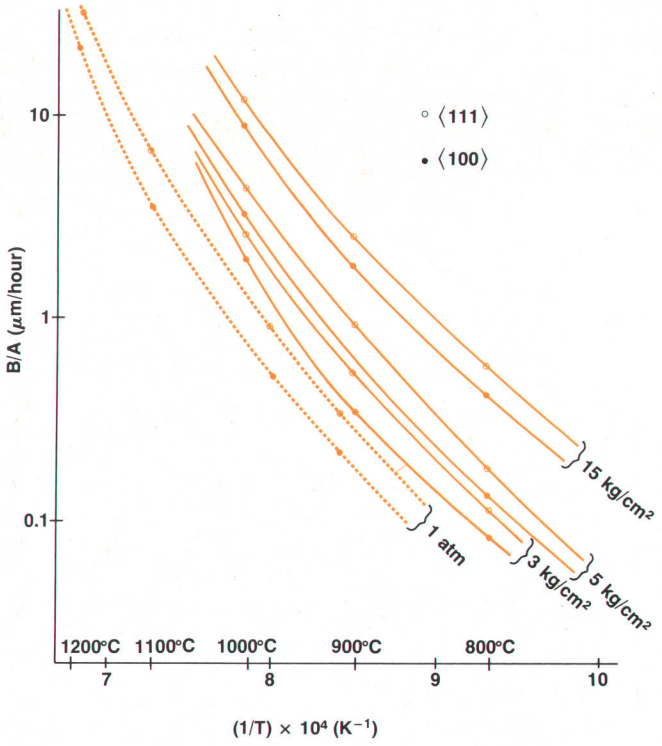

Fig. 3. *Effect of temperature and pressure on the linear rate constant B/A for <111> and <100> silicon surface orientations.*

investigators have observed improved device performance when atmospheric-pressure-grown oxides are replaced by films grown in a high-pressure oxidation system. Several domestic semiconductor companies are already using a high-pressure oxide growth operation as the basis for their oxide-isolated bipolar IC products.

At ICL the focus of current work is aimed at improvements in device structures and density that can be realized by accelerated oxidations. Research into other applications of high-pressure silicon processing, such as implant activation, electronic charge neutralization, and novel film forming processes, is being planned. It is clear that high-pressure oxidation will play a critical role in future integrated circuit processing technology.

Acknowledgments

Several people have contributed to establishing a high-pressure oxidation capability in Hewlett-Packard Laboratories. They are, in random order, Rick Dalla, Armando Iturralde, Dave Thrasher, Dan Cropper, Conrad Dell'Oca, Eileen Murray, Bob Grimm, Pat Castro, and Fred Schwettmann. Their ideas and support are gratefully acknowledged.

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William A. Brown

Bill Brown is a production process engineer at HP's Integrated Circuit Division, Santa Clara, California. He joined HP in 1975 with several years of product and process engineering experience in the commercial IC business. His work at HP and elsewhere has focused on high-temperature IC processing, resulting in several papers and two patents. Born in Remsen, New York, he attended Niagara University, earning a BS degree in chemistry in 1958, and Rensselaer Polytechnic University, earning a master's degree in metallurgical engineering in 1961. Bill is a member of the American Vacuum Society, has taught courses in silicon IC processing at HP and a local college, and recently spent three months in Korea helping the Korean Institute of Electronic Technology set up an IC fabrication facility. Bill lives in San Jose, California, is married, has two children, and is interested in personal computers and youth motocross racing.

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