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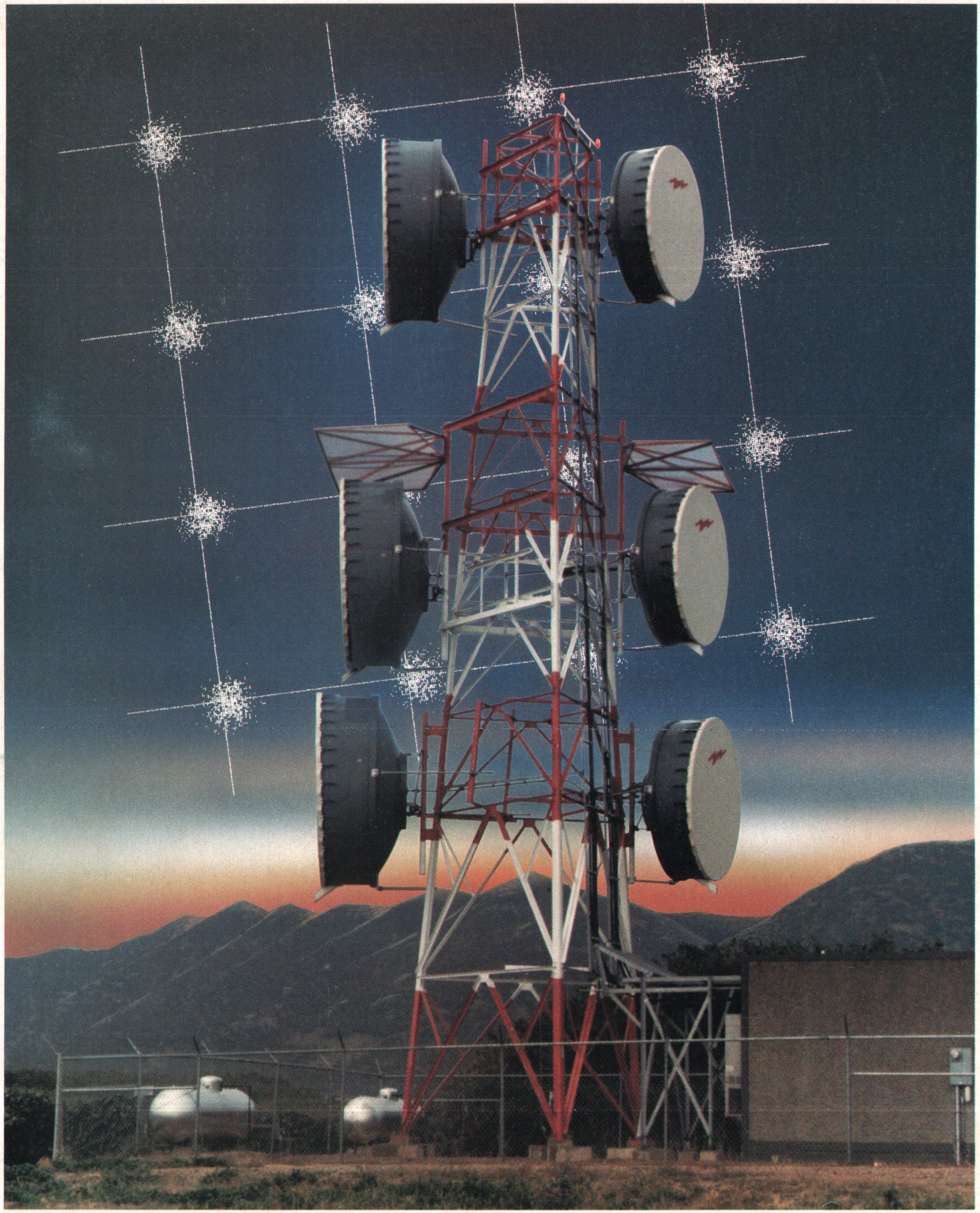

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Articles

Departments

In this Issue

Behind many of the microwave antenna towers one can see riding the tops of ridges and tall buildings are digital radio systems, that is, systems in which the information is imposed on the microwave carrier signal by digital modulation techniques. Two instruments for testing digital radios are the subjects of this issue.

One important measure of the performance of a digital radio is the bit error rate, or BER. What portion of the data bits being transmitted can be expected to be corrupted by noise? One in a million? One in ten million? The answer depends, as one might expect, on typical radio conditions like fading and interference. If the carrier power fades by as little as 10%, the BER can get ten times worse. The HP 3708A Noise and Interference Test Set is designed to inject precise amounts of noise and interference into a digital radio so the effect on the radio's BER can be measured. The design and theory of operation of this instrument are presented in the papers on pages 19, 26, and 30, and on page 36 is a description of an automatic test system for BER tests of digital radios in production. Among the engineering challenges faced by the HP 3708A's designers were how to maintain a precise carrier-to-noise power ratio when the carrier power is changing, how to guarantee that the noise has not only the required power level but also high enough peaks to approximate real noise, and how to get both fast response and high accuracy in microwave power measurements.

There are many different digital modulation techniques in use today. They have names like QPSK, 49QPR, and 64QAM, where the Q stands for quadrature. The modulation signal has two components, called in-phase (I) and quadrature (Q), each of which can assume only a finite number of values and will have exactly one of these values when the receiver samples the signal. In 64QAM, for example, which means 64-state quadrature amplitude modulation, I and Q can each take on eight values ($8 \times 8 = 64$). If you were to plot the I and Q values received in such a system, the plot should look like a regular 8×8 grid of 64 dots. Because of noise and other impairments, an I-versus-Q plot for a real digital radio more often consists of clusters of dots, and the grid may be distorted. The nice thing is that you can tell a lot about how the radio is performing by looking at such a plot, which is called a constellation diagram. There's one on the cover, and you'll find others in the papers on pages 4 and 13, which describe the design of the HP 3709A Constellation Display. This special-purpose display adapts to various digital modulation schemes at the flip of a switch, and not only displays the constellation diagram but also computes statistics of the dot clusters and various distortion parameters. Among the design challenges were how to minimize timing jitter in the sampling circuit and how to deal with display distortion, which can mimic distortion in the digital radio.

-R. P. Dolan

What's Ahead

The design and development of the HP-18C and HP-28C, HP's latest handheld calculators for business and technical professionals, are the subjects of the August issue.

The HP Journal encourages technical discussion of the topics presented in recent articles and will publish letters expected to be of interest to our readers. Letters must be brief and are subject to editing. Letters should be addressed to: Editor, Hewlett-Packard Journal, 3200 Hillview Avenue, Palo Alto, CA 94304, U.S.A.

Dedicated Display Monitors Digital Radio Patterns

One way of displaying the complex waveforms generated in digital radio systems is the constellation display, a method that allows rapid visual evaluation of a system's performance.

by David J. Haworth, John R. Pottinger, and Murdo J. McKissock

THE HP 3709A CONSTELLATION DISPLAY (Fig. 1) is a specially engineered two-channel sampling oscilloscope for monitoring the eye and constellation patterns in a digital radio. Although called digital radio because the input is digital, much of the circuitry is analog and the design of a digital radio is an exercise in high-performance analog and digital design. The waveforms are random multilevel wideband signals, and require a high-performance sampling oscilloscope to display them. The HP 3709A design goals were high performance, low cost, ease of use, quality, and manufacturability.

Because the instrument is dedicated to one application, it has some novel features such as user-selectable graticules and dedicated constellation measurements. Many of the controls have been simplified for easier use. The time base autoranges to display two complete cycles of the input waveform. The usual trigger and trigger mode controls are not necessary because the instrument triggers from a clock waveform supplied by the radio. The samplers have been optimized for use on random signals and do not have the dot response problems of earlier sampling oscilloscopes.

A choice of internally generated graticules can be selected by a rear-panel switch to correspond to commonly used modulation schemes: QPSK, 9QPR, 16QAM, 49QPR, and 64QAM (see references 1 through 4 for discussions of these modulation methods and other digital radio fundamentals). For 16QAM, a 4×4 graticule is displayed and for 49QPR, a 7×7 graticule is displayed. Alphanumeric information is also presented to display instrument status, self-test messages, and results of the dedicated measurements. A hard copy of the constellation can be output by the HP 3709A on an HP ThinkJet Printer via the HP-IB (IEEE 488/IEC 625). See Fig. 9 on page 17 for a sample printout.

The two input channels are labeled I (in-phase) and Q (quadrature) instead of Channel A and Channel B because this is how the typical customer refers to the two radio channels.

There are four modes: constellation, I eye, Q eye, and measure, selected directly by dedicated keys. In eye mode the HP 3709A operates as a conventional oscilloscope with volts indicated on the Y axis and time base sweep on the X axis. A typical eye diagram is shown in Fig. 2. Constellation mode is what some oscilloscopes label A versus B. This mode displays a sampled instant of the I signal on the X axis and the Q signal on the Y axis. In this mode there is no time base sweep, the same point on the waveform is sampled every time, and timing jitter performance must be good.

The displayed I and Q signals are controlled by a group of dedicated controls whose sensitivity is displayed on the CRT. The samplers are calibrated every three minutes to eliminate gain and offset errors. A delay control allows the user to move the sampling instant to the position of maximum eye opening. The two data inputs are normally sampled at the same instant, but two additional delays can

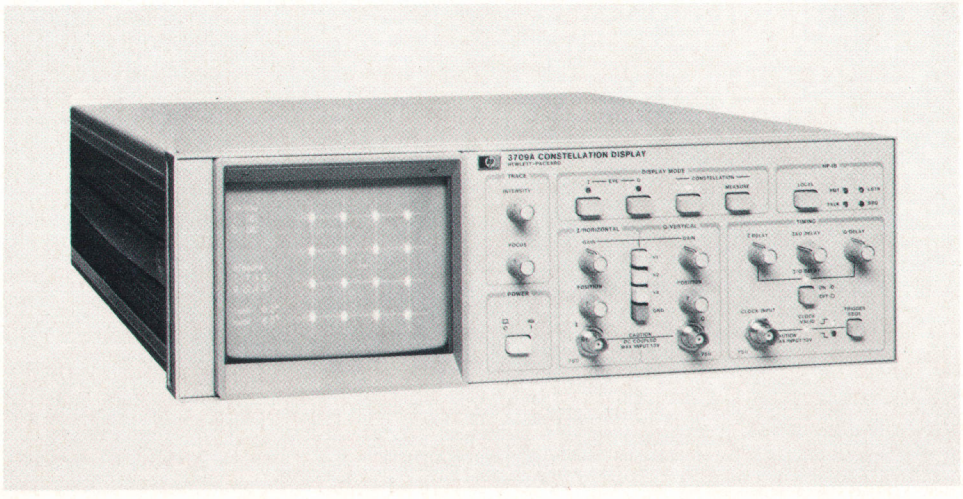


Fig. 1. *HP 3709A Constellation Display.*

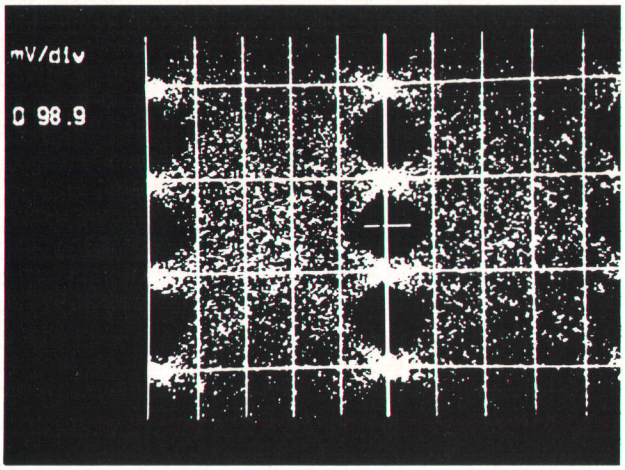


Fig. 2. *Eye diagram viewed on an HP 3709A. Looking grainy because the display is sampled, the eye is in the center with a bright line marker.*

be enabled to move the sampling instants independently. A trigger edge select key completes the user controls.

Fig. 3 shows the baseband signals and symbol clock for a typical modulation scheme, 16QAM. The signals are sampled at instants defined by the symbol clock generated within the digital radio receiver. The I and Q signals have discrete values when the active edge of the clock occurs. The eye has four discrete levels at the correct sampling instant for 16QAM signals. An ideal constellation is a single point for each modulation state and the whole pattern is aligned to the graticule. However, the typical constellation (Fig. 4) shows clusters instead of points because of imperfections in the radio. Similarly, the eye diagram is not a single line but many overlapping lines generated by the distortion of the data flowing through the radio.

Usually there are impairments causing small amounts of noise and geometric distortions of the constellation. The

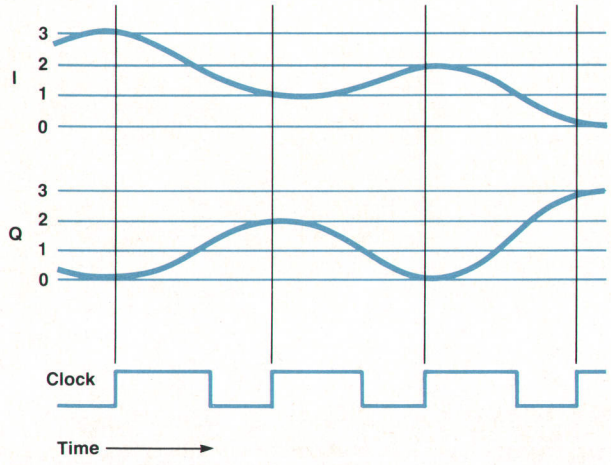


Fig. 3. *Typical baseband and symbol clock waveforms for a 16QAM radio system. The two channels, I and Q, have four possible states: 0, 1, 2, and 3. The waveforms are filtered to conserve bandwidth, so they look more sinusoidal than square. At the valid edge of the clock (leading edge) the I and Q data will be at one of the four levels.*

MEASURE key takes 600 samples from the constellation, calculates values for several common impairments, and displays these as numbers on the CRT (see article on page 13). The sampled data is also available over the HP-IB for further analysis by a computer.

Hardware Design

A block diagram of the instrument is shown in Fig. 5. The sample-and-hold circuit is similar to that used in conventional HP sampling oscilloscopes except that it is reset to zero between each sample. Digital radio waveforms are random multilevel signals and viewing these normally requires careful adjustment of a sampling oscilloscope to avoid excessive noise caused by intersymbol interference. By resetting the circuit between samples, the HP 3709A is free of intersymbol interference by design, and therefore is easier to use.

The sample-and-hold circuit consists of a four-diode sampling gate and holding capacitor followed by a stretcher circuit (Fig. 6). The input signal is sampled by switching on diodes D1 to D4 for about 1 ns. The hold capacitor C1 is charged to about 10% of the voltage appearing at the input to the gate. The charge on C1 decays rapidly, but the impulse on the base of Q1 causes an output waveform at its collector proportional in amplitude to the input voltage but stretched in time over several microseconds. The first half cycle of this waveform is integrated and the output of U1 is a voltage proportional to the input voltage. By varying the time switch S1 is closed, the gain can be varied. An autocalibration loop is used to maintain unity gain over a wide temperature range.

The waveforms in Fig. 7 show the circuit's operation. The input signal is a four-level pseudorandom binary sequence (PRBS) generator which is representative of a digital radio signal. The upper trace is the output of the impulse generator and is a damped resonance proportional in amplitude to the input signal but fixed in frequency. The lower trace is the integrator output.

Time A is when the sample is taken. The signal is then integrated from A to B, during which time S1 is closed. At time B the output of the integrator is equal to the input

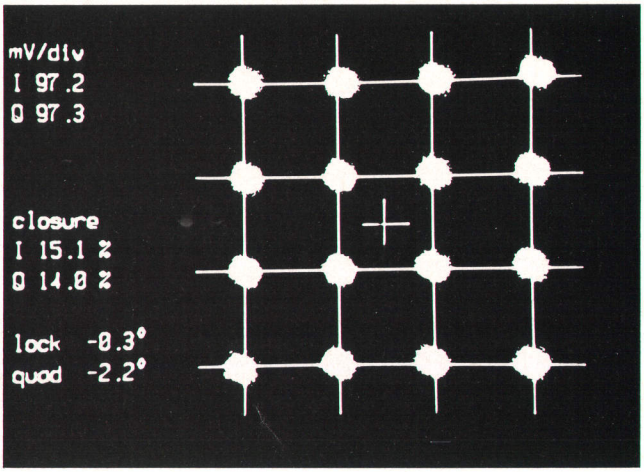


Fig. 4. *Constellation display on an HP 3709A with measurements of closure, lock angle, and quadrature angle.*

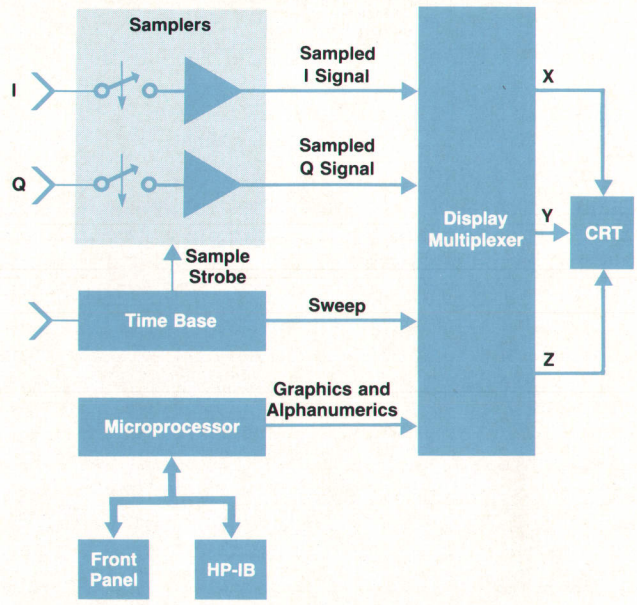


Fig. 5. *Block diagram of HP 3709A Constellation Display.*

voltage and S1 opens, a data valid signal becomes active, and the signal is displayed on screen. The next step resets the integrator to zero volts by closing S2. This happens between times C and D, and the sampler is then ready for the next sample.

In common with many high-frequency analog circuits, the sample-and-hold circuit suffers from drift of gain and offset. Rather than correct all of this in the circuit, a microprocessor-controlled autocalibration loop and a four-channel digital-to-analog converter (DAC) perform the correction. Gain drift is caused mainly by the sample pulse width varying with temperature and is corrected by varying the integration time. Offset drift is caused by diode forward voltage variations in the diode bridge sampling gate and changes in sample pulse shape. Offset correction is applied by varying the bias to the diode bridge. These corrections occur every three minutes unless autocalibration is disabled via the HP-IB.

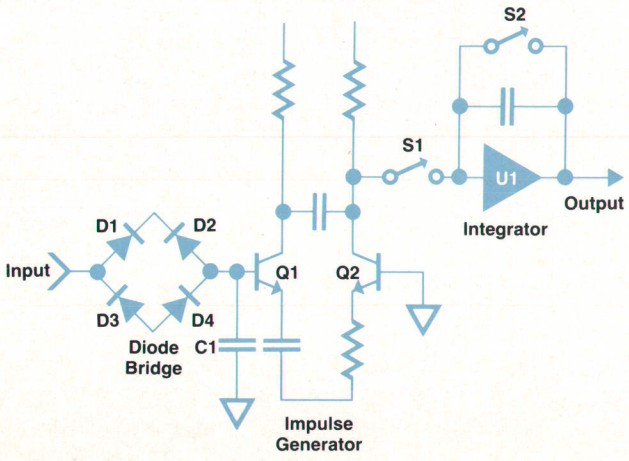


Fig. 6. *Sampler schematic.*

Time Base Modes

The time base operates in three modes: constellation, eye diagram, and calibration mode. The principal elements of the time base circuitry are shown in Fig. 8. A clock input edge is selected every 20 μs, delayed by a precise time, and output as the I and Q strobe to the samplers. In eye diagram mode an X-axis time sweep is also generated. The design goal was a CRT display with minimal time base jitter. Since the X axis is quantized to 200 increments over two symbols (two complete cycles), the time between samples is 125 ps at the maximum clock rate of 80 MHz. The jitter specification was set at 30 ps. In practice, the jitter is less (see box on page 11).

Eye Diagram. This mode is the most complex mode, and is similar to conventional sampling oscilloscope operation. There is no time base sweep control. The time base is adjusted automatically to make the display width equal to the width of two symbols for any clock in the range from 1 MHz to 80 MHz. Automatic width control is convenient for comparing eye diagrams. Since they are all displayed the same width, it is easier to pick out impairments. A two-symbol width allows one eye to be placed in the center of the screen, with a half symbol displayed on each side. Two ranges of automatic control are used: 1 MHz to 10 MHz and 8 MHz to 80 MHz. Autoranging handles the range selection. A voltage proportional to the clock input frequency is used to control the gain of the I-and-Q delay (and the I delay and Q delay) one-shot circuits. This voltage also selects either divide-by-2 or divide-by-16 operation via the autorange circuit.

The synchronizer uses two D flip-flops in cascade, both clocked by the divided input clock. The variable divider ensures that all clock inputs are at least 200 ns apart, which ensures that the first flip-flop has settled even if the data and clock change together. The second flip-flop then achieves jitter-free synchronization because its D input is stable long before the second clock edge occurs (see Fig. 9).

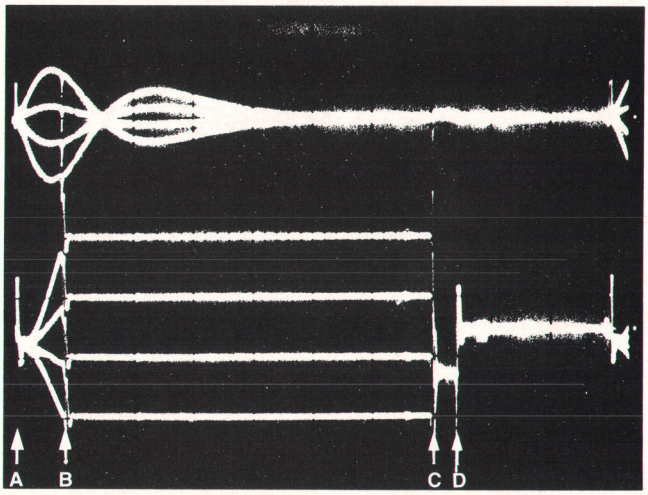


Fig. 7. *Sampler waveforms for a 4-level PRBS input signal. Upper trace is output of impulse generator and lower trace is output of integrator.*

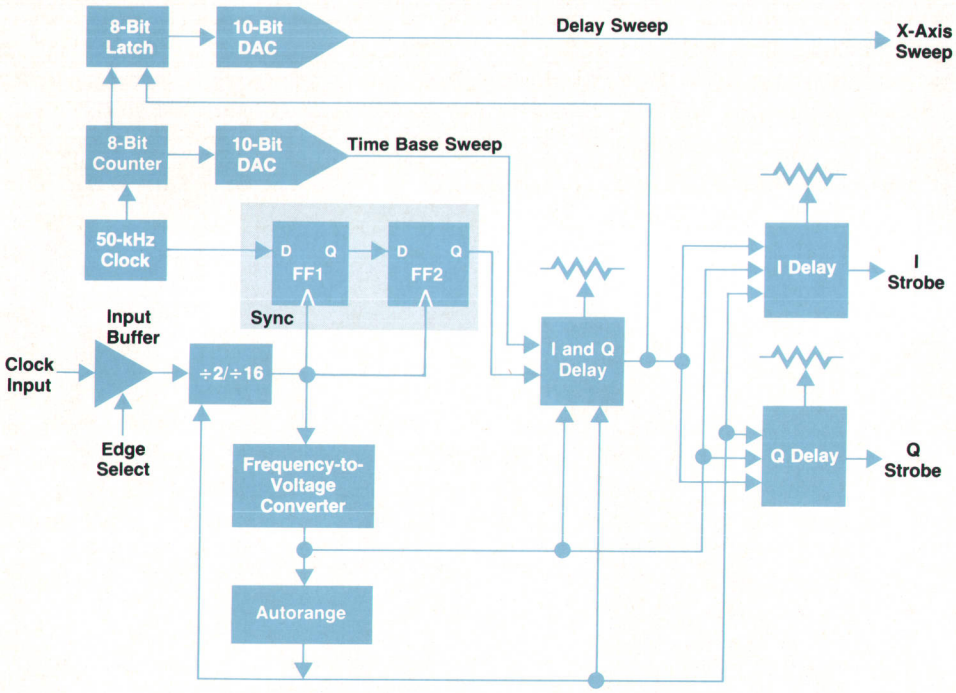


Fig. 8. *Time base block diagram.*

In Fig. 8, the I-and-Q delay allows the user to adjust the sampling instant of both strobes together over a range of one symbol. The I delay and Q delay allow each strobe to be delayed by up to one symbol period. The delay range is independent of the clock rate. The I-and-Q delay is swept by the time base sweep, which has 201 discrete levels. This allows the delay to be stepped progressively through two symbols in 1% steps. The I-and-Q delay function is performed by a monostable (one-shot) circuit designed to have very low timing jitter. This circuit is described later.

The time base sweep is generated by an 8-bit counter driving a 10-bit DAC with states 0 to 54 blanked. This allows 10-bit linearity, approximately 0.1%; the two least-significant bits are unused.

In eye diagram mode, a sweep is also required to drive the CRT display. A conventional sampling oscilloscope uses the time base sweep, which requires the sweep to be stable for the duration of the I-and-Q delay, the I (or Q) delay, the sample time, and the display time. The sample rate can be increased if two pipelined sweeps are generated. The first sweep only needs to be stable for the I-and-Q delay time, and the second sweep only needs to be stable while a point is displayed on screen. This allows one point to be displayed while the time base increments to the next point. The X-axis sweep is conveniently generated by latching the time base count and using a second 10-bit DAC.

Constellation. In constellation mode the 8-bit time base sweep counter is fixed at the center of the sweep. The display shows the I and Q signals on the X and Y axes. The sample times can still be manually adjusted by the three delay controls.

Calibration. In calibration mode, the microprocessor routes the 50-kHz clock directly to the I and Q strobes, so that sampler calibration can be performed even if no clock input is present.

Low-Jitter One-Shot Circuit

The sampling instant on the HP 3709A is varied with the I-and-Q-delay one-shot circuit (Fig. 10). A discrete circuit was designed because available integrated circuits did not have the required jitter performance.

The one-shot delay time is given by:

$$t = (C1+C2)(V_{Start} - V_{Stop} - iR)/i$$

For frequencies below 10 MHz, C1 and C2 are used; above 10 MHz, only C1 is used. V_{Start} is set by the user front-panel control. V_{Stop} is the sweep voltage in eye diagram mode, or a constant value in constellation mode. R represents the effect of R1 and R2, which are added to damp the resonant circuit formed by the timing capacitor and the printed circuit board trace inductance. For C1, a resonant frequency of about 100 MHz is observed. If undamped, the start-up transient would distort the ramp. The current i is supplied by Q3.

The circuit functions as follows. The voltage V_t at the collector of Q3 is clamped to V_{Start} initially. When the flip-flop is triggered, Q1 turns off and current supplied by

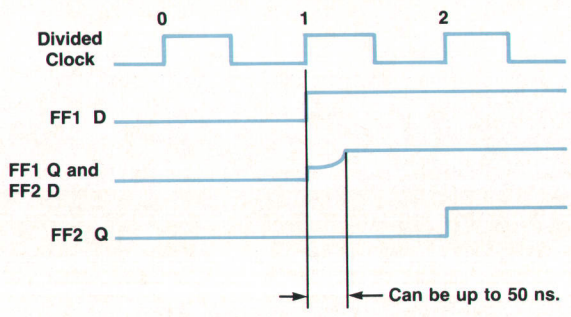


Fig. 9. *Time base synchronizer waveforms.*

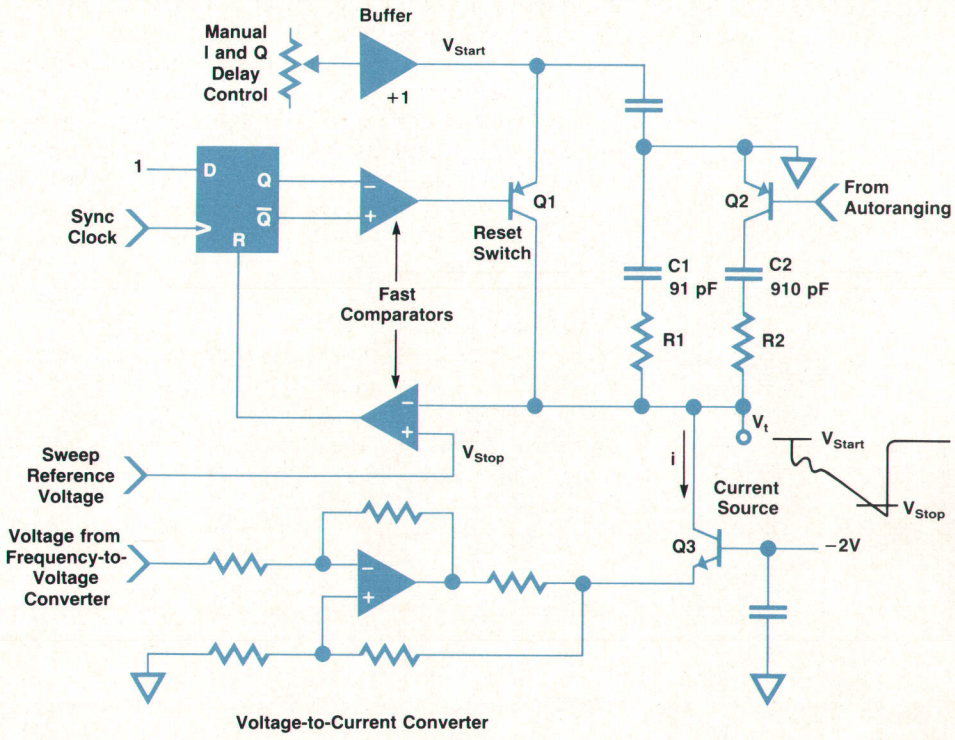


Fig. 10. *Low-jitter one-shot circuit.*

$Q3$ causes V_t to ramp down. When V_t is more negative than the sweep reference voltage, the flip-flop is reset and Q1 turns on.

The discharging current i is accurately controlled by the voltage-to-current converter operational amplifier. The amplifier is decoupled from the high-speed ramp by the cascode transistor Q3. This configuration allows an accurate current to be maintained despite the high discharge rate. The current source is controlled over a decade range. An additional decade range is provided by switching in the timing capacitor C2 using Q2.

The performance of such a circuit cannot be evaluated by observing the ramp directly at V_t. Any probe degrades the jitter performance, stray capacitance upsets calibration, and stray inductance causes ringing. Indirect means must be used. The best method is to use the time base to drive the sampler, and sample a sine wave. The zero crossing of a sine wave has a defined dV/dt which allows easy conversion from volts to picoseconds. For example, a 1V peak, 80-MHz sine wave has a dV/dt = 0.503 mV/ps at the zero crossing.

Using a 10-bit analog-to-digital converter after the sampler gives quantization steps of 2 mV for a ±1V input, allowing a time resolution of 2 ps. Linearity is measured by sampling a signal running at twice the clock frequency. Two symbols then contain four cycles or nine zero crossings. Linearity is measured by observing the displacement of the zero crossing. Using this principle, a reliable measurement of jitter and linearity can be achieved in a computer-based test system.

Fig. 11a shows the linearity and jitter performance of the time base one-shot circuit. Fig. 11b shows a residual jitter of approximately 9.5 ps. This value is derived as follows:

- 80 MHz = 12,500 ps/cycle

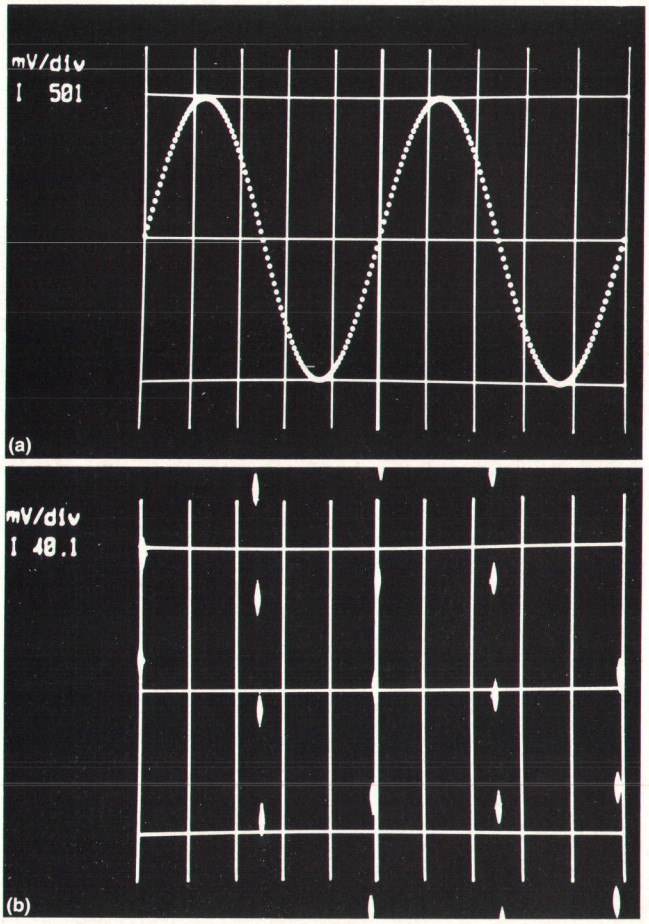


Fig. 11. *Jitter performance on sine wave. (a) 80 MHz, 1V p-p. (b) Above trace at increased sensitivity, jitter ≈9.5 ps.*

- 1% of cycle = 125 ps, which corresponds to a displacement of 16.5 mm
- Dot peak-to-peak displacement = 5 mm
- Dot rms displacement ≈5/4 = 1.25 mm
- Rms jitter ≈125 × 1.25/16.5 = 9.5 ps.

However, at lower clock input levels this value increases because of input buffer noise.

Analog Signal Processing

After being sampled, the signal is amplified to a suitable level for driving the display. Because the signal is now lower in frequency, this can be done with high-speed op amps. Perhaps the most interesting feature is the hardware multiplexing done to perform several tasks concurrently. The hardware is configured to one of four principal functions by the microprocessor. The various signal paths are (Fig. 12):

1. Display the incoming signal
2. Display the graticule and text from the microprocessor graphics generator
3. Measure the setting of the front-panel gain control, displayed on screen as mV/div
4. Measure and correct sampler gain and offset.

The first three functions are implemented with FET analog switches and appear concurrent to the user. The display continuously switches between incoming I and Q data at a 50-kHz rate, the graticule drawing is updated at a 40-Hz rate, and a dc calibration voltage is routed through the front-panel gain control twice per second to measure the setting and thus calculate the instrument sensitivity.

Sampler offset and gain correction normally occurs every three minutes. A three-level dc calibration signal is routed through the sample-and-hold circuit with the front-panel gain control bypassed, leaving only fixed gain stages. The offset is adjusted to zero volts and the gain is adjusted to the value held in ROM.

Resampling and Data Conversion. Because the output of the sample-and-hold circuit is only valid for 10 μs, it is resampled using a slower sample-and-hold circuit to give sufficient time for analog-to-digital (A-to-D) conversion. This conversion is performed by the microprocessor and the DAC using a successive approximation algorithm. The same DAC is used for both graticule generation and measurements, thus reducing errors between the signal on the screen referenced to the graticule and the signal measured by the processor.

Vector Graphics Generator

The need for a vector graphics generator was identified early in the design of the HP 3709A Constellation Display. To meet project design goals for low cost and high reliability, circuit complexity had to be minimized. Investigation showed that existing designs offered excellent display quality and plenty of features, but exceeded the target cost by an order of magnitude. Ruthless trimming of unnecessary display features resulted in an efficient design which has a low component count and is easy to manufacture.

The instrument display is an electrostatic CRT module with XYZ vector drive inputs. Graphics are produced by the vector graphic, or calligraphic, technique often used with this type of display. This technique builds a CRT display pattern by modulating the X and Y deflection to draw individual lines and characters. In contrast to a raster scan display, the time needed to refresh the display depends on the number and length of the individual lines (vectors). The technique is used here to generate full-screen graphics in a small fraction of the display time, so that more display time is available for analog data.

The design minimizes cost and board area by tight coupling between the graphics hardware and the main microprocessor. Two DACs are required. With the addition of precision comparators, these DACs are also used to perform

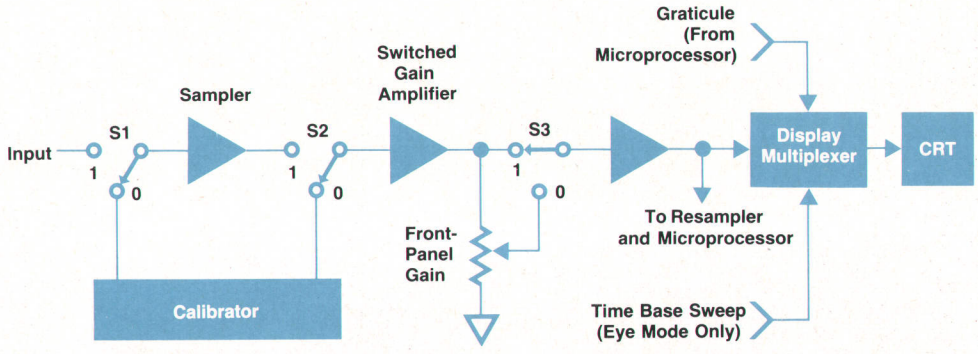


Fig. 12. *Analog signal processing. Four functions are performed: 1) input signal displayed on CRT (S1 = S2 = 1 and S3 = 0), 2) graticule is displayed on CRT, 3) front-panel gain potentiometer is measured (S1 = S2 = S3 = 0), and 4) sampler is calibrated (S1 = 0 and S2 = S3 = 1).*

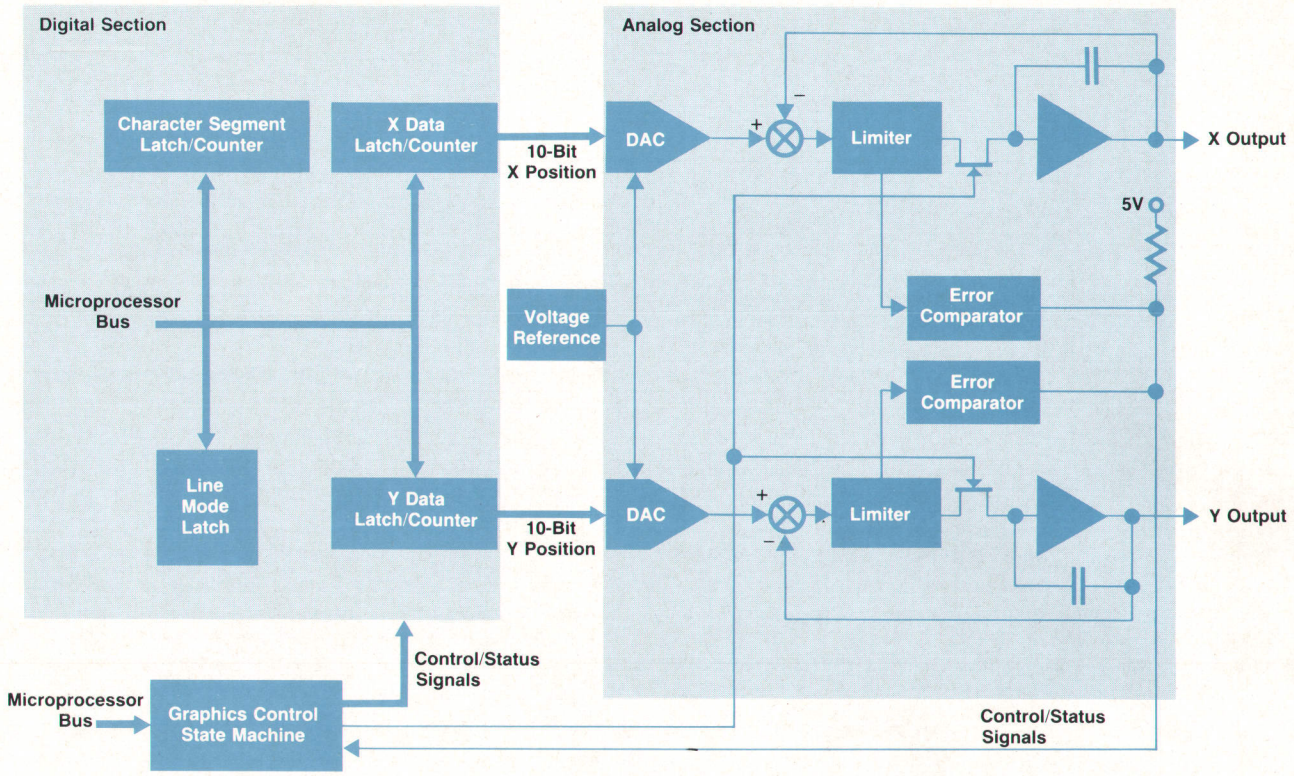


Fig. 13. *Graphics generator block diagram.*

analog-to-digital conversion for measurement of constellation samples. By reusing the microprocessor and DACs, the marginal cost of the graphics generator is reduced to only 160 cm^2 of printed circuit board area.

Display Refresh. The graphics display is continuously refreshed at a rate of 40 Hz. Although this rate is unusually low, it is sufficient to prevent display flicker with a P39 long-persistence CRT phosphor.

Each refresh cycle starts with a microprocessor interrupt from the real-time clock. This activates the firmware routine that drives the graphics generator. The display is stored internally as a list of primitive operations which represent horizontal lines, vertical lines, hidden moves, or ASCII characters. Line and move operations are sent directly to the graphics generator hardware while ASCII characters are interpreted by the firmware, using table lookup to generate a sequence of line segments for each character.

The display refresh cycle typically uses 5% to 15% of the available display time, and a similar fraction of microprocessor time. Execution speed of the firmware routine is important, so it is coded in assembly language. The inner loops for display list output and character interpretation contain only six microprocessor instructions. This is possible because simultaneous design helped select the best trade-off between hardware and firmware complexity.

Although described as a single operation, display refresh is divided into four phases to even out processor loading and minimize latency for other real-time processes. Two phases are allocated to parts of the graticule and the other two phases are allocated to display text.

Graphics Hardware. The graphics generator is divided into analog and digital sections, with a state machine to provide control signals. Fig. 13 shows the block diagram.

The analog section generates X and Y signals to drive the display. When drawing a line, these signals must ramp smoothly between the start and end points. If a line is at

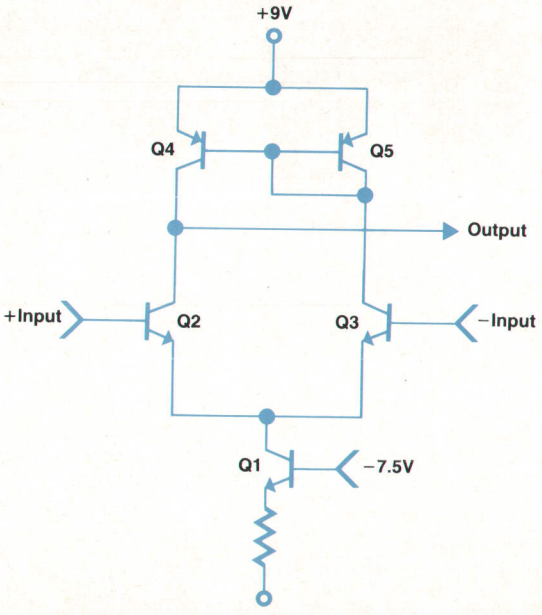


Fig. 14. *Differential limiter circuit.*

Automated Timing Jitter Testing

Automated testing allows measurement of parameters on every production instrument. In many cases there is virtually no manual method of performing the test in an acceptable time. A good example of this is timing jitter testing. A computer-driven automatic test is the only means of quantifying the amount of timing jitter in the HP 3709A Constellation Display.

The test system's clock input generator is set to the HP 3709A's specified minimum clock input level. This is the condition at which most timing jitter is likely to be seen. A sinusoidal signal is then fed into the I and Q channel inputs from the test system's signal input generator. When the HP 3709A is set to eye mode, two cycles of the signal can be seen. However, the test system is ignorant of the phase of the displayed waveform.

Because the I and Q position controls, which correspond to vertical position controls in eye mode, cannot be switched out, a measurement of the offset is required to be used as a reference for calculating the eye position of zero crossing points and peak points, etc. This is accomplished by switching the signal input generator off (i.e., to its minimum amplitude of approximately −90 dBm, which is approximately 50 dB below the HP 3709A noise floor) and measuring 1000 samples at Eye Position = 0.0000 Sample Periods.

From these 1000 samples, the mean is calculated to give a reference voltage V_{ref}. By adjusting the phase of the signal input generator using its minimum phase increment of 0.1 degree, the signal can be set up so that the zero crossing point occurs at Eye Position = 0.0000 Sample Periods. This is the point of maximum slew rate where the worst timing jitter will be observed. By measuring 1000 samples at this point, a distribution of voltage values will be obtained. Using the 1000 samples, the rms value of the voltage at the zero crossing point can be estimated. This rms voltage corresponds to noise at the zero crossing point and has to be converted into the time domain before the timing jitter can be calculated. To calculate the timing jitter from the noise at the zero crossing point, the peak value and frequency of the incoming signal must be known. The peak value is measured by changing the eye position to the peak position of the waveform and measuring the mean value in volts. From this value V_{ref} is subtracted to give V_{peak}. The frequency is known.

Using the following formula for the instantaneous voltage V_i of a sine wave, the rms noise can be converted to jitter in the time domain:

$$V_i = V_{peak} \times \sin \omega t$$

where ω = frequency in radians/s and $t = 1/\omega \times \sin^{-1}(V_i/V_{peak})$. Therefore:

$$\text{Timing jitter} = T_j = 1/\omega \times \sin^{-1}(V_{rms}/V_{peak}) \text{ seconds}$$

The results obtained during the development phase of the project and the results of the first production instruments were stored on disc. The analysis of the test results calculated the lowest and highest timing jitter values, the mean timing jitter, and the standard deviation at each frequency. This ensured that there were no hidden specification problems. Fig. 1 shows a typical distribution of timing jitter test results.

David Robertson
Production Engineer
Queensferry Telecommunications Division

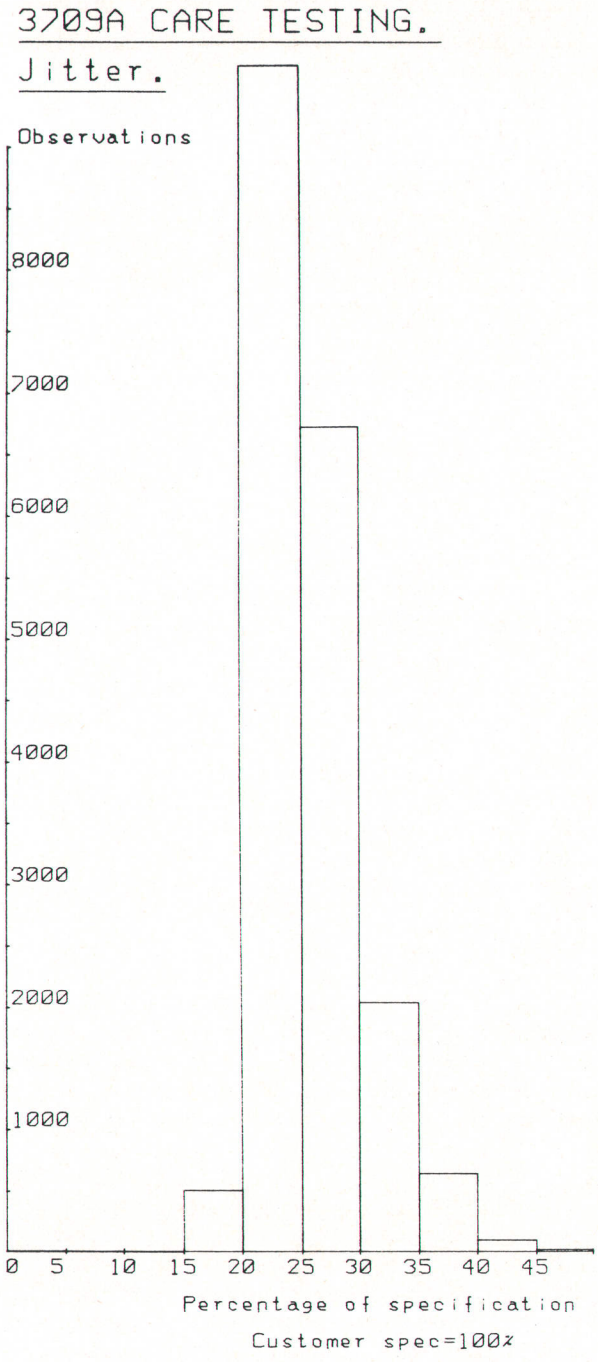


Fig. 1. *Timing jitter test results.*

an angle to the axes, the X and Y ramp rates must be proportional to the X and Y components of the line so that both signals reach the endpoint at the same time. In a general-purpose vector display the ramp generators are precision circuits since proportionality errors of only 1% are easily visible on a long line. Fortunately it was possible to limit graphics to horizontal lines, vertical lines, and short line segments at 45 degrees to the axes. This made it possible to use the simple ramp generator shown in the diagram.

The analog section operates in three states: idle, hold, and ramp. In the idle state the output of each channel tracks the input. The error signals are small, so the limiters act as simple amplifiers. Overall each channel behaves as a unity-gain buffer with single-pole frequency compensation. In the hold state the FET switches isolate the output integrators. This allows the inputs to be changed to a new graphics position while the outputs remain at the old position. In the ramp state there is a large error between the input and output of one or both channels. The limiter supplies a constant current to the output integrator that causes the output to ramp in the direction of decreasing error. As the error becomes small, the limiter moves into its linear region. Each channel has a pair of comparators which detect position errors that exceed the limiter threshold. For a visible line, the display spot is enabled from the start of the ramp state until the position error signal becomes false, indicating that both channels have returned to the idle state.

At the heart of the circuit is a differential limiter (Fig. 14). This venerable circuit is one of the simplest designs for an op amp input stage. Q1 supplies a constant current to the differential pair Q2 and Q3. Q3's collector feeds the current mirror formed by Q4 and Q5 and the output is added at Q2's collector to give an output current proportional to the differential input voltage. Input voltages of only 100 mV are sufficient to divert all current through one side of the differential pair, providing the limiting action.

The complete circuit for each channel can be likened to an operational amplifier; the integrator amplifier corresponds to the output stage while the integrator capacitor corresponds to the frequency compensation capacitance. The main function of the circuit, the constant rate output ramp, corresponds to one of the least desirable features of an operational amplifier—output slew rate limiting. In this circuit, slew rate limiting is realized with a precision that is not currently available in commercial integrated circuits.

The digital section latches the next graphics position for a line or move operation. For a line segment (ASCII character), it must generate the next position by adding relative segment offsets to the current position. These operations and the idle-hold-ramp-idle sequence for the analog section are controlled by the state machine. The control functions could be performed by the microprocessor, but performance would suffer. The state machine, implemented with a single 20-pin programmable logic device, is an extremely cost-effective solution.

Display Graticule

An unusual feature of the HP 3709A is the user-selectable graticule. Depending on the modulation scheme, a constellation display can have clusters arranged in two, three, four, seven, or eight parallel rows and columns. Instead of a fixed display grid, a different graticule is provided for each modulation scheme. These graticules are simpler than a single general-purpose graticule and provide an unambiguous reference position for constellation measurements.

Since the graticule is drawn on the CRT, display imperfections affect the measured constellation and the graticule equally. The operator can use the graticule to resolve small levels of impairment on screen, eliminating any error caused by the CRT. This is important since some constellation impairments are similar to common CRT imperfections. For example, traveling-wave-tube amplitude compression looks very much like CRT barrel distortion.

The graticule generator provides drive signals to the vector display module via a multiplexer, which selects between the sampled analog constellation signals and the graticule. In addition to drawing horizontal and vertical graticule lines, the graticule generator generates display text for the graticule calibration factor, measurement results, and error messages.

Measurement Verification

The measurements performed by the HP 3709A are complex and involve a combination of hardware and firmware. The three main stages are: sampling and displaying data (hardware), A-to-D conversion (hardware and firmware), and statistics accumulation and analysis (firmware).

The hardware system of the HP 3709A can be checked by applying input signals and measuring accuracy, flatness, noise, et cetera over the HP-IB. However, the dedicated measurements of closure, lock, and quad angle cannot easily be verified in this way. To allow firmware verification, the HP 3709A can accept data over the HP-IB that simulates sampled data from a constellation. A verification program was written on an HP 9000 Series 200 Computer to generate constellations with a variety of impairments for all modulation schemes covered by the HP 3709A. This program checks that the statistics accumulation agrees exactly and the analyses (closure, lock, and quad angles) agree within acceptable limits.

HP-IB Firmware Verification

A Series 200 BASIC program was written to exercise all the HP-IB commands separately and in sequence. The test program was written around the HP 3709A HP-IB External Reference Specification. This document defines all aspects of the HP-IB behavior of the instrument and is used as a basis for customer documentation. The program is written as a number of modules, each designed to exercise one HP-IB function as thoroughly as possible. Commands with a finite set of parameters are tested for each permissible parameter, while those with infinitely variable parameters are tested at key values (e.g., zero, limits, and just beyond limits) to test error detection and recovery. The modules are executed in a fixed sequence.

The long-term benefit of this approach to interface testing is having a test program to run on any future revisions of HP 3709A firmware.

Product Design

During the design of the HP 3709A, ease of manufacture was a prime goal. Some of the points considered were:

1. Keep the number of printed circuit boards to a minimum. The HP 3709A is made up of only seven printed circuit boards.
2. Where possible, choose components that can be inserted in the printed circuit boards by machine to minimize hand loading. 50% of the components in the instrument are inserted automatically.
3. Fewer printed circuit boards means that fewer cables are required to interconnect them. There are 13 cables in the HP 3709A: five coaxial, five ribbon, and three simple wire looms. By mounting the processor board against the rear panel we were able to mount the the HP-IB socket and address switch directly on the processor board. The electrical cable from the line power switch was eliminated by putting the switch on the line input board at the rear of the instrument and operating it via a flexible mechanical cable just like a bicycle brake cable. This is purchased as part of the line switch assembly. The advantages of this mechanical cable are that the hazardous line voltages are kept in one small area, and the 50/60-Hz line is not carried through the cabinet with its possible screening problems. This type of cable linkage is less sensitive to mechanical variances than a rigid link would be.
4. The preset adjustments and test pins should all be accessible with minimum effort. This was achieved without too much trouble. The only difficulty was providing easy access to the HP 1340A Display Module's X/Y gain, position, and alignment controls. By mounting them along the top edge of the keyboard, we made them accessible through the spare mounting holes in the top of the front frame casting.

Acknowledgments

Boyd Williamson did the product definitions for the HP 3709A and was project manager through the early design phase. Peter Roubaud did the operating system and HP-IB firmware. Ross MacIsaac was responsible for the analog gain switching and resampler. Arthur Thornton did the product design and David Robertson was responsible for test software.

References

1. H. Walker, "Modulation Schemes and Digital Radio Growth," *Microwaves & RF*, Vol. 26, no. 2, February 1987, p. 75.
2. H. Walker, "Gauging Errors Set Digital Radio Quality," *Microwaves & RF*, Vol. 26, no. 4, April 1987, p. 89.
3. *A Review of Digital Radio Principles and Measurements*, Hewlett-Packard Publication No. 5954-7941 (contains parts of references 1 and 2).
4. K. Feher, *Digital Communications: Microwave Applications*, ISBN 0-13-214080-2.

Constellation Measurement: A Tool for Evaluating Digital Radio

by Murdo J. McKissock

THE CONSTELLATION DISPLAY is an invaluable tool for alignment and fault diagnosis of digital radios, and an important indicator of the radio's performance margin. The HP 3709A Constellation Display is the first commercial instrument that provides the capability to make quantitative measurements of a constellation.

Measurement data is provided at three different levels: raw samples, statistical accumulations, and analysis results. The raw samples represent individual constellation points and typically might be used to reproduce a constellation on a plotter, or to measure nonconstellation signals. The statistical accumulations provide information on the position, size, and orientation of each display cluster. This forms the basic data for analysis. The analysis results evaluate some common constellation impairments: relative rms cluster size, angle of rotation, and angle of quadrature. Using an external HP-IB (IEEE 488/IEC 625) controller it is possible to use the statistical accumulations to perform

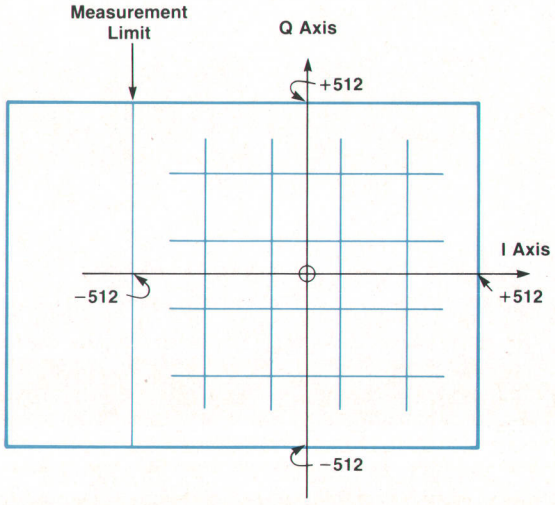


Fig. 1. *Constellation measurement scale.*

further analysis to measure other constellation impairments such as amplitude compression, amplitude-to-phase conversion, and phase noise.

Raw Constellation Samples

The real-time display is generated from input samples taken at regular intervals. These analog samples drive the display directly. A small proportion of the samples are converted to digital form during a constellation measurement. Each sample has two 10-bit digital values, one each for the in-phase (I) and quadrature (Q) modulation components. Sample values are returned as pairs of integers using the measurement scale illustrated in Fig. 1. A typical measurement might take 1000 digitized samples and plot them to produce a hard copy of the constellation (Fig. 2).

Statistical Accumulations

Instead of measuring and outputting raw samples, the HP 3709A can process samples internally. For each cluster in the constellation, the instrument accumulates six values:

Number of samples in the cluster: n_{ij}

Sum of the I values: $\sum_{k=1}^{n_{ij}} x_{ijk}$

Sum of the Q values: $\sum_{k=1}^{n_{ij}} y_{ijk}$

Sum of the squares of the I values: $\sum_{k=1}^{n_{ij}} x_{ijk}^2$

Sum of the squares of the Q values: $\sum_{k=1}^{n_{ij}} y_{ijk}^2$

Sum of the products of the I and Q values: $\sum_{k=1}^{n_{ij}} x_{ijk}y_{ijk}$

where (x_{ijk}, y_{ijk}) is the kth sample in the cluster with I and Q indices i and j.

This is similar to the statistics accumulation occurring in many pocket calculators, but there can be up to 64 sets of 6 registers each, one for each cluster in the modulation scheme.

From the register contents, it is easy to compute the mean position, rms size, and correlation coefficient between the I and Q values for each cluster. Fig. 3 shows a plot from a computer program which uses this information to generate ellipses representing Gaussian probability contours.

The individual samples are assigned to a particular "sample bucket" or set of registers using slicing boundaries midway between the constellation graticule lines (Fig. 4). Obviously, the position and overall size of the constellation must be adjusted so there is just one cluster in each of the sample buckets.

When the accumulation is complete, the contents of the registers can be output to an external controller or analyzed by the HP 3709A to obtain measures of constellation impairments.

Analysis Results

The HP 3709A computes four analysis results:

- I and Q constellation closure measures the relative rms cluster size in each direction. Constellation closure = [rms cluster size]/[0.5(cluster separation)] × 100% (see Fig. 5).
- Lock error measures the angle of rotation between the graticule and the cluster lines. This is related to receiver carrier phase lock error in a digital radio. In Fig. 6, lock error = $(\theta_1 + \theta_2)/2$.
- Quad error measures the quadrature error between the cluster lines. Quad error = $\theta_2 - \theta_1$ (see Fig. 6).

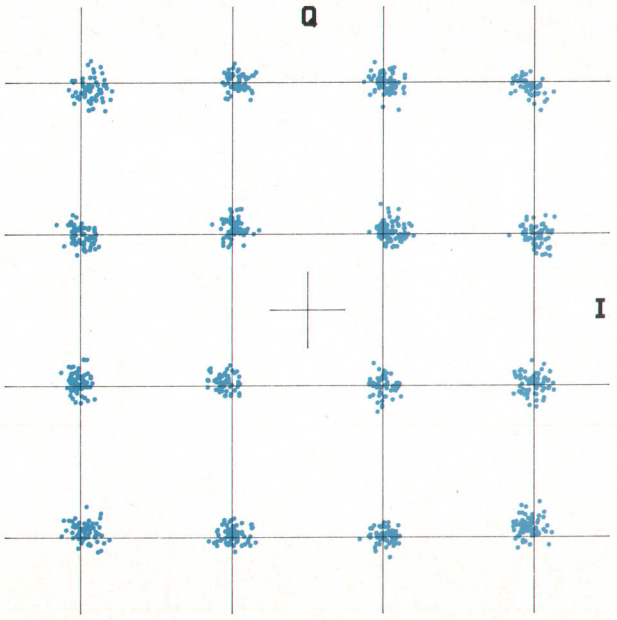


Fig. 2. *Typical constellation plot (1000 samples).*

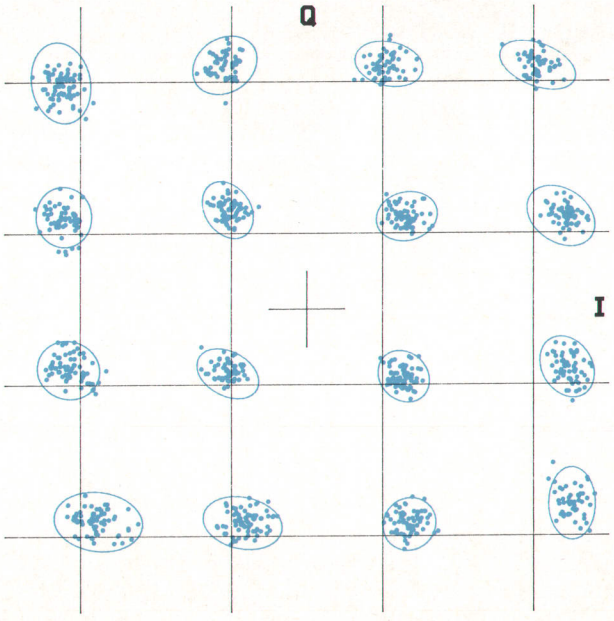


Fig. 3. *Constellation cluster ellipses.*

The results are determined using two separate analysis functions:

- The rms cluster size is estimated, computed as an average over all clusters in the constellation.
- The position, spacing, and slant of the cluster lines are estimated using a least mean squared error (LMSE) estimator to compute the parameters of a suitable model.

The rms cluster size is obtained by assuming that the distribution of points in each cluster is the same. The usual equation for standard deviation is modified to take into account the different mean positions of the individual clusters in the constellation. This gives the equations:

$$s_x^2 = \frac{1}{(N-M^2)} \sum_{i=1}^{M} \sum_{j=1}^{M} \left[\sum_{k=1}^{n_{ij}} x_{ijk}^2 - \frac{1}{n_{ij}} \left(\sum_{k=1}^{n_{ij}} x_{ijk} \right)^2 \right]$$

$$s_y^2 = \frac{1}{(N-M^2)} \sum_{i=1}^{M} \sum_{j=1}^{M} \left[\sum_{k=1}^{n_{ij}} y_{ijk}^2 - \frac{1}{n_{ij}} \left(\sum_{k=1}^{n_{ij}} y_{ijk} \right)^2 \right]$$

where M is the number of levels in the modulation scheme. Hence, M^2 is the number of clusters. N is the total number of samples. That is:

$$N = \sum_{i=1}^{M} \sum_{j=1}^{M} n_{ij}$$

The factor $(N - M^2)$, sometimes called the number of degrees of freedom, is used instead of N so that the estimate of rms cluster size is unbiased. It represents the total number of samples less the number of cluster mean position values used in the computation. The equations for s_x and s_y are designed to give equal weight to all samples to minimize the unavoidable errors caused by random variations in the distribution of samples.

The rms constellation closure for each axis is computed by dividing the rms cluster size s_x or s_y by one-half the cluster spacing p_{xx} or p_{yy} obtained from the LMSE estimator below:

$$\text{I closure} = 2\,(s_x/p_{xx}) \qquad \text{Q closure} = 2\,(s_y/p_{yy})$$

The term eye closure is often used to express the reduction in the opening of an eye diagram. There is a difference between eye and constellation closure (see Figs. 5 and 7). Constellation closure measures only the size of individual clusters, while eye closure also includes the effect of overlapping clusters in the eye diagram. A feature of the constellation display is that it is possible to resolve separately impairments that cause clusters to overlap in the eye diagram such as lock and quad errors.

The position, spacing, and slant of the cluster lines are estimated using a modeling technique. It is possible to estimate, for example, the spacing from the mean positions of a few clusters. However, this ignores most of the available data so that random errors (measurement variance) in the result will be much larger than necessary. Even the average of all cluster spacings effectively uses only the outer clusters.

Instead, a model constellation is defined. All clusters of the model lie on equally spaced parallel lines. The parameters of the model are the I and Q offsets, I and Q spacings, and I and Q slants. The parameters are computed such that the mean-squared error between the model and the measured constellation samples is minimized. Fig. 8 shows a constellation with mainly linear impairments. Not only is the constellation rotated and out of square, it is slightly offset from the graticule. The best-fit model is shown by the superimposed lines.

The model defines a linear relationship between the I and Q cluster indices and the cluster positions. As a result, the parameters that minimize mean squared error are easily computed from the constellation statistics. The model position of cluster i,j is given by:

$$\hat{x}_{ij} = \left(i - \frac{M+1}{2} \right) p_{xx} + \left(j - \frac{M+1}{2} \right) p_{yx} + p_x$$

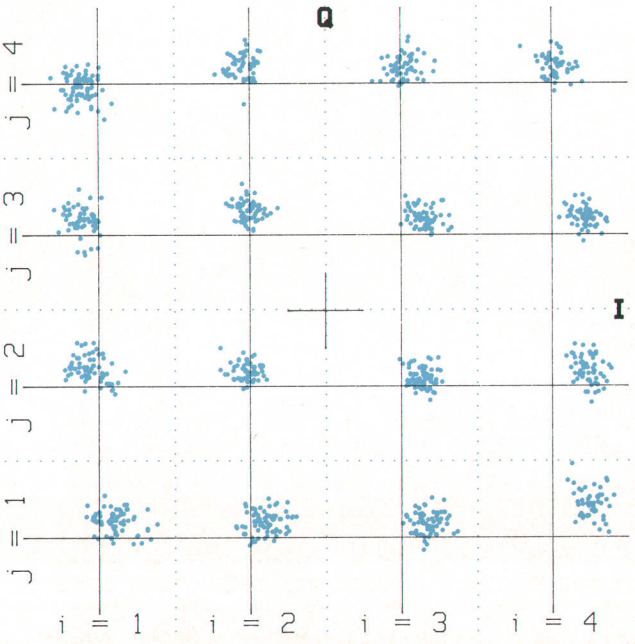


Fig. 4. *Constellation slicing boundaries.*

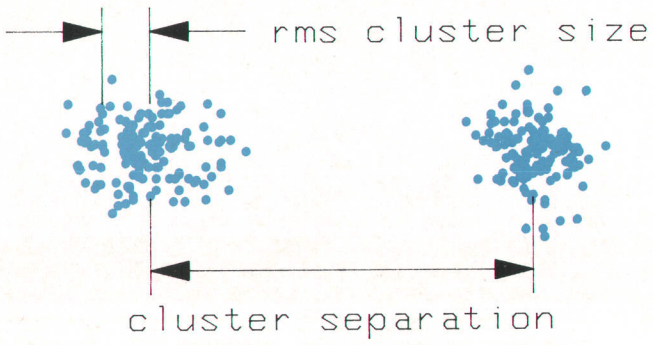


Fig. 5. *Constellation closure parameters.*

$$\hat{y}_{ij} = \left(i - \frac{M+1}{2}\right) p_{xy} + \left(j - \frac{M+1}{2}\right) p_{yy} + p_y$$

The parameters are represented as vectors:

$$\mathbf{P}_x = \begin{bmatrix} p_{xx} \\ p_{yx} \\ p_x \end{bmatrix} \qquad \mathbf{P}_y = \begin{bmatrix} p_{xy} \\ p_{yy} \\ p_y \end{bmatrix}$$

The values are computed by solving matrix equations:

$$\mathbf{AP}_x = \mathbf{B}_x \qquad \mathbf{AP}_y = \mathbf{B}_y$$

where

$$\mathbf{A} = \sum_{i=1}^{M} \sum_{j=1}^{M} \sum_{k=1}^{n_{ij}} \begin{bmatrix} (i-d)^2 & (i-d)(j-d) & (i-d) \\ (i-d)(j-d) & (j-d)^2 & (j-d) \\ (i-d) & (j-d) & 1 \end{bmatrix}$$

$$\mathbf{B}_x = \sum_{i=1}^{M} \sum_{j=1}^{M} \sum_{k=1}^{n_{ij}} \begin{bmatrix} (i-d)x_{ijk} \\ (j-d)x_{ijk} \\ x_{ijk} \end{bmatrix}$$

$$\mathbf{B}_y = \sum_{i=1}^{M} \sum_{j=1}^{M} \sum_{k=1}^{n_{ij}} \begin{bmatrix} (i-d)y_{ijk} \\ (j-d)y_{ijk} \\ y_{ijk} \end{bmatrix}$$

$$d = (M+1)/2$$

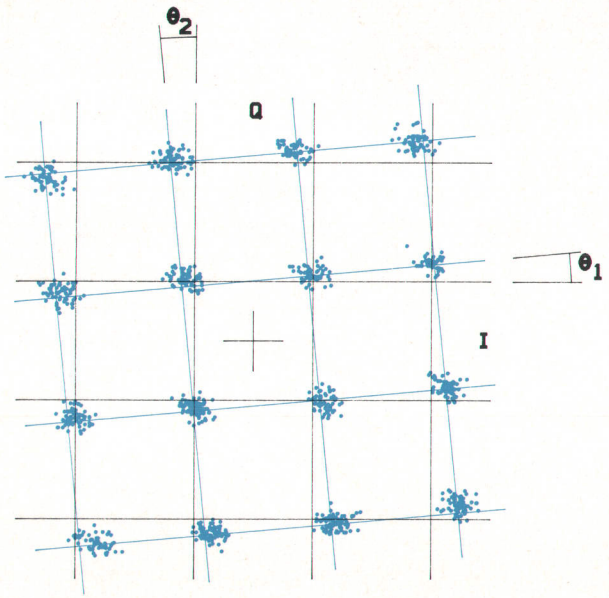


Fig. 6. *Lock and quad error parameters.*

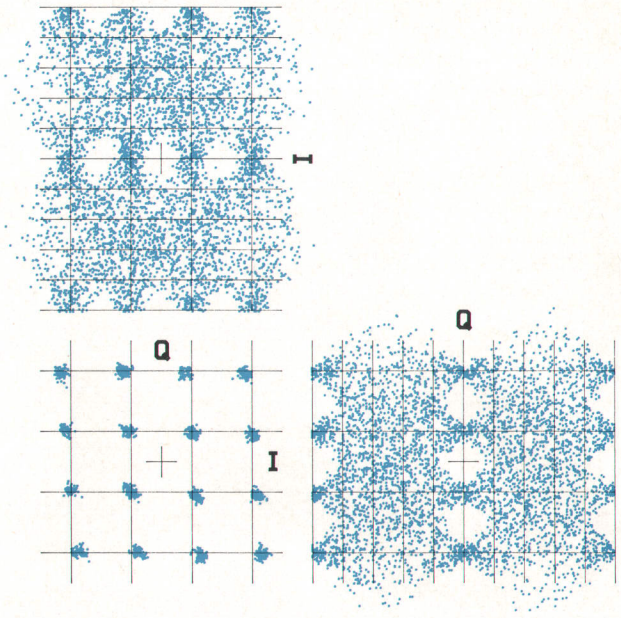


Fig. 7. *Constellation and eye diagrams.*

Lock and quad errors are computed from the model parameters:

$$\text{Lock error} = \tfrac{1}{2}[\tan^{-1}(p_{xy}/p_{yy}) - \tan^{-1}(p_{yx}/p_{xx})]$$

$$\text{Quad error} = -\tan^{-1}(p_{xy}/p_{yy}) - \tan^{-1}(p_{yx}/p_{xx})$$

The model gives results that make good use of a limited number of constellation samples. In addition, it neatly solves the question "What happens if the clusters do not lie on equally spaced parallel lines?" The model supplies a solution that will approximate the true constellation. It cannot be an exact fit if the constellation does not fit the linear model. However, the results are at least consistent, and

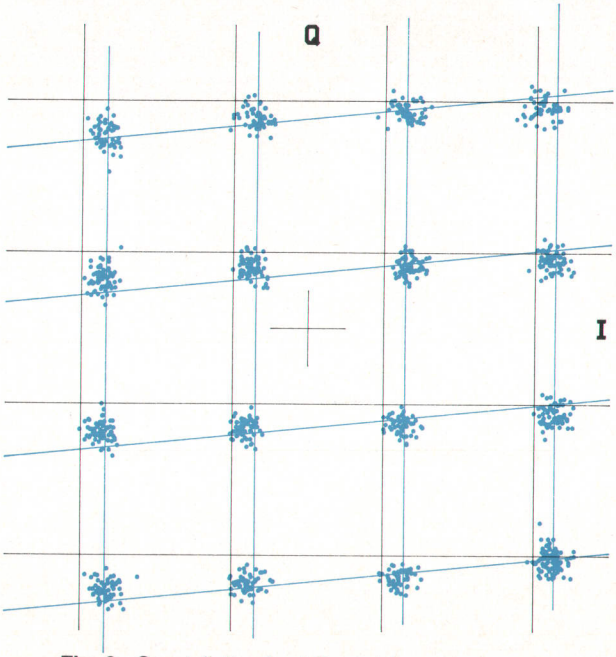


Fig. 8. *Constellation best-fit model.*

have low measurement variance. To determine the form and extent of nonlinear impairments, it is necessary to perform additional analysis in an external controller.

Notice in Fig. 8 that two of the corner clusters are slightly compressed towards the center of the constellation. The model gives more weight to the other fourteen clusters, so the lines do not pass through the centers of these corner clusters.

Stand-Alone Operation

All constellation measurement functions can be performed under HP-IB control. An external HP-IB controller can be programmed to collect constellation data for remote monitoring applications or to allow more extensive analysis.

During stand-alone operation, access to the HP 3709A's measurement functions is provided by the **MEASURE** key on the front panel. When this key is pressed, the instrument accumulates statistics and displays the analysis results. This allows the operator to resolve small changes in the constellation which are often difficult to detect by eye. If an HP ThinkJet Printer is attached to the instrument, pressing the **PRINT** key will produce a report (Fig. 9) containing a copy of the constellation plus the analysis results. This can be filed to provide a permanent record, allowing a carrier organization to monitor long-term changes in the performance of its radio links.

Acknowledgments

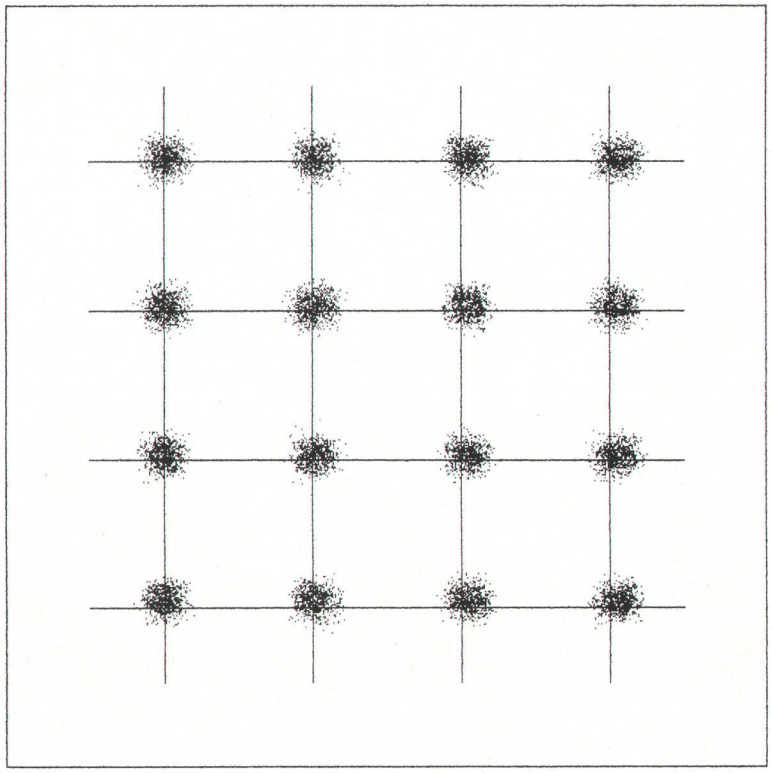
Peter Roubaud developed the firmware for the HP 3709A HP-IB interface, including the PRINT function.

HP3709A Constellation Display

RADIO

LOCATION

OPERATOR DATE



Modulation	16QAM
Scaling, I axis	220 mV/div
Scaling, Q axis	233 mV/div
I/Q Delay	ON
Closure, I	14.4 %
Closure, Q	13.8 %
Lock Angle Error	0.0 °
Quad Angle Error	0.1 °

COMMENTS

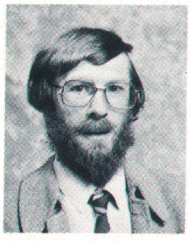
Fig. 9. *HP 3709A constellation report printed on a Thinkjet Printer.*

Authors

July 1987

4 Constellation Display

John R. Pottinger

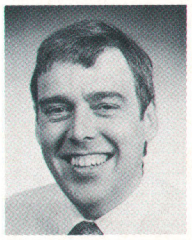


John Pottinger holds a 1970 BSc degree in electronics from North Staffs Polytechnic Institute and a 1985 MSc degree from Heriot-Watt University. With HP since 1978, he contributed to the development of the HP 3724A, HP 3725A, and HP 3726A Baseband Analyzers before working on analog and digital radio measurements and constellation analysis. He did the time base circuitry for the HP 3709A Constellation Display and is named coinventor on a patent application related to constellation analysis. Born in Reading, England, John now lives in Dunfermline, Scotland. He's married and has two children. His outside interests include gardening and mountain climbing, especially in challenging winter conditions.

Murdo J. McKissock

Author's biography appears elsewhere in this section.

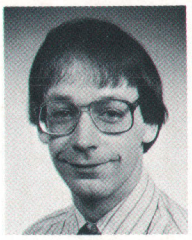
David J. Haworth



A project manager at the Queensferry Telecommunications Division, David Haworth has been with HP since 1972. He was responsible for the development of the HP 3709A Constellation Display, the HP 3717A 70-MHz Modulator/Demodulator, and the HP 3756A 90-MHz Switch. He earned a BSc degree in electronics from Salford University in 1964 and is a specialist in high-frequency analog design, amplifiers, and oscillators. David is married and has two children. He likes photography and shares with Murdo McKissock an interest in Munro bagging.

13 Constellation Measurement

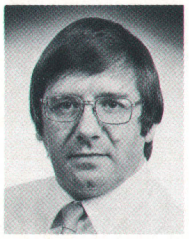
Murdo J. McKissock



With HP since 1981, Murdo McKissock worked on microprocessor and graphics hardware, constellation analysis, and instrument control firmware for the HP 3709A Constellation Display. He is named inventor for one patent application and coinventor for a second application. Both are related to constellation measurement. Murdo is a graduate of the University of Manchester, Institute of Science and Technology (BSc electronics 1981). A resident of South Queensferry, Scotland, he enjoys bicycling, archery, cross-country skiing, and go. Another pastime is Munro bagging. (This means that he climbs Scottish mountains over 3,000 feet. Sir Hugh Munro published a table of such peaks in 1891.)

19 Digital Radio Test Set

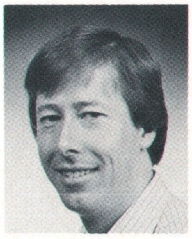
Geoffrey Waters



With HP's Queensferry Telecommunications Division since 1980, Geoff Waters is the R&D section manager responsible for developing instruments for testing broadband transmission systems. He was project manager for the HP 3708A Noise and Interference Test Set. Before coming to HP he led an engineering group at Marconi Communication Systems, Ltd. that developed equipment for microwave radio links and satellite earth stations. Born in Sunderland, England, he earned a BSc degree in electrical engineering from the University of Newcastle upon Tyne in 1966. He has written several papers on diverse topics and is interested in the evolution of broadband fiber-optic-based telecommunication systems. Geoff and his wife and three children are residents of Edinburgh, Scotland. His favorite leisure activity is field archaeology, especially discovering unrecorded prehistoric sites. He also sings in a choral society and is learning to play traditional music on the piano accordion.

26 Analog Power Meter

Anthony Lymer



A 1975 graduate of the University College of North Wales, Tony Lymer holds a BSc degree in electrical and electronic engineering. He was a researcher at the University of Bath before coming to HP in 1982. He developed the rms-to-dc converter for the HP 3708A Test Set and more recently has worked on gate array design. He's coauthor of five articles on mobile radio modulation techniques and phase-locked loops and is a member of the Institution of Electronic and Radio Engineers. Born in Chelmsford, England, Tony is now a resident of Edinburgh, Scotland. Cross-country skiing and hiking head his list of leisure activities.

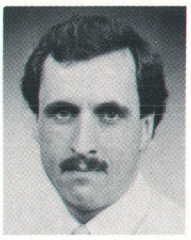
30 Noise Generator and Reference

Dayananda K. Rasaratnam

Daya Rasaratnam was born in Colombo, Sri Lanka and studied violin at the Royal College of Music, London (ARCM diploma 1975) before continuing his education in electrical and electronic engineering. He received a BSc degree from the University of Birmingham in 1978 and joined HP the same year. An R&D engineer, he has contributed to the development of the HP 3724A Baseband Analyzer and the HP 3708A Test Set. At the same time, he was working toward an MSc degree in digital techniques from Heriot-Watt University and completed work for his degree in 1984. A resident of South Queensferry, Daya is married and has a young daughter. Music is an important outside interest. He participates in several orchestral concerts each year and plays duets with his wife for church meetings.

36 Automated Radio Testing

John A. Duff



With HP since 1983, John Duff contributed to the development of the HP 3708S Measurement System and is currently working on a system for monitoring data lines. His professional specialty is workstation-based instrument control systems. He was born in Earley, Berkshire, England and educated at the University of Southampton (BSc electronic engineering 1983). He now lives in Edinburgh, Scotland, is active in scouting, and is studying for an MBA degree. John likes all sports, especially white water canoeing, swimming, golf, and squash.

A Digital Radio Noise and Interference Test Set

This instrument facilitates the measurement of the bit error ratio (BER) for a digital communication system under simulated path fade conditions. A desired C/N or C/I ratio can be established and maintained in the presence of received radio signal variations.

by Geoffrey Waters

SINCE THE LATE 1970s, an increasing proportion of long-haul telecommunications link equipment has used digital modulation techniques and this trend is expected to continue. Because of the nature of the error-generating mechanism in digital transmission, the accurate evaluation of a digital radio in terms of BER (bit error rate) versus C/N (carrier-to-noise) ratio requires a higher degree of measurement accuracy and repeatability than is required to evaluate an analog radio. Furthermore, the crest factor of the noise causing the errors assumes a more vital role. These factors initiated the development of the HP 3708A Noise and Interference Test Set (Fig. 1).

Establishing a C/N or C/N_o Ratio

The BER is usually measured over the range of C/N ratios encountered during hostile propagation conditions. The required C/N ratio is established either by varying the received signal level (RSL) by means of an attenuator (varying C) or by injecting additive noise into the receiver IF (varying N). Frequently in the laboratory, factory, or field, a variable RF attenuator is inserted into the microwave receiver input waveguide to attenuate the RSL. The thermal noise from the receiver's front end then defines the C/N_o (carrier-to-noise-density) ratio according to:

$$C/N_o = RSL + 174 - F \text{ at } 17°C$$

where F is the noise figure of the receiver in dB and 174 dBm/Hz is the thermal noise floor at 17°C.

For example, assume the receiver noise figure is 6 dB and RSL is −70 dBm for a 10^{-6} BER, then $C/N_o = 98$ dB-Hz. This ratio remains unchanged throughout the receiver RF, IF, and predetection circuits because signal and noise are amplified equally. The typical unfaded C/N_o ratio would be about 40 dB higher, or 138 dB-Hz, and the BER would revert to a typical residual value of much less than 10^{-10}. A 40-dB attenuator can be used to vary the C/N_o ratio from its unfaded value, allowing a BER curve to be plotted as a function of C/N_o ratio down to the receiver's threshold. Additional information on establishing a C/N or C/N_o ratio is given in reference 1.

Unlike C/N_o, the C/N ratio in the receiver varies at points throughout the RF/IF chain and depends on the appropriate noise bandwidth. That is:

$$C/N = C/N_o - 10 \log B_e$$

where B_e is the noise bandwidth at the point of interest. In terms of RSL:

$$C/N = RSL + 174 - F - 10 \log B_e$$

Using this equation, the C/N ratio can be related to the

(continued on page 21)

Fig. 1. *HP 3708A Noise and Interference Test Set for evaluating long-haul digital telecommunications systems.*

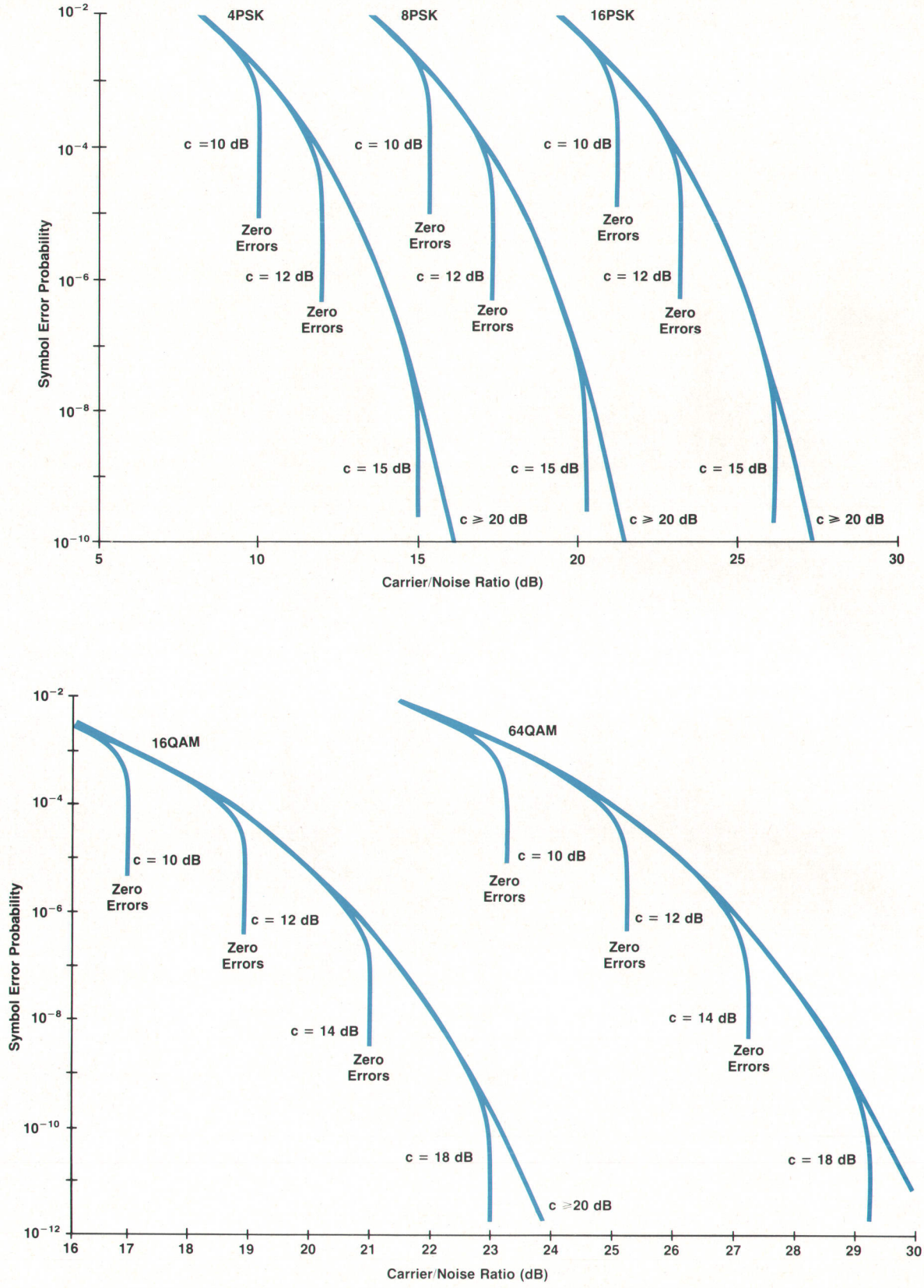


Fig. 2. *Probability of symbol error versus C/N ratio for finite noise crest factor c for N-phase PSK (phase shift keying) data transmission and (b) QAM (quadrature amplitude modulation) data transmission.*

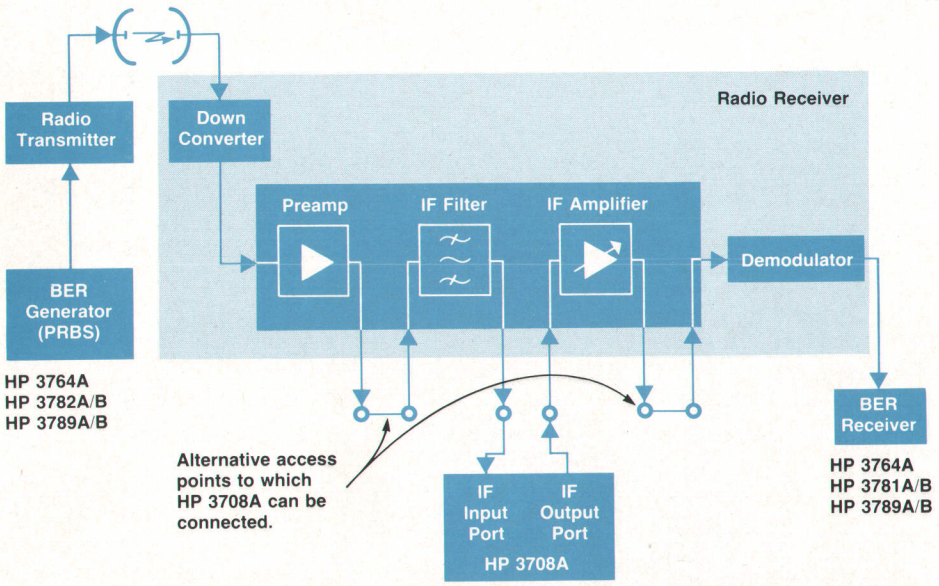


Fig. 3. *Typical test configuration using HP 3708A Test Set.*

RSL for the purposes of flat fade simulation. This method relies on knowing the noise bandwidth and noise figure for every radio under test. The sensitivity of the method to these values is unacceptably high, since BER can change by more than one order of magnitude for a C/N change of less than 0.5 dB.

The traditional method of fade simulation uses a power meter to check the effective C/N ratio in the receiver's IF strip or to measure the RSL at the RF stage. In the latter case, the levels are low and the nominal RSL is measured. The attenuator accuracy is relied on to set the desired RSL, assuming that the incoming signal level does not vary.

The RF attenuator method is time-consuming and inconvenient. In field tests, variations in RSL make it difficult or impossible to fade the RF signal as desired and make accurate BER measurements, particularly when working near receiver thresholds where a small scintillation fade can cause loss of synchronization.

Sometimes the inaccessibility of the waveguide attenuator makes the measurement slow, and it is difficult to automate. Matching problems and inherent attenuator inaccuracy at microwave frequencies reduce the reliability and repeatability of the measurements and increase the probability of operator error. There are too many uncontrolled variables for repeatable measurements.

Another method, the additive noise method, cannot check the overall fade margin but gives an accurate analysis of the C/N penalties caused by individual impairments in the radio. It is difficult and sometimes impossible to obtain this using the traditional method. The additive noise method establishes a C/N, C/N_o, or E_b/N_o (energy/bit-to-noise-density) ratio by injecting relatively high-level noise into the receiver's demodulator or IF at normal RSL. The wideband noise spectral density of a noise generator is filtered to the desired bandwidth and supplied via an attenuator and amplifier combination to a network where it is combined with the IF carrier. The C/N ratio is established in the known noise bandwidth of the filter.

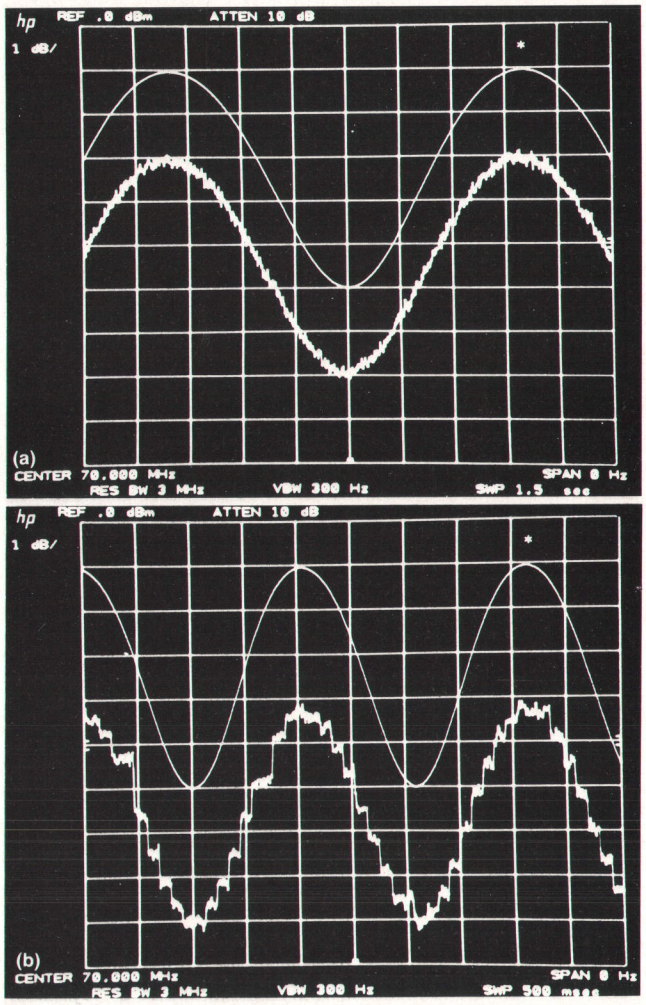


Fig. 4. *Injected noise level versus variation in IF signal power. (a) Variation = 10 dB/s. (b) Variation = 50 dB/s. The top waveform in each plot is the sinusoidally varying carrier level and the bottom waveform is the averaged noise level.*

Noise Crest Factor Enhancement

Crest factor is, by definition, the ratio of peak value to rms value. The noise crest factor at the noise output or the IF output of the HP 3708A is defined as the ratio of the hard-limiting voltage level to the rms value of the noise voltage. It has been shown[1] that the crest factor of noise used for determining bit error rate (BER) versus carrier-to-noise (C/N) ratio curves can significantly affect the accuracy of these curves for low BERs. Although a crest factor greater than 15 dB is sufficient to achieve good accuracy at BERs down to 10^{-6}, it may sometimes be necessary to observe digital radio operation at significantly lower BERs.

The HP 3708A control algorithm in C/N mode makes it possible to have several different combinations of fine attenuator and step attenuator settings with a given carrier level and C/N ratio. This property can be exploited to enhance the noise crest factor at the IF output by exchanging attenuation between the fine attenuator and the step attenuators to reduce the level at the input to the final pair of amplifiers in the noise chain. The fine attenuator can, by this method, be set with a resolution of 1 dB to any part of its dynamic range provided that the resulting noise level at this output is ≤ -10 dBm and ≥ -152 dBm/Hz.* The highest crest factor that can be so obtained is typically 25 dB.

The following general procedure lets the user establish a desired noise crest factor between 15 dB and 25 dB with a given carrier level and C/N ratio. Let the desired crest factor be k dB, where k is an integer such that $15 \leq k \leq 25$. Then:

1. Start with the desired C/N ratio as the current entry.
2. Enter desired C/N ratio incremented by ≥ 12 dB.
3. Enter desired C/N ratio incremented by x dB, where $x = 20 - k$.
4. Reenter desired C/N ratio (if x is not zero).

*Value in dBm is filter dependent.

Reference

1. I. Young and G. Waters, "Practical Error Probability Estimation for Digital Radio Systems in the Presence of Interference and Noise of Finite Crest Factor, and the Prediction of Residual Error Rate," *IEE International Conference on Measurements for Telecommunication Transmission Systems—MTTS 85*, IEE, London, November 27-28, 1985.

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Finite Crest Factor Noise

The injected noise used in C/N testing must fulfill certain criteria: it must have sufficient bandwidth, a defined spectral density, and the correct statistics. The last requirement is frequently ignored.

The crest factor of a waveform is the ratio of the peak voltage to the rms value. An ideal Gaussian noise source process has infinitely high peaks. In other words, there is a finite chance that a peak as high as 7σ will occur, even though this probability is only 1 in 10^{12}. In practice the maximum noise output is constrained by power supply limitations. Gaussian noise with an infinite crest factor always produces a small but finite BER, no matter how large the C/N ratio is. However, when the crest factor is finite, reducing the noise below a certain threshold (or equivalently, raising the C/N ratio above a certain limit) makes the BER zero.

The theoretical probability of various symbol error rates has been computed for N-phase PSK (phase shift keying) and QAM (quadrature amplitude modulation) systems for various finite crest factors. The results are shown in Fig. 2. The effect of noise crest factor on the error rate can be seen together with the bound in C/N ratio discussed above where the error rate falls to zero. The crest factor should be high enough to allow accurate measurement at the appropriate BER. If this is not the case, the BER-versus-C/N-ratio plot for the radio under test can deviate significantly from the theoretical curve, and different noise sources will produce different deviations. A critical factor in the design of the HP 3708A was to maximize the noise crest factor. Over the dynamic range of the instrument, typical values of 15 dB to 25 dB are achievable.

HP 3708A Principles of Operation

Two methods of establishing a C/N ratio have been described. The additive noise or noise injection method is used by the HP 3708A (see Fig. 3). Noise of known spectral density is injected into the IF section of the receiver under test to establish the desired carrier dependent ratio (C/N,

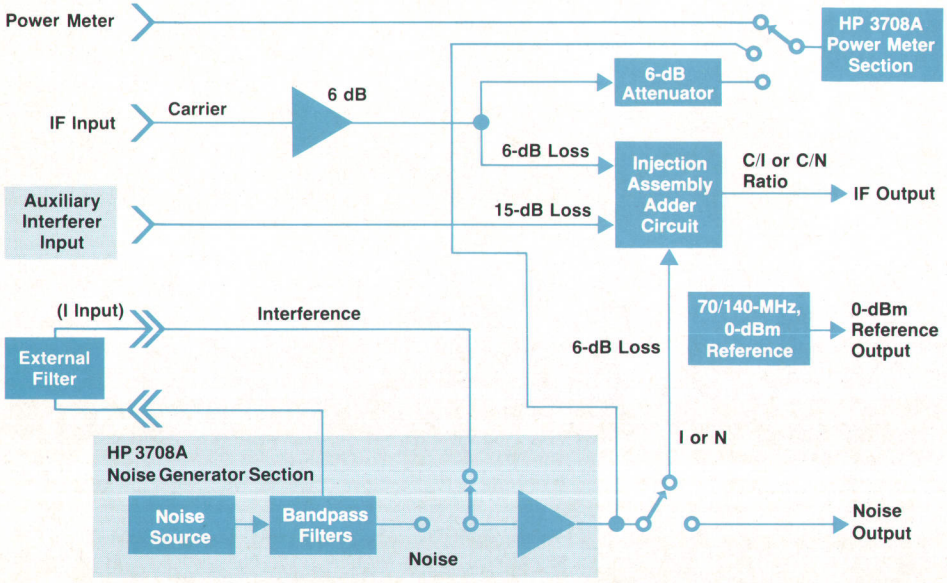

Fig. 5. *Block diagram of HP 3708A.*

Noise Bandwidth Measurement

The HP 3708A can measure the equivalent noise bandwidth of bandpass filters centered at 70 MHz or 140 MHz. This measurement is automatic except for one connection change. Other filters in the range of 10 to 200 MHz can be automatically measured after the insertion loss at the filter center frequency is entered into the HP 3708A.

The filter noise bandwidth (NBW) is the width in Hz of a rectangular filter that gives the same total noise power output as the actual filter, and has the same level of output noise density at the center frequency. An NBW of 10 MHz might be expressed as 70 dB-Hz where NBW (dB) = 10 log NBW (Hz). An NBW of 20 MHz would pass twice the power and would be given as 73 dB-Hz.

The HP 3708A measurement sequence starts with a gain or loss measurement of the filter under test at the band center frequency (70 MHz or 140 MHz). Using the gain or loss value and the input noise density, the HP 3708A calculates the output noise density at the center frequency. The total output power divided by this output noise density gives the NBW, which is then displayed on the front panel.

Fig. 1 shows a noise bandwidth calculation for a 70-MHz filter. In Fig. 1, the filter output noise density is 1 μW/Hz at 70 MHz and so a bandwidth of 1 MHz at this noise density must be postulated to account for the output power of 1 watt. The equivalent noise bandwidth is therefore 1 MHz. In this case the input noise density is 2 μW/Hz since there is a 3-dB loss at the band center.

Fig. 1 also illustrates a method of measuring noise power density. When the output power, NBW, and loss of the filter are known, the input noise density can be calculated. For example, since the output power is 1 watt, the noise bandwidth is 1 MHz, and the loss at 70 MHz is 3 dB, the constant-level input noise density extending over the test-filter window must be 2 μW/Hz.

The shape of the filter response is not critical. The filter and power meter represent a black box. This method is used to measure the output noise density of the HP 3708A in production test. Periodic calibration of the filter and power meter combination to find the relation between input noise density and power meter reading is carried out by a computer-controlled routine using a signal generator, a power meter, and numerical integration.

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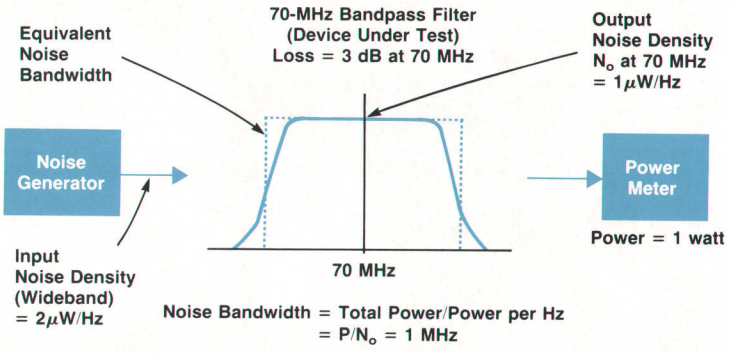

Fig. 1. *Derivation of noise bandwidth NBW from total output power and output noise density at 70 MHz.*

C/N_o, or E_b/N_o). The receiver IF power is measured at the point of noise injection, and the noise density is adjusted automatically under microprocessor control to maintain the required carrier dependent ratio in the presence of received signal level variations. The typical instrument response time is 10 ms, which enables BER testing to be performed in the field in the presence of rapid changes in RSL. Fig. 4 shows the injected noise tracking sinusoidal variations in IF signal power at 50 dB/s and 10 dB/s. Because the carrier power is measured at the point of noise injection, the required carrier dependent ratio is maintained at any point chosen for noise injection throughout the IF chain.

The block diagram of the instrument consists of a power meter, a noise source, an injection assembly, and a microprocessor (Fig. 5). To this is added a 0-dBm reference source, an HP-IB (IEEE 488/IEC 625) port, and a power supply.

The user's radio signal is passed through the injection assembly via the HP 3708A's IF input and output ports. The injection assembly has 0-dB loss and negligible transmission impairments to carrier powers as high as 5 dBm.

Noise injection is controlled by a switched attenuator and a continuously variable pin diode attenuator in the noise source. When a requested C/N ratio is established, the microprocessor sets the switched attenuator so that the pin diode attenuator is in the middle of its range. This allows a rapid variation of the noise level over ±5 dB without operating the switched attenuator, which ensures fast response to carrier variations. In some special applications this noise tracking facility is not required and a track inhibit mode of operation is available.

The HP 3708A can be used to test TDMA (time division multiple access) burst mode systems. The carrier power is measured with an external burst mode power meter and entered into the HP 3708A using the **ENTER C** data entry key in track inhibit mode.

Special Features

Three ratios are available on the HP 3708A: carrier-to-noise ratio, carrier-to-noise-density ratio, and energy/bit-to-noise-density ratio. The last two ratios are independent of bandwidth and are particularly useful in R&D work for comparing the efficiency of different radio systems. These measurements require an accurately known noise density

for injection into the radio's IF section. The concept of E_b/N_o ratio results in a figure of merit for comparing systems that emphasizes the minimization of the total transmitted energy required to convey a given amount of data. E_b is obtained by dividing the carrier power C by the bit rate f_b. Therefore, $E_b/N_o = (C/f_b)(1/N_o)$, or in dB, $E_b/N_o = C/N_o - 10 \log f_b$.

After measuring the IF carrier power, the HP 3708A must know the transmission bit rate of the system under test to inject the appropriate noise density to establish a required E_b/N_o. This can be entered via the data entry keys on the front panel. If the receiver noise bandwidth is B_e Hz and the total noise power measured in this bandwidth is N watts, then $N_o = N/B_e$ watts/Hz. Hence, $E_b/N_o = (C/N)(B_e/f_b)$, or in dB, $E_b/N_o = C/N - 10 \log f_b/B_e$. Therefore, if the noise bandwidth equals the bit rate, $E_b/N_o = C/N$.

The measurement of the BER of a system at a particular C/N ratio must be related to a specified system bandwidth (e.g., the noise bandwidth of practical receiver filters) or to the theoretical minimum Nyquist bandwidth (symbol rate bandwidth). Therefore, a system bandwidth key is associated with the C/N data entry key on the HP 3708A. This allows noise of appropriate noise density to be injected at a convenient point in the radio's IF section to establish a required C/N ratio at another point (e.g., downstream in the bandwidth of the baseband filters at the regenerator input).

The HP 3708A operates at common microwave receiver IF bands from 10.7 MHz to 140 MHz. The injected noise is band limited in the range of 10 MHz to 200 MHz by a choice of four internal filters or by connecting an external filter of the operator's choosing. To ensure that the injected noise density is calibrated, the noise bandwidth of each filter in each instrument is individually measured and stored as a soft constant.

Because the HP 3708A contains an accurate noise source, an IF power meter, and a microprocessor, the instrument can be configured to measure the noise bandwidth of an external filter in seconds, thus avoiding the lengthy numerical integration procedures normally used (see "Noise Bandwidth Measurement," page 23). To increase the instrument's flexibility, both its internal power meter and its noise source are accessible from the front panel for more general-purpose applications.

Additive Interference Testing

The HP 3708A offers two distinct facilities for interference testing. Aimed at different applications, both facilities have broadband inputs with a frequency range of 10 MHz to 200 MHz.

Co-channel and adjacent channel interference effects influence the design of radio hardware and are of interest to the frequency planner and regulatory agencies. These effects can have a predominating influence on the BER performance of a radio. It is common practice to measure the C/N threshold degradation that occurs in the presence of interference over a range of co-channel and adjacent channel frequencies. Fig. 6 shows a typical co-channel C/I (carrier-to-interference) plot for an 8-phase PSK radio. The degradation in threshold can be seen clearly.

To simplify this measurement, the HP 3708A has an auxiliary interferer input on its rear panel with a fixed loss to the HP 3708A's IF output port of typically 15 dB. The required C/N ratio is established via the keyboard in the normal manner and the C/I ratio is determined by the level presented to the auxiliary interferer input. In this mode of

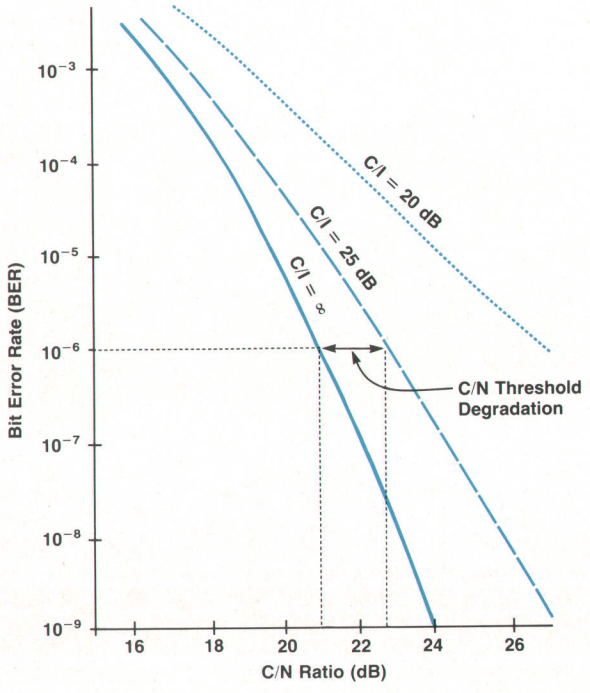

Fig. 6. *Typical co-channel carrier-to-interference ratio plot for an 8-phase PSK radio.*

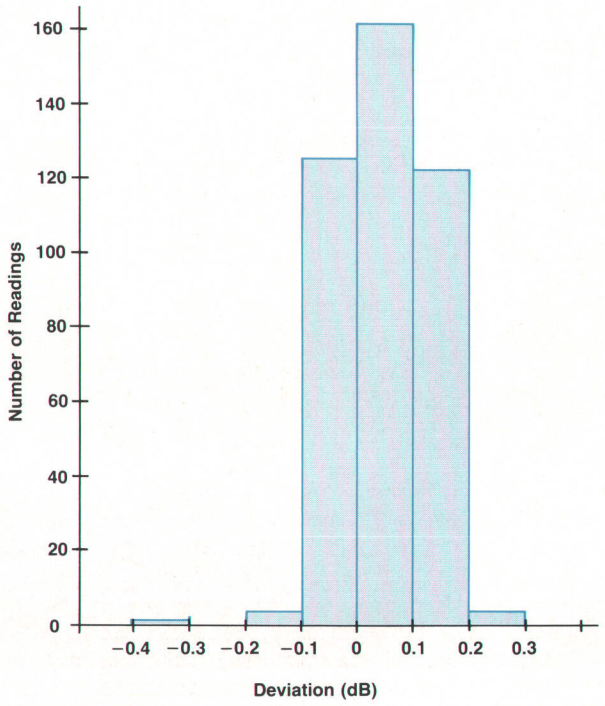

Fig. 7. *C/N ratio repeatability for HP 3708A measurements at 70±20 MHz.*

operation the established C/N ratio is independent of variations in received carrier power, but the C/I ratio is not.

An external source of interference (modulated or unmodulated) can be used or the internal 0-dBm calibrator (normally at 70 MHz and 140 MHz) can be substituted.

Because of a growing interest in deterministic testing of QAM radio systems (rather than statistical testing with noise), the C/I mode of the HP 3708A allows the injection of a noise-free additive sinusoidal tone. In this mode of operation the automatic leveling algorithm maintains the C/I ratio in the presence of received signal level variations. The interferer is connected to the input port on the instrument's front panel.

The residual BER of a radio system at nominal received signal level is practically impossible to measure because the mean time between errors can be from tens to hundreds of hours. The C/I ratio required to establish a specific BER depends on the amount of intersymbol interference and residual noise present around the phase states in the constellation display. The estimation of this C/I ratio can be used to predict the residual, or dribble, BER for a radio system. This technique is described in reference 2.

Measurement of residual BER can now be made in minutes as opposed to the three days previously required to wait for 30 errors (100 Mbits/s, BER = 10^{-12}). Measurement of residual BER is now feasible in the field and test time can be saved in production, allowing repeated tests to be made for evaluation of adjustments.

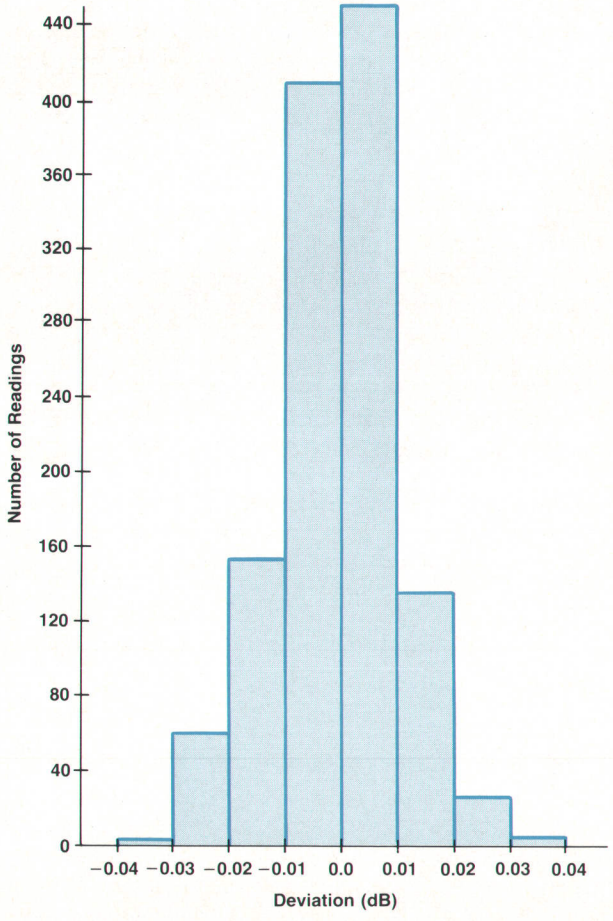

Fig. 8. *Linearity of internal HP 3708A power meter over 1240 measurements.*

Self Calibration Enhances Accurate Operation

When measuring the fade margins of a microwave radio system, the accuracy with which the C/N ratio can be specified is of vital importance. This is primarily because the slope of the BER-versus-C/N-ratio curve is so steep that less than a 0.5-dB change in C/N ratio can result in one order of magnitude variation in BER. Hence, the HP 3708A uses a powerful 16-bit microprocessor to implement sophisticated calibration procedures that enable a C/N or C/I ratio to be established to a typical accuracy of 0.1 dB at room temperatures.

Each signal path in the HP 3708A and the noise bandwidths of the noise defining filters are characterized by individually measured software constants. This calibration data is held in nonvolatile memory. The exact values are determined for each instrument during production test to achieve maximum accuracy. Thirty-three soft constants are stored in each HP 3708A. These constants are:

1. RF path gains and losses
2. Filter noise bandwidths
3. Measured attenuator incremental attenuation values.

A temperature sensor ensures that an autocalibration cycle is initiated should the noise source temperature change by 3°C or more.

The power meter can be calibrated using the accurate internal 0-dBm source described in the article on page 30, and subsequent measurements are referred to this level.

The HP 3708A specifications include test station measurement uncertainties and guarantee traceability to international standards. C/N ratio accuracy and repeatability are measured by a substitution method. A precision calibrated attenuator is used to attenuate the carrier signal until its power is within ±1 dB of the noise being generated by the HP 3708A under test at a specific C/N ratio. The noise and attenuated carrier power levels are then measured separately on the same range of an HP 438A Power Meter connected to the IF output port of the HP 3708A. The error in the C/N ratio is computed from the measured results and known calibration data for the attenuator. For a typical production HP 3708A, C/N ratio accuracy was measured at carrier powers of 5, 1, −2, −5, −10, −20, and −40 dBm and at C/N ratios of 0, 10, 20, 30, and 40 dB. The test was repeated automatically 416 times and consisted of 26 combinations of carrier power and C/N ratio. The C/N ratio repeatability is shown in Fig. 7. For 16 out of the 26 combinations the standard deviation of the C/N ratio accuracy was less than 0.01 dB. The standard deviation of the mean of the 26 combinations was 0.02 dB. The C/N ratio accuracy was ±0.06 dB with 99.7% confidence. These measurements were made with noise generated via the 70±20-MHz internal filter.

Power meter linearity was measured at 31 different power levels from 6 to −45 dBm and the test was repeated 40 times, resulting in 1240 measurements. The results are shown in Fig. 8. The power meter is linear to ±0.03 dB with a 99.7% confidence level.

Acknowledgments

I would like to thank the following people for their enthusiasm and contributions to the instrument. Brian Woodroffe developed the firmware, HP-IB circuitry, and microprocessor circuitry. David Stockton, whose ideas are to be found in many parts of the instrument, designed the C/N switch in the power meter, and developed the noise filter board. Daya Rasaratnam designed the power supply and Ian Matthews developed the noise injection assembly and power meter attenuator. James Gentles was the production engineer. Harry Elder was responsible for the product design.

References

1. G. Waters, "Digital Radio Measurements," *Telecommunication Measurements, Analysis and Instrumentation*, K. Feher, editor, Prentice-Hall, 1986.
2. I.K. Compston, *Methods for Estimating Residual BER in Digital Radio*, Hewlett-Packard Company, Publication No. 5954-2036.

Microprocessor-Enhanced Performance in an Analog Power Meter

by Anthony Lymer

THE HP 3708A NOISE AND INTERFERENCE TEST SET can be used to test microwave point-to-point radios. It simulates flat (frequency independent) fading and co-channel and adjacent channel interference by injecting band-limited noise or interference into the IF stages of the radio. The instrument continuously monitors the incoming carrier level and adjusts the impairment level to maintain an accurate carrier-to-noise (C/N) ratio or carrier-to-interference (C/I) ratio. This feature is particularly convenient when live radio traffic is being used as the test signal to measure fade margin. The radio signal may vary because of multipath interference effects. A 0.5-dB change in signal level might, in the absence of a tracking C/N test set, lead to an order of magnitude change in bit error rate (BER) for the link, making repeatable measurements difficult to obtain.

A special feature of the HP 3708A, its tracking capability, demands a very fast response time from the power meter that measures the incoming carrier level and the impairment level. A settling time of 3 ms has been achieved, so the instrument response time is limited by the rate at which the processor samples the carrier and updates the noise output, and not by the power meter. A custom thermal converter IC manufactured by HP[1] is used to achieve both short settling time and true rms response. The latter is important when dealing with white Gaussian noise and with both sinusoidal and modulated digital radio signals.

Since carrier power and noise power are not usually measured at the same levels, the linearity of the power meter over its range of 5 dBm to −45 dBm is of critical importance. A very simple but powerful enhancement technique employing a microprocessor solves the problem of producing the very accurate attenuators necessary to meet the stringent linearity requirements of C/N ratio testing. Operator conveniences such as automatic sensor zeroing with temperature changes, the capability of calibrating the power meter against the built-in 0-dBm reference oscillator at the touch of a button, variable-time-constant averaging, and calculation of filter noise bandwidths are easy and cheap to provide. HP-IB control eases the problems of test-

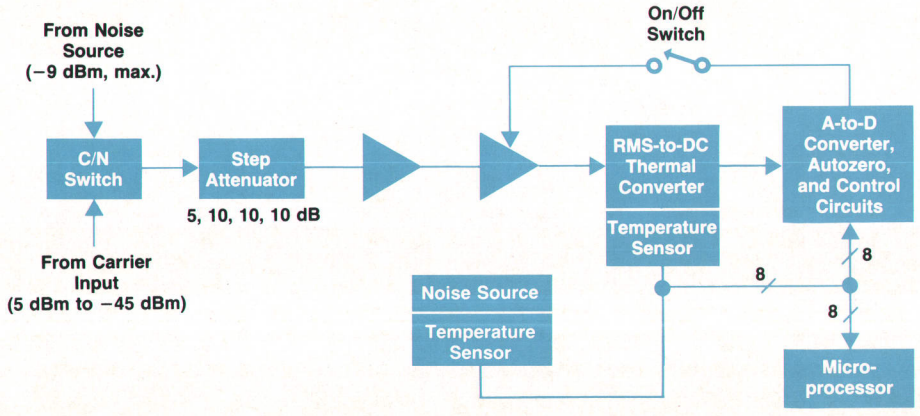

Fig. 1. *Block diagram of the HP 3708A's internal power meter.*

ing the instrument, so it is no longer an optional extra. These were major influences on the design of the power meter section of the HP 3708A.

Dual-Purpose Power Meter

A block diagram of the power meter is shown in Fig. 1. The first functional block is a pin diode switch (Fig. 2) which selects either the carrier at the IF input or the noise from the final amplifier in the noise chain. This is followed by a processor-controlled step attenuator with one 5-dB and three 10-dB sections. These values were chosen to reduce the need to change range with cyclically varying signals. Such signals occasionally occur in microwave radio links. The basic rms converter operates over a 12-dB range without loss of accuracy. With a 5-dB difference between ranges, a signal must vary by at least 7 dB to require a change in range (Fig. 3). If only 10-dB ranges were used, a 1-dB peak-to-peak fade at either end of a range would be enough to produce switching relay chatter, causing unnecessary wear.

To increase the signal level to a suitable power for the thermal converter, a 50-dB fixed-gain amplifier is provided. The final stage is electronically switchable so that the thermal converter can be isolated from the RF input when it requires zeroing. Finally, the signal reaches the thermal converter, where the dc value equivalent to the true rms voltage of the input signal is generated and converted to a 12-bit binary number. This number forms the address of a lookup table for the power level in dB seen at the thermal converter input. A simple calculation is made by the processor using the loss in the step attenuator, gain in the amplifier chain, and power at the thermal converter to give the power at the IF input in dBm.

PIN-Diode Switch Isolation

The C/N switch (Fig. 2) selects either the carrier path or the noise path for power measurement. If noise leaks through the switch when the carrier is selected, then inaccurate readings will result. This is also true when noise is selected, but the problem is less severe.

The required isolation can be estimated by considering the maximum noise power at the switch input, −9 dBm, and the minimum carrier signal expected, −45 dBm. The power difference is 36 dB. For the carrier power to be accurate to 0.01 dB, it can be shown that the carrier must be greater than the noise by another 26 dB. So, an isolation of 62 dB is needed. Because of the broadband nature of the noise and modulated carrier signals, amplitude response with frequency and return loss at the inputs are also of importance. The input attenuator (R1, R2, and R3) ensures a good match and allows the dc switching current for the diodes to be injected. A positive control voltage switches D1 and D2 into conduction and reverse biases D3, D4, and D5. This allows power to reach the output. If a negative control voltage is applied, D1 and D2 block the signal path while D4 and D5 shunt any leakage through D1 to ground. D3 is also forward biased and allows R4 to terminate the attenuator in its characteristic impedance. A second identical section is used for the other input channel, with all the diodes reversed so that the same switching voltage can be used. The low ground impedances and the level of screening required made it necessary to house the C/N switch in a machined enclosure with some components mounted in individual cavities.

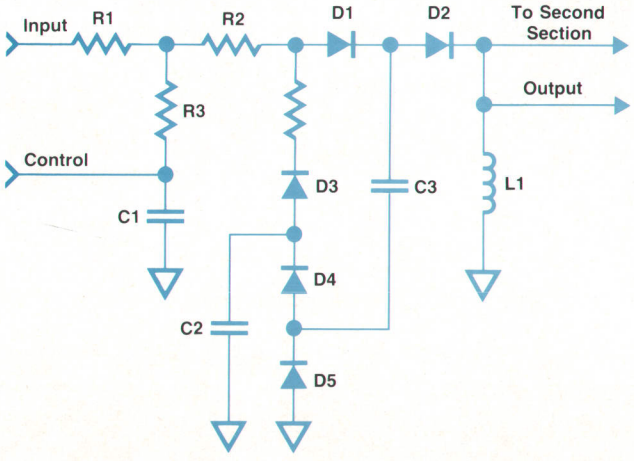

Fig. 2. *C/N pin diode switch (one of two channels).*

Software-Enhanced Accuracy

The overall power meter linearity specification of 0.1 dB does not allow the individual attenuator sections to be more than 0.01 dB different from the nominal values. It seemed an impossible task to manufacture attenuators in

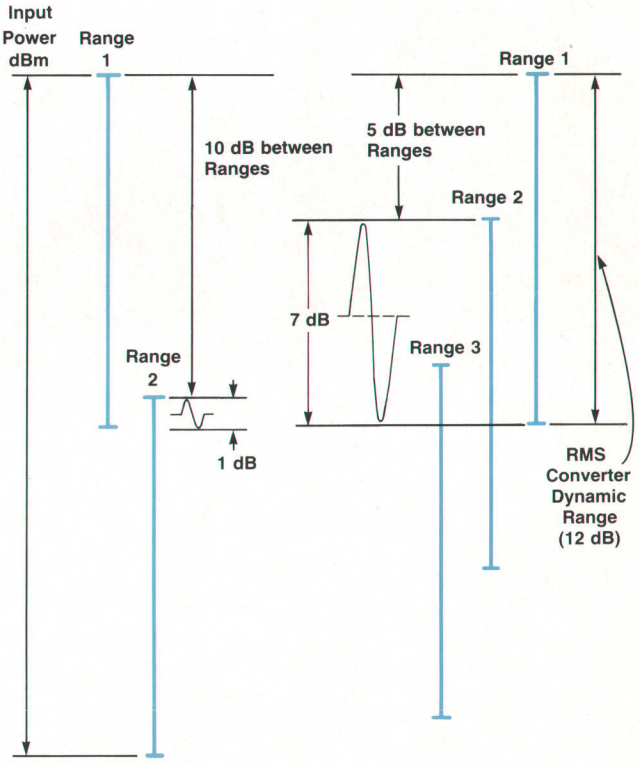

Fig. 3. *Power meter ranges. With 10-dB differences between ranges (left), a signal greater than 1 dB peak-to-peak may require a range change. With 5-dB differences between ranges, as in the HP 3708A (right), a signal must vary in level by at least 7 dB to effect a change in range.*

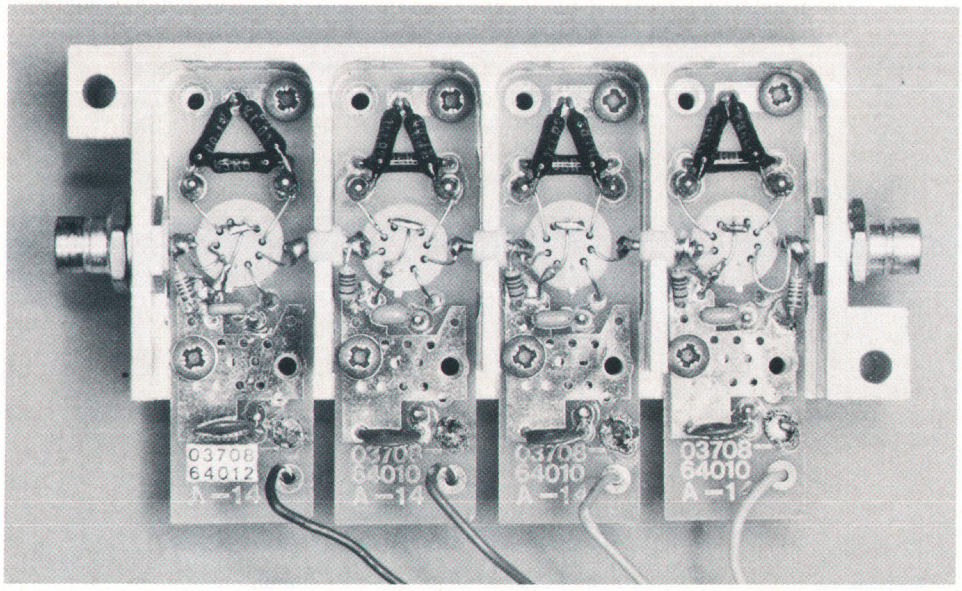

Fig. 4. *Photograph of programmable input attenuator.*

quantity to this standard. The solution adopted uses the computing power available to enhance the accuracy. The attenuators are measured in the power meter circuit at final calibration and the measured value is used by the computer in any calculations. These values and others, such as the measured gain of the power meter amplifiers, are stored in electrically erasable read-only memory (EEPROM) on the processor printed circuit board. The idea was so successful it was extended. Thirty-two calibration values are now stored in this way, including noise bandwidths of filters and noise step attenuator values. Consequently there is only one gain adjustment in the entire power meter.

The programmable attenuator used in power meter autoranging is shown in Fig. 4. Each compartment contains a printed circuit board loaded with a relay (TO-5 case size) and a 75Ω attenuator section. The amplitude response from 10 MHz to 200 MHz shows an almost constant droop at all attenuator settings. The droop is caused by the RF loss of the TO-5 case header and is compensated by the following amplifier.

Power meter calibration is accomplished by connecting a 0-dBm level to the power meter input and pressing a key. The processor notes the power reading obtained and subtracts this value from the input power, forcing the meter to read 0.00 dBm. The 0-dBm calibration source provides the common digital radio IF frequencies of 70 MHz and 140 MHz.

Variable-time-constant averaging is another operator convenience made possible by the microprocessor at very low cost. Short-term variations in a signal can be averaged to give a more stable display when desired. At power-on, the power meter time constant defaults to around 150 ms, but can be reduced to around 15 ms or increased to 3 seconds. Settling time is about 3 to 4 time constants.

True RMS Thermal Converter

The HP 3708A's power meter must measure sinusoidal unmodulated carriers, carriers with digital modulation, and band-limited (pink) noise. It is important that a true rms value is measured and not an average value as would result from a diode detector. The true rms voltage is the dc value that gives the same heating effect as the incoming waveform. Using a thermal converter with two resistor-diode sensors ensures that this happens. The circuit diagram is shown in Fig. 5. The RF signal is applied to R1, which is in close thermal contact with D1. The voltage across D1 has a temperature coefficient of −2.2 mV/°C. The combination of R1 and D1 heats up by about one degree Celsius per milliwatt of RF supplied to R1. D2 and R2 are another resistor-diode pair matched to D1 and R1, but thermally isolated from them. The difference between V1 and V2 is amplified, integrated, and fed back to resistor R2. The output of the integrator completes the negative feedback loop and ensures that the power in R2 is the same as in R1. Therefore, the voltage at the output of the integrator is proportional to the rms voltage across R1.

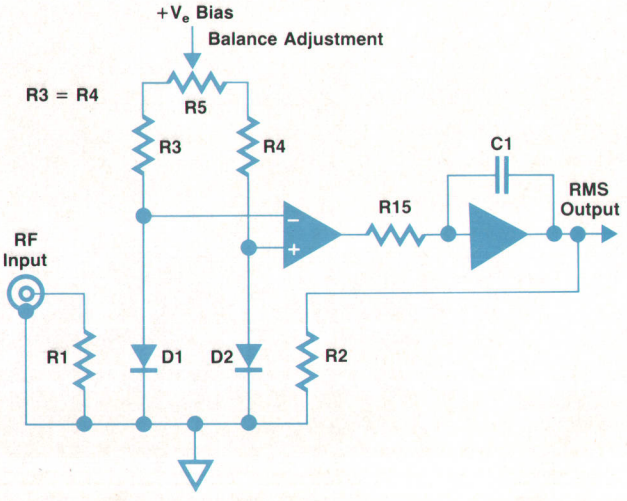

Fig. 5. *Thermal converter circuit.*

Thermal Effects

Several causes of inaccuracy and nonlinearity in this kind of power meter are thermal in origin. They include the thermal EMF generated at the copper/Kovar™ lead junctions, temperature drift of the offset voltage of the sensor diodes and associated amplifier, and excessive heating caused by an overload in the thermal converter.

The magnitude of the thermoelectric voltages generated at the copper/Kovar junctions can be as much as 35 μV/°C. The temperature differences can be caused by the proximity of heat-producing components or by the forced air cooling system in the instrument. In the HP 3708A's thermal converter, these effects are reduced by housing the sensor diodes and low-level amplifier in a metal housing which provides shielding from drafts and reduces any temperature gradients in the vicinity of the sensor diodes to negligible proportions.

The effects of offset voltage drifts can be estimated as follows. If the ambient temperature seen by the sensor diodes and low-level amplifier changes by one degree Celsius, then the diode balance will have altered typically by 3 μV. The effect of one milliwatt of power dissipated in the input resistor heats the diode by about 1°C. This leads to a reduction in the diode voltage of about 2.2 mV. The 3-μV offset adds to or subtracts from the 2.2-mV signal. This results in an error of:

$$(2.2\text{ mV} + 3\ \mu\text{V})/2.2\text{ mV} = 1.00137 \text{ or } 0.012\text{ dB/°C}$$

Kovar is a trademark of Westinghouse Electric Corporation.

For an input signal of 10 mW, the effect is reduced and the error is only ±0.0012 dB/°C.

For a 30°C change in ambient temperature the total error at 0 dBm would be about ±0.36 dB, which is unacceptable in this design. Clearly some form of automatic zeroing was called for to reduce the size of this potential error source.

Autozero Circuit

Errors caused by thermal drift are controlled by the autozero circuit (Fig. 6). Autozeroing is performed under processor control at power-on and at other convenient times such as on a change of instrument mode. Thereafter the autozero runs when either of two temperature sensors detects a 3°C change in temperature. One of the sensors is mounted in the housing alongside the thermal converter IC. The other sensor is mounted next to the HP 3708A's noise source. If the possibility of calibration occurring during a measurement procedure is unacceptable, then this facility can be disabled.

The autozero sequence begins with the RF input signal to the thermal converter being removed by switching off the final amplifier in the power meter gain block and inserting full attenuation. The dc feedback loop is broken by switching Q4 on, pinching off Q3. The diodes now exhibit only the offset voltage to be nulled. The sign of this voltage is sensed at the output of U3 by U8, which controls the direction of counting in U6, an 8-bit binary up/down counter. The processor releases the inhibit line, allowing the counter to run. If U3's output is less than 0V, then the counter increments and the digital-to-analog converter

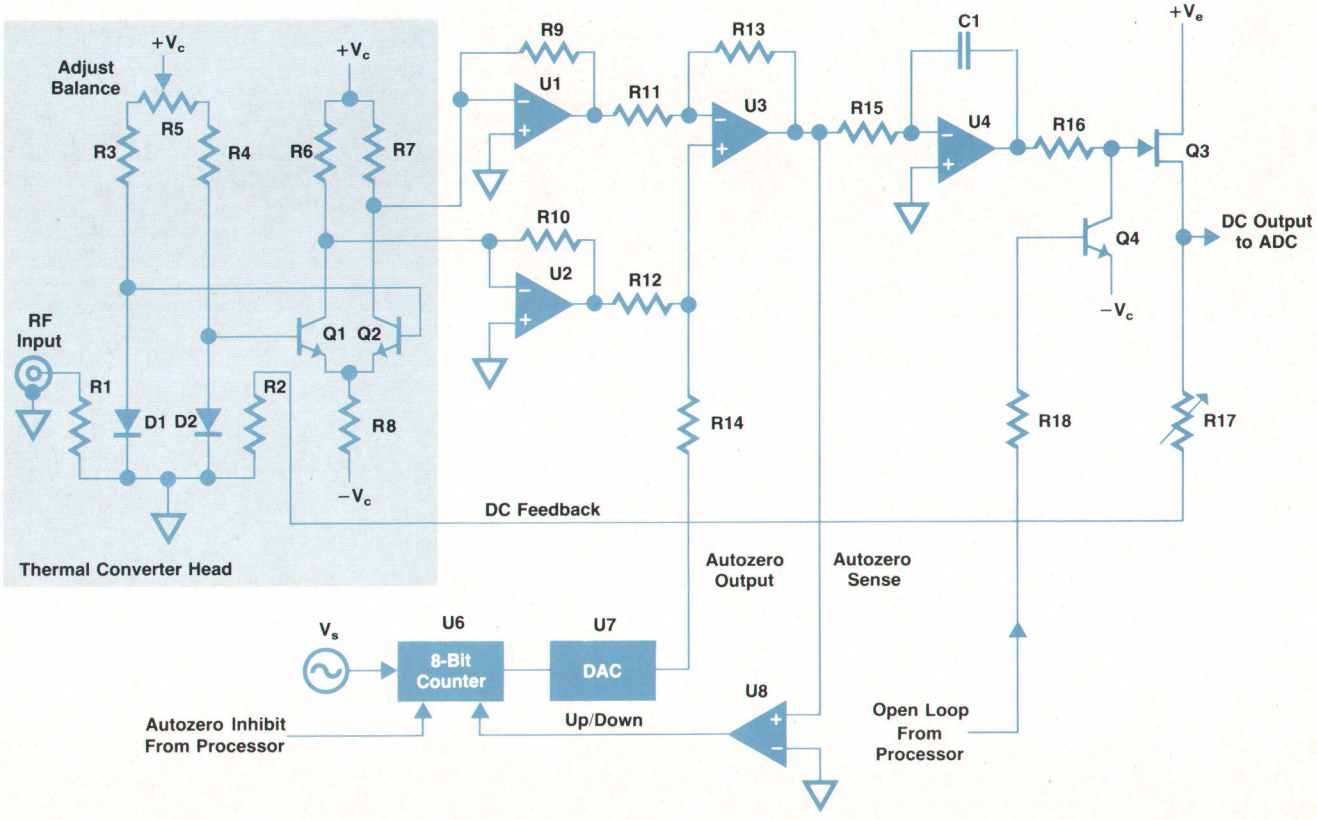

Fig. 6. *Thermal converter and autozero circuit used in the HP 3708A's internal power meter.*

(DAC) U7 gives a greater output, bringing U3 closer to the desired 0V. This continues until the output of U3 becomes greater than 0V. The output of U8 changes value, forcing the counter to decrement and the autozero loop to limit cycle: a step up, then a step down. The processor inhibits the counter at the end of the cycle after 500 ms. The last counter state remains on the DAC input until the next autozero operation. This nulls the diode and amplifier offset voltages at that temperature. Finally, the loop is closed by switching Q4 off, and the power meter amplifier is reactivated, restoring status quo.

Log Conversion

The dc output from the rms converter is digitized and used as the address for a lookup table, stored in ROM, which converts the 12-bit analog-to-digital output to dB form. This process results in much greater accuracy and stability than an analog log converter, yet saves the processor considerable time in calculating the logarithm each time. Input power is calculated by summing the individually measured values of amplifier gain and attenuator section values algebraically with the rms converter output.

Acknowledgments

Thanks are due Geoff Waters, project manager, who designed the thick-film hybrid amplifiers (see box, page 33) used in the gain block and to Ian Matthews who completed the rest of the RF design. Dave Stockton contributed the C/N switch and Harry Elder was responsible for the product design. Brian Woodroffe wrote the operating software.

Reference

1. P.M. O'Neill, "A Monolithic Thermal Converter," *Hewlett-Packard Journal*, Vol. 31, no. 5, May 1980, p. 12.

An Accurate Wideband Noise Generator and a High-Stability Reference Source

by Dayananda K. Rasaratnam

THE HP 3708A NOISE AND INTERFERENCE TEST SET simulates microwave flat fade conditions by injecting noise of defined spectral density into the IF section of a radio receiver. It automatically maintains a selected carrier-to-noise (C/N) ratio by adjusting the noise power level so that reliable measurements can be made to evaluate the performance of the radio. This requires an accurate wideband noise generator and a high-stability reference source in the instrument.

Noise Generator

The noise generator is designed to meet the following requirements:

- Flat broadband (10 MHz to 200 MHz) white noise with a large crest factor (>15 dB)
- A selection of noise-band-defining filters
- High accuracy (absolute level error $<\pm 0.5$ dB) and high resolution (<0.02 dB)
- Large dynamic range (6 dBm maximum total power to −154 dBm/Hz*)
- Fast level tracking within any 10-dB window in the dynamic range
- Remote control of level and filter selection.

The noise generator (Fig. 1) is made up of a cascade of gain stages, switchable band-defining filters, and program-

*Total power in dBm is filter bandwidth dependent.

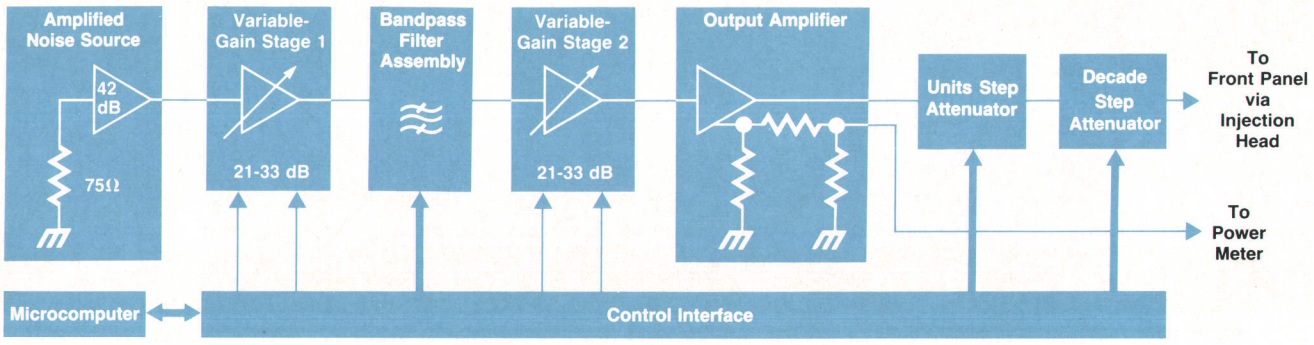

Fig. 1. *Block diagram of the internal noise generator for the HP 3708A Noise and Interference Test Set.*

mable step attenuators. To meet the required specifications and because of the high gain (≈100 dB) in the forward path, particular care was given during the design phase to such aspects as RF grounding, RF screening, mechanical layout, and cooling. The requirement for noise with a large crest factor was also an important consideration and the gains and losses in the path of the generator were distributed in such a way that this requirement would not be compromised.

The amplified noise source consists of a cascade of amplifiers terminated at the input with a passive resistor. Virtually all the noise in the output of the noise generator originates from the terminated input stage of this 42-dB gain block. A variable-gain stage is incorporated at two locations in the generator; each consists of a variable pin diode attenuator and 34 dB of gain. The filter assembly uses pin diode switches to facilitate the remote selection of any one of four internal band-defining filters or a filter connected across a pair of front-panel ports. One of these ports can also be used for the injection of an interfering tone. The output amplifier has two outputs. One of these outputs feeds into the input of a cascaded pair of step attenuators while the other can be selected by a switch for connection to the input of the internal power meter. The step attenuators are precision programmable units from the HP 33320 Series with resolutions of 1 dB and 10 dB.

The output from the step attenuators is fed to one of two front-panel ports via the injection head, depending on the selected mode of operation. In the noise generation mode the maximum power level at the noise output port is 6 dBm. In the C/N mode, however, a loss of 6 dB in the injection head results in a maximum noise power level at the IF output port of 0 dBm.

Remote control of the noise power level is achieved by means of the pin diode attenuators and step attenuators. The internal power meter is used to measure the noise power level at the input to the pair of step attenuators. This measurement is used to determine the settings of the step and pin diode attenuators for a given noise level at the front panel.

Step Attenuator Calibration. The step attenuators are specially calibrated when the HP 3708A is set up in production. This calibration is effected by comparison with a pair of standard attenuators that have been measured accurately by an HP standards laboratory. The calibrated attenuator values are entered into electrically erasable programmable read-only memory (EEPROM) and the HP 3708A's internal microcomputer uses these values to adjust the noise output level.

PIN Diode Attenuators. The pin diode attenuators in the variable-gain stages and the means of controlling them are designed so that the high resolution and fast tracking capabilities of the noise generator can be achieved without compromising the specifications for flatness and accuracy.

A pin diode appears as an almost pure resistance at RF and this resistance is a function of dc bias current. This property of the pin diode makes it a very suitable element for implementing a continuously variable attenuator. Such an attenuator with constant input and output impedances can be realized with the bridged-T configuration.[1] This configuration also results in good flatness and lends itself to temperature compensation. The attenuation of the bridged-T circuit (Fig. 2) can be varied while maintaining its characteristic impedance Z_o at a constant value by varying R1 and R2 in such a way that:

$$R1 \times R2 = Z_o^2 = \text{constant} \quad (1)$$

The forward RF resistance of a pin diode is given by:

$$R_f = r/I^x \quad (2)$$

where I is the dc bias current and r and x are constants for a given diode type. Assuming a matched pair of pin diodes taking the places of R1 and R2 in Fig. 2, we have:

$$Z_o^2 = R1 \times R2 = r^2/(I_1 \times I_2)^x \quad (3)$$

It can be seen that the product of I_1 and I_2 must be held constant to satisfy equation 1.

The forward voltage V_f of a pin diode is related to its forward current I_f by the relationship:

$$I_f = I_s \exp(qV_f/kT) \quad (4)$$

where q is the charge on an electron, k is Boltzmann's constant, T is the absolute temperature in Kelvin, and I_s is the reverse saturation current. Therefore:

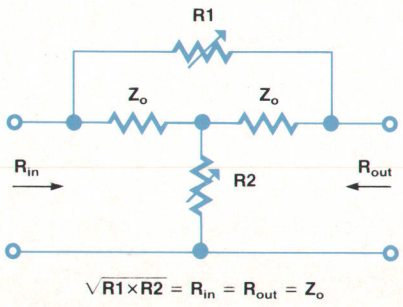

Fig. 2. *Bridged-T circuit variable attenuator.*

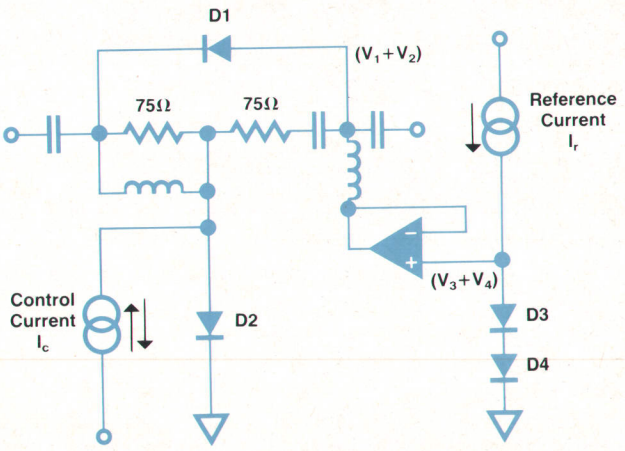

Fig. 3. *Method for biasing bridged-T pin diode attenuator to maintain its characteristic impedance with varying temperature.* $V_1+V_2=V_3+V_4$.

$$I_1 \times I_2 = (I_{s_1} \times I_{s_2}) \exp[q(V_1 + V_2)/kT] \quad (5)$$

and $I_1 \times I_2$ will be a constant if $V_1 + V_2$ is a constant, but only at a fixed temperature.

Temperature compensation is necessary if the characteristic impedance of the pin diode attenuator is to be maintained in a changing environment. Fig. 3 illustrates a means of biasing the attenuator and maintaining its characteristic impedance with varying temperature.[2] The voltage developed across pin diodes D3 and D4 by the reference current I_r is applied across pin diodes D1 and D2 in the attenuator. I_r is adjusted to give the desired characteristic impedance at the attenuator ports.

The reverse saturation current I_s can be written as:

$$I_s = Mf(T)$$

where M is a constant for a given diode and f(T) is a function of absolute temperature. Then equation 5 can be written as:

$$I_1 \times I_2 = (M_1 \times M_2)f^2(T) \exp[q(V_1 + V_2)/kT]$$

Since the same current flows through both D3 and D4, from equation 4 we have:

$$I_r^2 = (M_3 \times M_4)f^2(T) \exp[q(V_3 + V_4)/kT].$$

If $V_3 + V_4$ is maintained equal to $V_1 + V_2$ and I_r is held constant as in Fig. 3, then $I_1 \times I_2 = I_r^2 (M_1 \times M_2)/(M_3 \times M_4)$ will be constant, independent of temperature, and so will the characteristic impedance.

The choice between using voltage or current drive to control the attenuator, although influenced by such factors as resolution, was primarily determined by the requirement for temperature stability of the attenuation setting. The attenuation A as a function of control current I_c is given by:

$$A = 20 \log \left\{ (Z_o/r) \left[\frac{I_c + \sqrt{I_c^2 + 4(r/Z_o)^{2/x}}}{2} \right]^x + 1 \right\} dB \quad (6)$$

The variations of r and x with temperature and the consequent effects on the attenuation are small for the particular diodes used. The temperature variation of the characteristic impedance Z_o has also been compensated for. Thus, a significant reduction in the temperature dependence of the attenuation setting is achieved with the use of a temperature-stable current, rather than a voltage, to control the attenuator.

Further provision for maintaining the accuracy of the noise generator under varying environmental conditions is made with automatic adjustments to the drive currents of the pin diode attenuator in the second variable-gain stage. These firmware-driven adjustments are made when a characterization process (see below) is carried out; they supplement the hardware temperature compensation techniques.

Characterization

The high resolution and fast tracking capabilities of the noise generator are achieved by using the pin diode attenuator in the second variable-gain stage—the fine attenuator. While continuous monitoring of the noise level with the internal power meter ensures accuracy and stability in the noise generation mode of the HP 3708A, this technique cannot be adopted in C/N mode, when the power meter is preoccupied with continuously monitoring the incoming carrier level. In this latter case the attenuator is driven from a table in RAM. This table is generated by a routine that uses the internal power meter to make measurements of the noise level at chosen settings of the fine attenuator and then interpolates linearly between these cardinal points.

The time taken to characterize the attenuator is largely determined by the number of measurements, i.e., the number of cardinal points. Hence, it is desirable to keep the number of these points to a minimum. The attenuation characteristic of equation 6 can be rewritten as:

$$A = 20 \log \left\{ a[(I_c + \sqrt{I_c^2 + b})/2]^d + 1 \right\} dB \quad (7)$$

where a = 1.563, b = 1.31, and d = 0.8 are typical values with $Z_o = 75\Omega$. A plot (Fig. 4) with these typical values shows that this characteristic is nonlinear. The cardinal points must therefore be appropriately spaced if a minimal set with a given resolution is to be obtained. In the HP 3708A, a single fixed set of cardinal points is used. This set is derived by numerical methods from the second derivative of the theoretical characteristic.

A special hardware adjustment procedure ensures that deviations of practical characteristics from the theoretical curve are small enough to be accommodated within specification. The required resolution is obtained by using a 12-bit digital-to-analog converter (DAC). The table of attenuation versus 12-bit word settings is generated at power-on and whenever the temperature of the noise source has changed by more than a few degrees Celsius.

Reference Source

The reference source in the HP 3708A Test Set is designed to provide a highly stable 0-dBm sinusoidal tone at the front panel. Either of two frequencies (70 MHz and 140 MHz are standard) can be selected by operating a pushbutton. Primarily intended as a calibration source for the resident power meter, this output can also be used as a general-purpose reference and as a source of interference in the C/I (carrier/interferer) mode of the instrument.

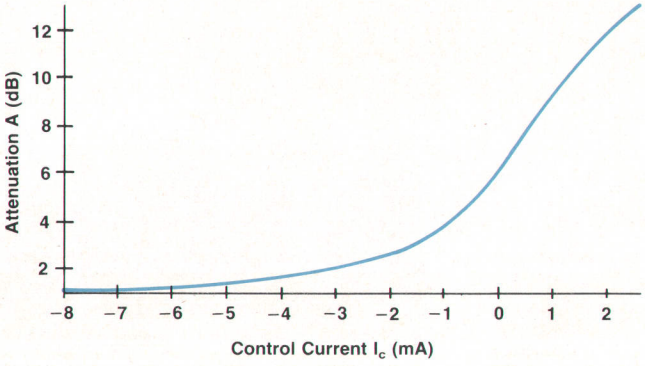

Fig. 4. *Plot of attenuation versus control current for equation 7 with a = 1.563, b = 1.31, and d = 0.8.*

General-Purpose Wideband Thick-Film Hybrid Amplifier

During the development of the HP 3708A's internal noise source it became obvious that a general-purpose amplifier could be designed for use in many sections of the instrument. The objective was to produce a 10-dB amplifier with a frequency response as flat as possible from 10 to 200 MHz, two independent outputs linear up to levels of +10 dBm, high gain stability, and high reverse isolation. The result is a hybrid amplifier that is used in 14 positions in the instrument. In addition, a second high-level hybrid and a discrete noise power amplifier use the same circuit configuration.

Choice of Circuit Configuration

The use of high-f_T transistors precluded any transformers in the feedback loop. In addition, experience has shown that at these frequencies it is inadvisable to include more than two stages within a feedback loop because of a tendency towards high-frequency instability at anything other than small loop gains. However, in general, for a given overall gain and a given number of stages, the sensitivity of a multistage feedback amplifier to changes in the active elements is reduced as the number of stages within each feedback loop is increased. Thus, a cascade of feedback pairs has a lower sensitivity than a cascade of single-stage feedback amplifiers.

In 1962, Cherry[1] showed that the sensitivity of a cascade of alternate series and shunt feedback stages is very nearly as small as that of a cascade of feedback pairs.

The alternate cascade approach is based on the introduction of a gross impedance mismatch between adjacent stages so that there is negligible interaction. Also each stage operates under the nearly ideal conditions for which its stable transfer function is defined, and the overall gain is approximately the multiplied individual stage transmittances. There is high reverse isolation; thus the use of cascaded single stages introduces a considerable amount of flexibility into the design. It was therefore decided to design a two-stage amplifier consisting of a series feedback stage followed by a shunt feedback stage. The high isolation between stages allows the input and output amplifiers to be independently optimized either manually or by CAD techniques, and the low output resistance of the shunt feedback stage is a convenient point to connect two isolated matched outputs.

Circuit Design

The design uses general-purpose transistors biased at a collector current corresponding to their maximum f_T of typically 5 GHz. A simplified circuit schematic is shown in Fig. 1.

The design was refined by CAD techniques to determine first-order dependence of circuit parameters on element values. As a starting point for optimization, some approximate low-frequency design equations were used.

The gain is 20 log $(0.5R_f/R_en)$ dB, where n is the interstage coupling efficiency (the input resistance of the shunt feedback stage is not zero and therefore a small portion of the first stage output current flows into the next stage's collector supply resistor). In practice, n is approximately 90%.

Signal current flowing in R_f reduces current available to the load and the value of R_f is a compromise between output loading, the required stage gain stability, and the output resistance. To a first-order approximation, output resistance = R_f/β.

The input data available for the CAD process includes the initial element values and the measured s-parameters for both transistor types. The s-parameters were measured on devices embedded in representative bias and collector supply networks.

Small variations in collector current cause variations in transistor gain of the order of 0.1 dB/mA. This becomes very significant when there are nine amplifiers cascaded, as in the HP 3708A noise source. Consequently, a special bias supply circuit is used to stabilize the collector currents.

The flexibility of the design approach is used to advantage in some positions in the instrument where 26-dB gain is obtained from two cascaded hybrids by effectively removing the 75Ω termination at the input to the second hybrid at all but gigahertz

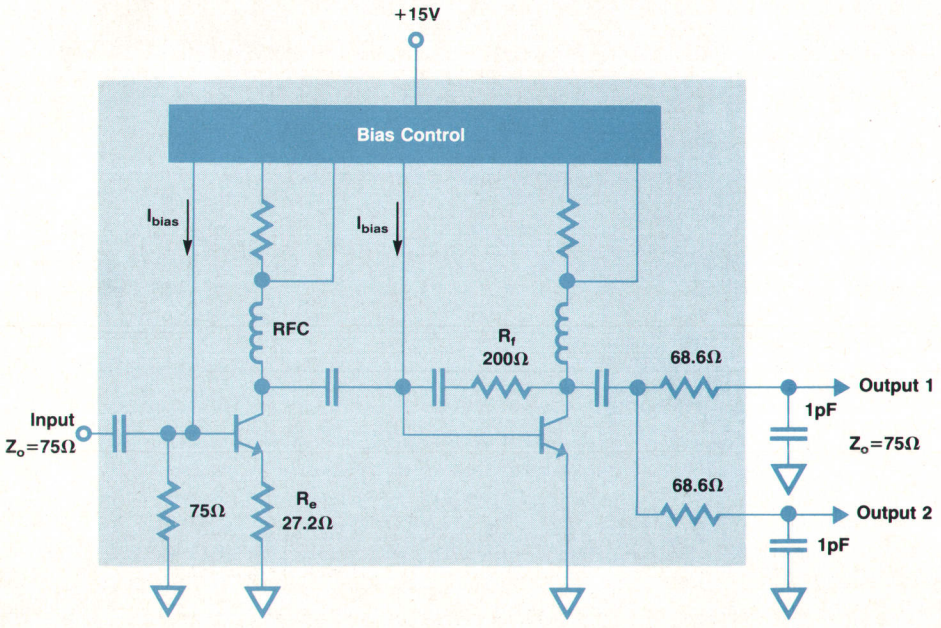

Fig. 1. *Schematic of wideband thick-film amplifier.*

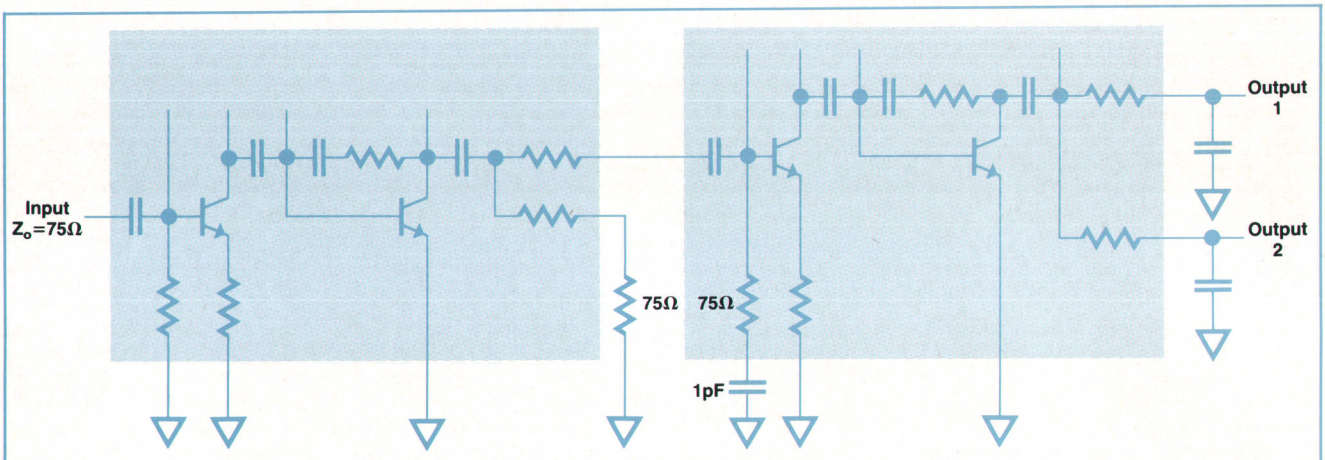

Fig. 2. *Connection of two hybrid circuit amplifiers in HP 3708A Test Set to obtain 26-dB gain.*

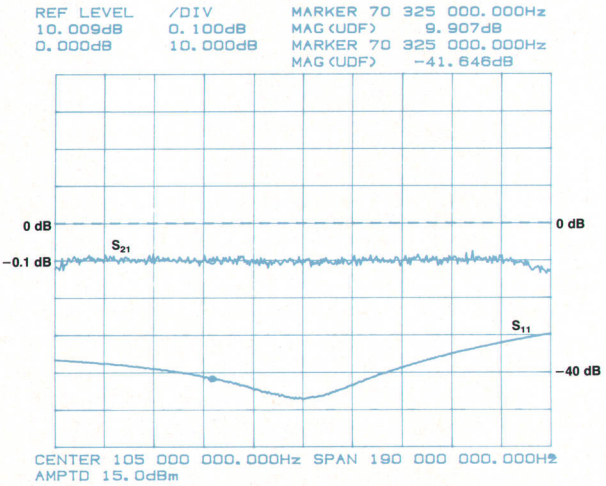

Fig. 3. *Amplitude response and input return loss versus frequency for wideband amplifier.*

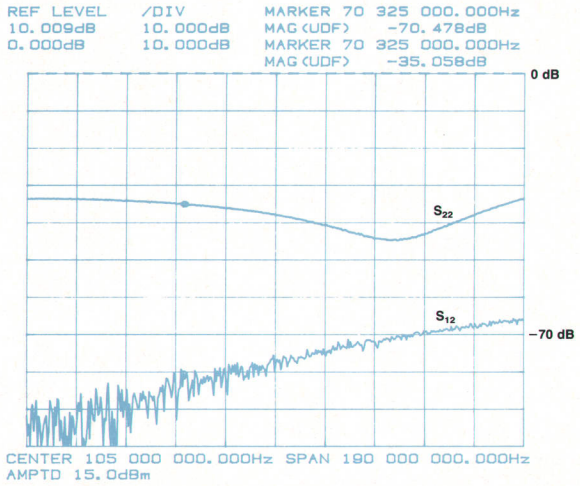

Fig. 4. *Output return loss and reverse transmission versus frequency for wideband amplifier.*

frequencies as shown in Fig. 2. In this application the margin for stability is increased by terminating the unused second output of the first hybrid with a 75Ω load.

Measured Performance

The amplifier forward gain changes by 0.04 dB at 200 MHz for an ambient temperature variation of 40°C. Results at 10 MHz are at least three times better.

The amplitude-versus-frequency response and the input return loss of the thick-film hybrid amplifier are shown in Fig. 3 at 0.1 dB and 10 dB per division, respectively, measured over a frequency range from 10 to 200 MHz. Fig. 4 shows the output return loss and reverse transmission at 10 dB per division over the same frequency range.

The input and output return losses are better than 30 dB in a 75Ω system. The intrinsic high reverse isolation is approximately 90 dB at 10 MHz and is still greater than 60 dB at 200 MHz.

Reference

1. E.M. Cherry, "An Engineering Approach to the Design of Transistor Feedback Amplifiers," *Journal of British Institute of Radio Engineers*, February 1963.

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Section Manager
Queensferry Telecommunications Division

The circuit (Fig. 5) is made up of two crystal-locked transistor oscillators, either of which can be switched into a level-stabilizing feedback loop. Hence, only one oscillator is active at any given time. The oscillators are based on a well-known common-base configuration.[3] However, they also incorporate a special pin diode negative feedback control circuit. A pin diode is placed in effect between the collector and base of each oscillator transistor and the dc-controllable RF resistance of these diodes is used to control the gain of the active oscillator.

Leveling Loop. The leveling loop operates in the following manner. The output of the active oscillator is connected to the input of a broadband (10 MHz to 200 MHz) RF amplifier by a pin diode switch. One output of this dual output amplifier is fed via an attenuator pad to the front panel while the other output is fed via a linear, passive

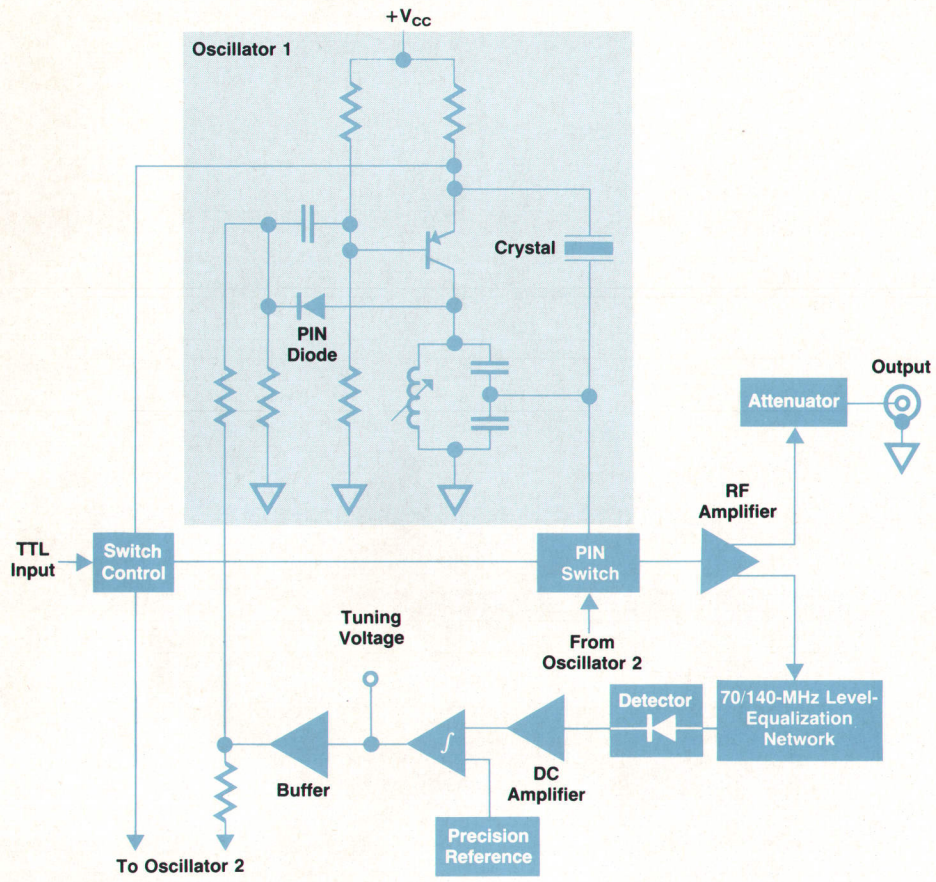

Fig. 5. *Circuit diagram of HP 3708A's internal reference source.*

RLC level-equalizing network to a Schottky-diode detector. Level equalization is necessary so that the output levels of the two oscillators at 70 MHz and 140 MHz are the same at the front panel. The dc voltage from the diode detector is amplified to a suitable level and compared with a reference voltage from a precision dc source. The resulting error voltage is amplified, integrated, and used to drive the pin diodes in both oscillators to close the loop and thus stabilize the output level of the reference source.

To enhance the level stability of this output, the detection circuitry is driven with the highest signal level that will not compromise the harmonic performance of the RF amplifier. The circuitry also includes temperature compensation and is isolated from the effects of small power supply variations.

An oscillator will only come to life if its loop gain is greater than unity. When the amplitude of the oscillation has built up to the required level, however, this loop gain must be reduced to unity. It is also necessary to restrict the crystal drive voltage so that the transistor is not driven into cut-off and the crystal power dissipation limit is not exceeded. The high accuracy required of the output level of the reference source precludes any significant harmonic content in this output, and the usual method of determining the level of an oscillator by amplitude limiting would require filtering. These problems are avoided in this circuit by adopting automatic gain control (i.e., the leveling loop).

At power-on, the feedback around the oscillator is automatically adjusted from a low value which ensures start-up to the precise value at which the loop gain is unity and the output is at the desired level. The spread and drift in device parameters are also automatically corrected. The crystal drive voltage is maintained at a known fixed value by the control loop to ensure that this voltage is not excessive. Since the oscillator is restricted to operating in its linear region, the harmonic content of the output is low and additional filtering is unnecessary.

Frequency Switching and Tuning. Ganged solid-state switching ensures that only one oscillator is active at any one time and that the oscillator outputs are isolated from each other. Either oscillator is switched off by forcing its transistor's base-emitter junction into a high impedance state while at the same time isolating its output by means of a pin diode switch.

The frequency of each oscillator is adjusted at the factory by monitoring a dc tuning voltage at the output of the integrator in the control loop (Fig. 5). This voltage is proportional to the dc current in the pin diode across the collector and base of the active oscillator transistor. The frequency of the oscillator is tuned by the variable inductor in its tank circuit until this voltage is at a minimum. At this frequency the negative feedback through the pin diode, and hence the positive feedback via the crystal, will be at a maximum. This implies that the impedance of the crystal is at a minimum and that it is operating at or very near its series resonance frequency. This tuning method chooses the optimum crystal frequency and minimizes the possibility of losing crystal lock because of environmental vari-

ations and aging. Therefore, the tolerance on the frequency of the oscillator is essentially determined by the tolerance on the frequency specification of the crystal.

Acknowledgments

The author wishes to acknowledge the contributions of several members of the design team. The thick-film hybrid amplifier (see box on page 33) used extensively in the noise generator and in the reference source was developed by Geoff Waters who also designed the output amplifier. David Stockton completed the design of the filter assembly. Harry Elder was responsible for the mechanical design. Brian Woodroffe wrote the operating software.

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Automated Radio Testing Shortens Test Time and Enhances Accuracy

by John A. Duff

WHEN TESTING the flat fade performance of a digital radio, a series of repetitive measurements have to be made to produce a complete curve (Fig. 1). If a typical characteristic plot consists of ten measured points (each averaged over three readings), the overall test would take about one hour. By using the HP 3708A Noise and Interference Test Set to vary the IF C/N level directly, this test time can be reduced to around 20 minutes while increasing the measurement accuracy and repeatability. If the HP 3708A is controlled remotely by computer via the HP-IB (IEEE 488/IEC 625), and the same is done with the bit error rate (BER) test sets to produce an integrated system, this time can be cut to around five minutes. When automatic graph plotting and results storage functions are provided, the savings in engineer time become even more substantial.

It is this automation of the fade measurement sequence that the HP 3708S Noise and Interference Measurement System addresses. This system consists of an HP 3708A, any HP bit-error-rate test set with HP-IB capability, and software written in HP Pascal and running on HP 9000 Series 200 and Series 300 Computers (see Fig. 2). The system offers comprehensive measurement support facilities in addition to performing the measurement sequence.

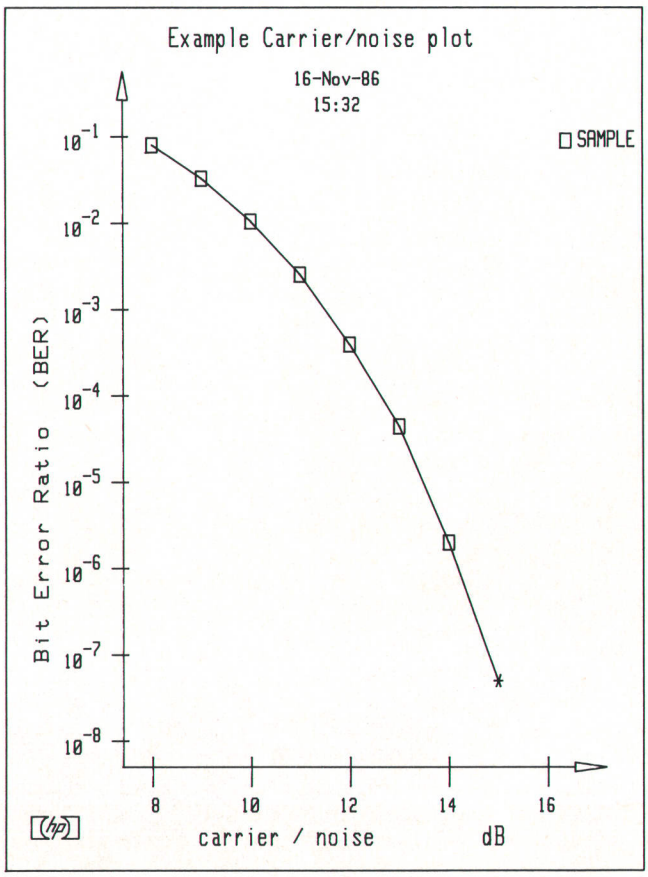

Fig. 1. *Flat fade performance curve for a typical digital radio obtained by automated testing.*

Interface Ergonomics

Simplicity of use was a prime requirement for the system; nonexpert production personnel should be able to perform measurements with the minimum of complication. At the same time the system should provide a comprehensive set of functions for an experienced design or test engineer.

To achieve this dual interface functionality, the system has a strict hierarchy of commands that allow access to the detailed features progressively, each command requiring only a single keystroke. To avoid complication, there are

never more than seven options at any command node in the system, and common functions are represented by the same key each time. Of course this interface method is neither novel nor unique, but in the HP 3708S it is complemented by displaying a tree of the command structure with the user's current position highlighted. This allows users to visualize their path through the system, avoiding the common problem of becoming lost in a maze of special function key definitions. Furthermore, the key required for a particular option corresponds to that option's position (as read from the left) in the following level on the tree. This can be seen in Fig. 3, where the command to enter the curve manager is 3.

System Localization

Readability and clarity were obviously important features for the system interface. To cope with the large amounts of information and data to be viewed and changed by a user, a general-purpose screen forms package (see box, page 38) was developed which is capable of reading predefined full-screen pages of text from files, displaying them, and reading and writing data to and from windows on them. Not only does this provide an easy-to-use user interface, it greatly simplifies the task of programming the various pages of text required and exchanging information with the user.

A secondary effect of this package, brought about by the ease of text manipulation within the system, led to an overall strategy of allowing full localization of the system text. That is, all the system screens, prompts, error messages, and even keystrokes can be changed without altering the program source code. This means text can be converted to other languages for support abroad, or customer-preferred formats can be accommodated.

Three separate files contain the localizable text: one for the screen display forms, one for help information (also stored as complete forms), and one for the user prompts, error messages, and key definitions. Each file is easily altered using the standard system editor and following simple design rules. Thus, no special-purpose builders or com-

Fig. 2. *HP 3708S Noise and Interference Measurement System.*

A Reusable Screen Forms Package

A common requirement for all software systems is a method for displaying full pages of text quickly and simply on the screen, and being able to put extra information and messages on the form or read data entered by a user from it. The Forms 200 package for the HP 3708S System enables pages of text to be read from files and displayed selectively. Both text and numbers can be written to or read from predefined windows (fields) in the forms.

Two types of form are available, a basic one for text display only (useful for giving standard information, such as in help facilities), and another more complex form with interactive data fields and display enhancements. The two sets of forms, named **HELP** and **SCREEN**, respectively (see Fig. 1), are held in separate ASCII text files for simple and easy update or relocalization.

The **HELP** forms file is opened each time a form is required, and searched until the required form is found by name. This reduces the amount of memory required for forms which are, by their nature, used infrequently. The **SCREEN** forms file, however, is opened once only during activation, and the forms set up in an internal data structure. This means that the more common forms, which have data windows and display enhancements, are set up in advance, ready for rapid display.

To make the forms as simple to change as possible, a what-you-see-is-what-you-get (WYSIWYG) approach is adopted. Each form contains the 24 lines of text as they are to be displayed, with the additional data fields of screen forms being specified by putting a field marker on the form at the start position required, followed by a row of an identifying character. These serve to give the field's length, but are not shown when the form is displayed. The type of field marker used determines which of the

```
@help_form
  This is the first line of form text, and appears at the top of the screen.

      The HELP forms file is opened and read each time a form is required,
                  and this form found by name (ie "help_form").


                                      No
                                     data
                                    fields
                                     are
                                  supported.


         HELP forms are designed for simple display of text information,
               such as pages of help information like this one.

            The form is displayed until a key is pressed by the user.

                        A maximum of 24 lines are allowed.
```

```
@screen_form  ,OVERLAY ,INHB,UNDL
  This is the first line of form text, and appears at the top of the screen.

     The SCREEN forms file is opened once only, and all the forms read and
   set up internally. Each form is then used by name (ie "screen_form" here).

     The data fields are specified as:

                        #aaaa      or      %bbbbbbbbb

     where field 'a' is five characters long and will display any data in
      half-bright inverse video (INHB specified in the form header above).
Field 'b' is ten characters long and displays data underlined (UNDL specified).

This form will be overlaid on top of the previous one (OVERLAY specified), and
we can let information (including data fields) from the previous form
'show through' this one by specifying a series of blank lines:
\
\
\

        All forms display and field control functions are performed by
                     high-level calls from the application.

                        A maximum of 24 lines are allowed.
```

Fig. 1. **HELP** *(top) and* **SCREEN** *(bottom) forms for HP 3708S software system.*

two available display modes the field is to use, each mode mapping to one of ten possible video highlights for that form. Successive **SCREEN** forms can also be overlaid on previous ones to allow a pseudowindowing feature. Finally, since no record is made of the contents of a field, any field can be used to read or write text and real or integer number types (unlike many other forms systems).

Besides its simplicity, the WYSIWYG approach has the advantage that, because the forms are read directly from text files and created by the standard editor, no special-purpose builder or compiler utilities are required to generate the forms. Once the form file has been edited, the application program can be simply rerun with no other intermediate steps necessary.

Integration into application programs is eased by a procedural interface to the subsystem, enabling all internal forms details and data to be hidden from the caller.

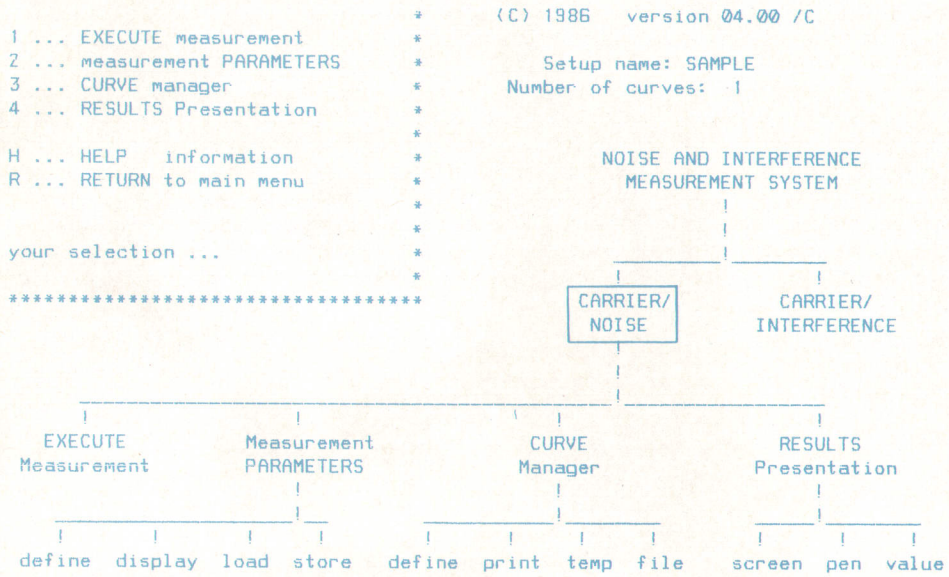

Fig. 3. *HP 3708S user menu. Here the number of the softkey label position from the left is used to select the next level of the command tree. For example, 3 selects the curve manager.*

pilers are required to produce the forms or language-dependent text.

Measurement Accuracy

To improve the HP 3708S fade simulation method further over the traditional technique other than simply automating the process, several features are included to enhance the measurement accuracy and repeatability. Each point on the fade characteristic is averaged over a user-programmable number of BER readings and the point is plotted as the arithmetic mean, with an error bar drawn between the upper and lower values measured.

A conventional BER measurement is made over a fixed-length gating period (e.g., 10 seconds), that is, a fixed-length window in which the error detector logs transmission errors. However, because of the random nature of error occurrences and hence their nonuniform distribution (Poisson) in time, a certain number of errors are normally required to assure a correct BER measurement. Put mathematically, for a truly random error process that is time invariant, a BER result based on N errors has a standard deviation of $100/\sqrt{N}$ percent. Hence, if 100 errors are counted, the calculated BER has a 63% probability of being within 10% of the long-term BER.

Consequently, any timed measurement gating period is a compromise between being short enough to produce a quick test, yet long enough to allow a minimum number of errors to be received at low error rates. The HP 3708S overcomes this by providing an adaptive-length gating period. The controller reads the error count from the BER detector and stops the period when the required number of errors have been received. This error limit is user-programmable.

Correct, calibrated operation of the HP 3708A depends upon the IF input to the instrument having little or no noise component, so that the signal-to-noise ratio at the injection point is determined only by the noise added by the instrument. However, most radios will have some noise that is intrinsic to the circuitry before the HP 3708A insertion point, and this could produce inaccurate values from the HP 3708A. A mathematical function is provided in the system to compensate for these errors by adjusting the values set up on the HP 3708A, given the intrinsic signal-to-noise ratio of the radio sections.

Acknowledgments

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