ROHDE&SCHWARZ

Manual

TEST RECEIVER

ESH3

335.8017.52
335.8017.56

Table of Contents

3. Maintenance

3.1 Measuring Instruments and Auxiliary Equipment Required

For the measuring instruments and auxiliary equipment required see Table 5-17 in the appendix.

3.2 Performance Check

The performance check must be made only after the functional check in accordance with section 2.2.4 has been carried out, to avoid carrying out a performance check on a faulty receiver.

3.2.1 Checking the Accuracy of the Level Measurement

The accuracy of the level measurement of the Test Receiver ESH 3 is determined by

- the accuracy of the calibration generator,
- the accuracy of the internal attenuator, and
- the accuracy of the A/D converter path.

The permissible resulting total error (assuming that an adequate signal-to-noise ratio is ensured) in average or peak value modes is ≤ 1 dB. For checking, set the measuring times to the standard values (0.1 s; 1 s) by means of the MEAS. TIME key 37.

3.2.1.1 Checking the Level Indication in the 20-dB Operating Range

a) Average value:

Settings on the ESH 3:

Operating range 33:	20 dB
Indicating mode 35:	AV.
IF attenuation 40, 41:	40 dB*
RF attenuation 40, 41:	50 dB
IF bandwidth 5:	500 Hz (model 52) < 1 kHz (model 56)
Calibrate receiver 15	

Apply sinewave signal of 78 dBµV ±0.1 dB in the frequency range from 10 kHz to 29.9999 MHz.

Nominal indication ..... 78.0 dBµV

Permissible error of level indication ..... ≤ 1 dB

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* The IF attenuation I = IF attenuation, R = RF attenuation and P_{lower} = lower level of operating range is derived from the formula $I/dB = P_{lower} + 30 - R$

b) Peak value:

Settings on the ESH 3:	Indicating mode 35:	PEAK
	IF attenuation 40, 41:	40 dB
	RF attenuation 40, 41:	10 dB
	IF bandwidth 5:	10 kHz
	Calibrate receiver (15)	

Apply pulse signal of 78 dBµV/MHz, pulse repetition frequency 100 Hz, to the RF input of the ESH 3 (45) (corresponds to a setting of 48 dB with the Schwarzbeck CISPR 2/4 standard pulse generator).

Nominal indication with $f_{in} > 1$ MHz ..... 38.0 dBµV

Permissible error of level indication ..... ≤ 2 dB

c) Pulse spectral density:

Settings on the ESH 3: Indicating mode 35: MIL

(All other settings same as under section 3.2.1.1b)

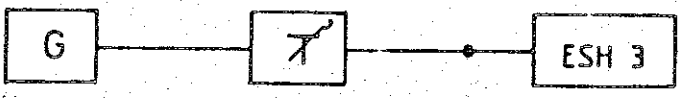
Nominal indication ..... 78.0 dBµV/MHz

Permissible reading error ..... ≤ 2 dB

d) Checking the scale accuracy and the analog level indication:

Settings on the ESH 3: Same as under section 3.2.1.1a

Test setup:



Reduce the level by 20 dB by switching the external attenuator in steps of 1 dB starting at full-scale analog indication.

Check the light dot of the analog level indication from maximum to minimum (left-hand scale end).

Check the scale accuracy:

Permissible scale error of 13

in upper half of operating range ..... ≤ 0.2 dB

in lower half of operating range ..... ≤ 0.3 dB

3.2.1.2 Checking the Level Indication in the 40-dB/60-dB Operating Level Range

a) Average value:

Settings on the ESH 3:	Indicating mode 35:	AV
	IF attenuation 40, 41:	40 dB
	RF attenuation 40, 41:	30 dB or 10 dB
	IF bandwidth 5:	500 Hz (model 52) 1 kHz (model 56)
	Calibrate receiver (15)	

Apply sinewave signal of 78 dBµV ±0.1 dB in the frequency range from 9 kHz to 29.9999 MHz.

Nominal indication ..... 78.0 dBµV
Permissible error of level indication ..... < 1 dB

b) Peak value:

Settings on the ESH 3:	Indicating mode 35:	PEAK
	IF attenuation 40, 41:	40 dB
	RF attenuation 40, 41:	10 dB
	IF bandwidth 5:	10 kHz
	Calibrate receiver (15)	

Apply pulse signal of 90 dBµV/MHz, pulse repetition frequency 100 Hz, from a standard pulse generator to the RF input 45 of the ESH 3 (corresponds to a setting of 60 dB with the Schwarzbeck-CISPR 2/4 standard pulse generator).

Nominal indication with f_{in} = 1 MHz ..... 50.0 dBµV
Permissible indicating error ..... < 2 dB

c) Pulse spectral density:

Settings on the ESH 3: Indicating mode 35: MIL
(All other settings same as under 3.2.1.2b)

Nominal indication ..... 90.0 dBµV/MHz
Permissible reading error ..... < 2 dB

d) Checking the scale accuracy and analog level indication:

Settings on the ESH 3: Same as under section 3.2.1.2a

Operating range 33: 40 dB or 60 dB

Reduce level by 40 or 60 dB by switching the external attenuator in 2-dB steps starting at full scale deflection of the analog level indication.

Check the light dot of the analog level indication from maximum to minimum (left-hand scale end).

Checking the scale accuracy:

Permissible scale error of 13 ..... < 1 dB

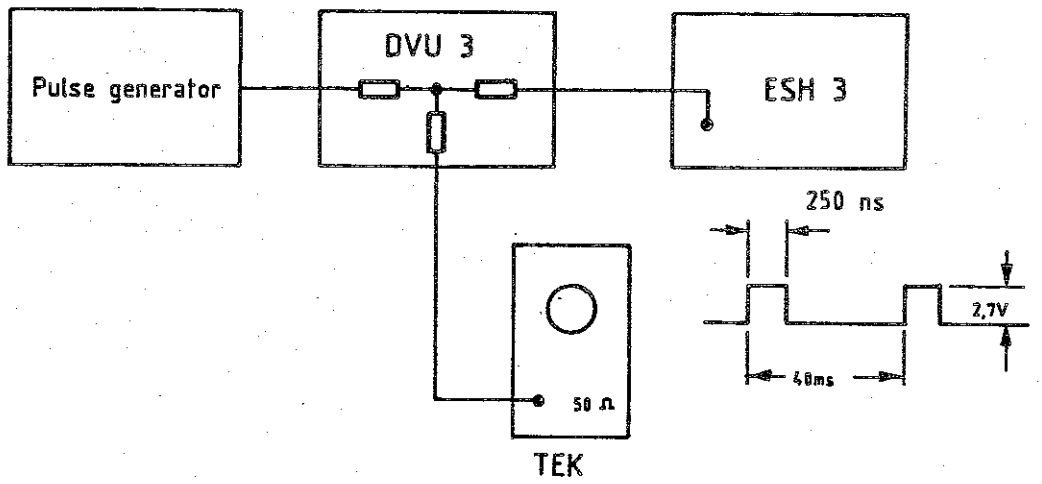
3.2.1.3 Checking the Level Indication in the CISPR (Publication 3) Mode of Indication

Settings on the ESH 3: Receive frequency: < 150 kHz

Indicating mode 35: CISPR

Attenuation 43, 42: AUTO, LOW NOISE

Test setup:



The pulse generator (pulse repetition frequency 25 Hz) supplies the standard pulse required in compliance with CISPR 3
(EMF 1.35 µVs = 5.4 V · 250 ns; Z_{out} = 50 Ω)

Nominal indication ..... 40.0 dBµV

Permissible reading error ..... ± 1 dB

When varying the pulse repetition frequency as shown in Fig. 5 - 9 the indication on the receiver must be within the tolerances specified.

3.2.1.4 Checking the Level Indication in the CISPR (Publication 1) Mode of Indication

Settings on the ESH 3: Receive frequency: > 150 kHz
Indicating mode 35: CISPR
Attenuation 43, 42: AUTO, LOW NOISE

Connect standard pulse generator which supplies a standard pulse with an EMF of 0.316 µVs (Z_{out} = 50 Ω) and a pulse repetition frequency of 100 Hz to the RF input 45 .

Nominal indication ..... 60.0 dBµV

Permissible reading error ..... ± 1 dB

NOTE:

When using the Schwarzbeck pulse generator IGU the following should be taken into consideration:

The IGU pulse generator supplies a pulse of 0.044 µVs (EMF) in compliance with CISPR 2/4. The difference between this pulse and the CISPR 1 pulse is -17.12 dB. The indication on the ESH 3 is, therefore, correspondingly less.

When varying the pulse repetition frequency as shown in Fig. 5 - 10 the indication on the receiver must be within the specified tolerances.

3.2.1.5 Checking the Generator Output

3.2.1.5.1 Checking the Generator Output in the TWOPORT Mode

Settings on the ESH 3: Mode of operation 38: TWOPORT

Connect the RF Insertion Unit URV-Z2 of the URV 4 to socket 44 and an RMC Termination to its output.

Nominal indication on the URV 4 ..... -27 dBm

Permissible deviation over entire receive frequency range ±0.3 dB

3.2.1.5.2 Checking the Generator Output in the REM. FREQ. Mode

Settings on the ESH 3: Operating mode 38: REM. FREQ.

Connect a counter with a sensitivity of < 10 mV to the generator output 44. Apply a signal of a known frequency, e.g. from a sound broadcasting station, to the RF input 45. The frequency read out on the counter must not vary when tuning the receiver between the -3-dB points of the IF pass band. Select the IF bandwidth to match the modulation and the channel spacing.

3.2.1.6 Checking the Attenuator

Settings on the ESH 3:	Indicating mode 35:	AV.
	Operating range 33:	20 dB
	IF attenuation 40, 41:	40 dB
	IF bandwidth 5:	500 Hz (model 52) 1 kHz (model 56)
	RF attenuation 40, 41:	90 dB
	Measuring time 37:	0.5 s

Same test setup as under section 3.2.1.1d)
Tune the signal generator (level 118 dBµV) to the receive frequency of the ESH 3. Set the attenuator to 0 dB. Set the level on the signal generator such that the indication on the ESH 3 is ..... 118.0 dBµV.
Increase the attenuation in steps of 10 dB and reduce the ESH 3-RF attenuation setting starting from 90 dB and check deviations from the rated indication.
Deviation ..... ≤ 0.4 dB

3.2.1.7 Checking the IF Level Switch

Same test setup as under section 3.2.1.1d)

Tune the signal generator to the exact receive frequency of the ESH 3 (level approx. 78 dBµV).

Settings on the ESH 3:	IF attenuation 40, 41:	40 dB
	RF attenuation 40, 41:	40 dB
	IF bandwidth 5:	200 Hz

Set the attenuator to 10 dB.

Set indication to ..... 68.0 dBµV

Reduce the IF attenuation of the ESH 3 in steps of 10 dB and increase the attenuator setting accordingly. Check deviation from the original indication.

Permissible deviation ..... ≤ 0.3 dB

3.2.2 Checking the Analog Readouts

3.2.2.1 Checking the Analog Level Indication

Settings on the ESH 3:	Indicating mode 35:	AV.
	Operating range 33:	20 dB
	IF bandwidth 5:	10 kHz
	IF attenuation 40, 41:	30 dB
	RF attenuation 40, 41:	10 dB
	Receive frequency:	1 MHz

Same test setup as under section 3.2.1.1d)

Tune the signal generator to the receive frequency of the ESH 3 (level 40 dBµV) and set the attenuator to 10 dB.

Check the LED light dot ..... right-hand scale end

Increase the attenuation to 20 dB.

Check the LED light dot ..... scale centre

Increase the attenuation to 30 dB.

Check the LED light dot ..... left-hand scale end

Increase the attenuation to 40 dB.

Check the LED light dot ..... MIN. LED lights

Set the attenuator to 0 dB.

Check the LED light dot ..... MAX. LED lights

3.2.2.2 Checking the Analog Frequency Offset Indication

Settings on the ESH 3: Same as under section 3.2.2.1

Calibrate receiver (15)

Check the light dot ..... scale centre, CENTRE LED lights

Tune signal generator to a frequency 5 kHz below the receive frequency.

Check the LED light dot ..... left-hand scale end

Tune the signal generator to a frequency 5 kHz above the receive frequency.

Check the LED light dot ..... right-hand scale end

3.2.3 Checking the Special Functions

3.2.3.1 Checking the Modulation Depth Measurements

Settings on the ESH 3:

Operating range 33:	20 dB
IF bandwidth 5:	10 kHz
IF attenuation 40, 41:	40 dB
RF attenuation 40, 41:	40 dB
Calibrate receiver (15)	
SPEC. FUNC. 11:	"10"

Apply signal to RF input 45 of the ESH 3 (frequency = $f_{ESH\,3}$, level = 68.0 dBµV, modulation depth 50%, f_{mod} = 1 kHz).

a) Modulation depth m: SPEC. FUNC. 11: "21"

Nominal indication ..... 50% m

Permissible deviation of the indication ..... ≦5 digits

b) Positive modulation peak m+: SPEC. FUNC. 11: "20", "23"

Nominal indication ..... 50% m+

Permissible deviation of the indication ..... ≦5 digits

c) Negative modulation peak m-: SPEC. FUNC. 11: "22", "25"

Nominal indication ..... 50% m-

Permissible deviation of the indication ..... ≦5 digits

3.2.3.2 Checking the Frequency Offset Measurement

Settings on the ESH 3: Attenuation 43, 42: AUTO, LOW NOISE

Operating range 33: 60 dB

All other settings same as under section 3.2.3.1

Calibrate receiver (15)

SPEC. FUNC. 11: "10", "31"

Apply unmodulated signal (frequency = $f_{ESH\,3}$, level = 40 dBµV) to the RF input (45) of the ESH 3.

Nominal indication ..... 0.00 kHz

Permissible reading error ..... ≦ 0.1 kHz

Increase frequency of input signal to $f_{ESH\,3}$ + 3 kHz.

Nominal indication ..... 3.00 kHz

Permissible reading error ..... ≦10%

Reduce frequency of input signal to $f_{ESH\,3}$ - 3 kHz.

Nominal indication ..... -3.00 kHz

Permissible reading error ..... ≦10%

3.2.3.3 Checking the Deviation Measurements

Settings on the ESH 3:

Attenuation 43, 42:	AUTO, LOW NOISE
Operating range 33:	60 dB
IF bandwidth 5:	10 kHz
Calibrate receiver (15)	
SPEC. FUNC. 11:	"10"

Apply signal to RF input of the ESH 3 45 (frequency = $f_{ESH\ 3}$, level = 40 dBµV, frequency deviation 3 kHz and f_{mod} = 400 Hz).

a) Frequency deviation: SPEC. FUNC. 11 "41"
   Nominal indication ..... 3.00 kHz
   Permissible deviation of the indication ..... ≤ 10%

b) Positive peak deviation: SPEC. FUNC. 11: "40", "43"
   Nominal indication ..... 3.00 kHz
   Permissible deviation of the indication ..... ≤ 0.4 kHz

c) Negative peak deviation: SPEC. FUNC. 11: "42", "45"
   Nominal indication ..... 3.00 kHz
   Permissible deviation of the indication ..... ≤ 10%

d) Subsequently set SPEC. FUNC. to ØØ

3.2.4 Checking the Frequency Accuracy

Settings on the ESH 3:

Receiver frequency:	29.9999 MHz
Operating mode 38:	TWOPORT

Connect frequency counter with an accuracy of 1×10^{-7} and a sensitivity of < 10 mV to the generator output 44 of the ESH 3.

Permissible frequency error ..... < 500 Hz

3.2.5 Checking the IF Bandwidths

Settings on the ESH 3:	Operating range 33:	20 dB
	Indicating mode 35:	AV.
	IF attenuation 40, 41:	40 dB
	RF attenuation 40, 41:	10 dB
	Operating mode 32:	GEN, OFF

Adjust level of generator signal (frequency = f_{ESH3}) applied to the receiver RF input 45 until the level indication is exactly 40.0 dBµV (maximum analog level indication). For each of the four bandwidths provided, detune the signal generator towards lower and then towards higher frequencies until the level indication decreases by 3 and 6 dB. The -3 dB and -6 dB IF bandwidths are given by the difference between the upper and the lower tuning frequency at which these level drops occur.
Tolerances for the various bandwidths are contained in the specifications.

3.2.6 Checking the Noise Figure

Settings on the ESH 3:	Operating range 33:	20 dB
	Indicating mode 35:	AV.
	IF bandwidth 5:	10 kHz
	RF attenuation 40, 41:	0 dB
	IF attenuation 40, 41:	10 dB

Connect noise generator to the RF input 45 of the ESH 3.

Read off level indication.

Increase level of the noise generator until the level indication increases by 3 dB.

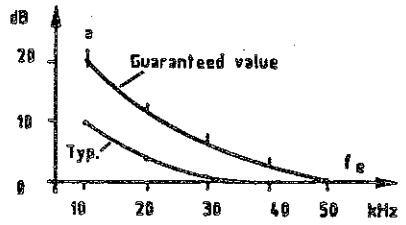
Due to the special calibration of the noise generator it now reads the noise figure directly in dB. If f > 50 kHz, the noise figure is as follows:

At IF bandwidths 10 kHz/2.4 kHz/200 Hz ..... typ. < 14 dB,
at IF bandwidths 500 Hz (model 52) ..... typ. < 16 dB.

If f_{in} > 50 kHz, the noise indication on the ESH 3 is as follows:

Average value	(B = 200 Hz)	.....	typ. -30 dBµV
Peak value	(B = 200 Hz)	.....	typ. -22 dBµV
CISPR 1	(B = 1Ø kHz)	.....	typ. -6 dBµV
CISPR 3	(B = 200 Hz)	.....	typ. -28 dBµV
Pulse spectral density (MIL)	(B = 10 kHz)	.....	typ. 38 dBµV/MHz

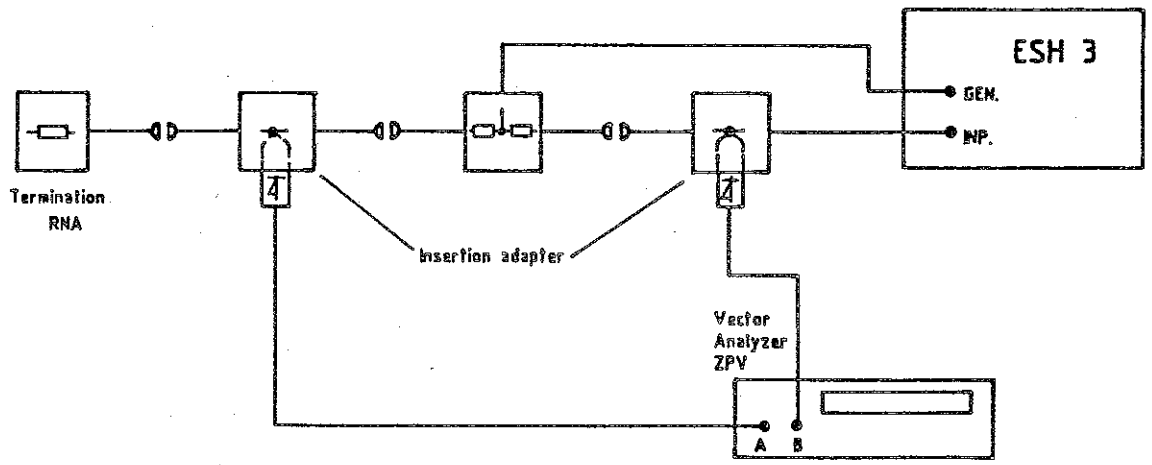
If f_{in} < 50 kHz (B = 200 Hz) (model 52), the noise indication increases as shown in the diagram below.



There is no noise increase for model 56.

3.2.7 Checking the Input Reflection Coefficient

Test setup:



The reflection-coefficient indicator, such as the ZPV, operates at the frequency to which the receiver is tuned.

RF attenuation: 0 dB ..... r < 33% (= VSWR < 2)

> 0 dB ..... r < 10% (= VSWR < 1.2)

3.2.8 Checking the Oscillator Reradiation at the RF Input

Settings on the ESH 3: RF attenuation 40, 41 : 0 dB

Connect a sensitive selective voltmeter (e.g. wave analyzer) to the RF input 45 of the ESH 3. The receive frequency of this meter must be $f_{ESH\,3}$ + 75.000 MHz.

Level indication ..... ≦ 0 dBµV

3.2.9 Checking the 75-MHz IF Rejection

Settings on the ESH 3:

Operating range 33 :	20 dB
IF bandwidth 5 :	200 Hz
Indicating mode 35 :	AV.
IF attenuation 40, 41 :	0 dB
RF attenuation 40, 41 :	0 dB

Apply signal (frequency = 75.000 MHz, level = +70 dBµV) to the RF input 45 of the ESH 3 and check all tuning frequencies of the ESH 3.

Permissible increase in the noise indication ..... ≦ 3 dB.

3.2.10 Checking the Image Frequency Rejection

Same settings on the ESH 3 as under section 3.2.9.

Apply signal (frequency = $f_{ESH\,3}$ + 150.000 MHz, level = +70 dBµV) to the RF input 45 of the ESH 3 and check all tuning frequencies of the ESH 3.

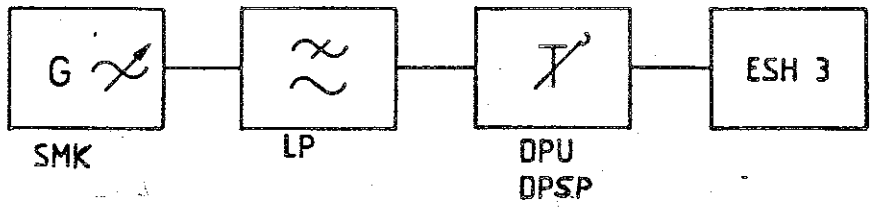
Permissible increase in the noise indication ..... ≦ 3 dB.

3.2.11 2nd Order Harmonic Distortion (a_{K2})

Apply signal of low harmonic content (frequency f_1) to the RF input 45. Due to the non-linearity of the input mixer, for example, a signal $f_2 = 2 \cdot f_1$ is obtained. Measure the level of this signal and compare it with the wanted signal level. There is a square-law relationship between the level of the spurious product and the wanted signal level. This means that when the input level is increased by n dB the spurious product increases by 2 · n dB and the level difference between the two signals decreases by n dB.

The requirements placed on the test assembly for measuring harmonic distortion and intermodulation rejection are very exacting since the Receiver ESH 3 features excellent characteristics.

Test setup:



The attenuation of the low-pass filter, LP, should be > 60 dB at the 2nd harmonic of the generator signal and the harmonic distortion of the signal generator should be down > 35 dB.

Calculation of the harmonic distortion and the 2nd-order intercept point K2:

Input signal to the receiver: level l_1 / dBµV
frequency f_1

Resulting unwanted signal: level l_2 / dBµV, frequency f_2

Harmonic distortion a_{K2} / dB = down $l_1 - l_2$ at a level of l_1 / dBµV

Intercept point K2: K2 intercept / dBm = $l_1^+ + a_{K2}$ where
$l_1^+ = l_1$ converted into dBm, i.e.
$l_1^+ = l_1$ / dBµV - 107 dB

Measurement:

Settings on the ESH 3: Indicating mode 35: AV
IF bandwidth 5: 200 Hz
RF attenuation 40, 41: 0 dB

For level and frequency see "Specifications".

3.2.12 2nd and 3rd Order Intermodulation Rejection

Apply two signals of low harmonic content at frequencies f_1 and f_2 to the input of the receiver. Due to the non-linearity of the input mixer signals of the

2nd order: $f_3 = f_1 + f_2$, $f_4 = f_2 - f_1$ and

3rd order: $f_5 = 2f_2 - f_1$, $f_6 = 2f_1 - f_2$

are produced.

Measure the level of the signals f_4, f_5 and f_6. The averaged level difference between f_1, f_2 and f_3, f_4 determines the 2nd order intermodulation rejection (a_{D2}) and that between f_1, f_2 and f_5, f_6 determines the 3rd order intermodulation rejection (a_{D3}). The minimum frequency spacing between the two signals f_1, f_2 must be > 40 kHz. Very exacting requirements are placed on the test assembly for measuring the 2nd and 3rd order intermodulation rejection since the Receiver ESH 3 features excellent characteristics.

Calculation of the intermodulation rejection and the respective intercept points:

Input signals: level l_1 / dBµV, frequency f_1

level $l_2 = l_1$, frequency f_2

Resulting 2nd order IM products: level l_3 / dBµV, frequency $f_3 = f_1 + f_2$

level l_4 / dBµV, frequency $f_4 = f_2 - f_1$

2nd order intermodulation rejection a_{D2} / dB = $l_1 - \frac{l_3 + l_4}{2}$ at a level of l_1 / dBµV

Intercept point D2: D2 intercept / dBm = l_1 / dBm + a_{D2}

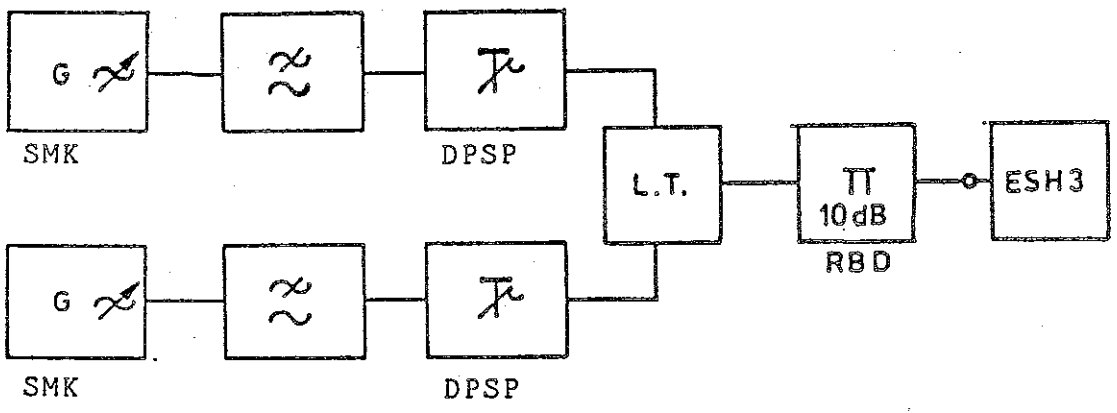
Resulting 3rd order IM products: level 15 / dBµV, frequency $f_5 = 2f_2 - f_1$

level 16 / dBµV, frequency $f_6 = 2f_1 - f_2$

3rd order intermodulation rejection a_{D3} / dB = $l_1 - \frac{l_5 + l_6}{2}$ at a level of l_1 / dBµV

Intercept point D3: D3 intercept point / dBm = l_1 / dBm + $\frac{a_{D3}}{2}$

Test setup:



Both signal generators are set to maximum output. The attenuation of the low-pass filters must be > 60 dB at twice the wanted signal.

Measurement:

Settings of the ESH 3:	Indicating mode 35:	AV.
	IF bandwidth 5:	200 Hz
	RF attenuation 40, 41:	0 dB

For level and frequency see "Specifications".

3.2.13 Checking the Crossmodulation

For test setup, see 3.2.12.

Connect a spectrum analyzer to the IF output (30 kHz) of the ESH 3.

A spurious signal of 36 dB at a frequency spaced 1 kHz away corresponds to a crossmodulation content of 3%. This signal must, however, be a discrete line and should not be caused by the sideband noise of one of the oscillators involved.

Measurement:

Setting on the ESH 3:	RF attenuation 40, 41:	0 dB
	IF attenuation 40, 41:	30 dB
	IF bandwidth 5 :	10 kHz
	Operating range 33:	20 dB

Set transmitter 1 to receive frequency

Level ..... 20 dBµV

Set transmitter 2 (AM-modulated, m = 30%, f = 1 kHz)

to a frequency at a spacing > 100 kHz from f_{rec}

Level ..... 100 dBµV

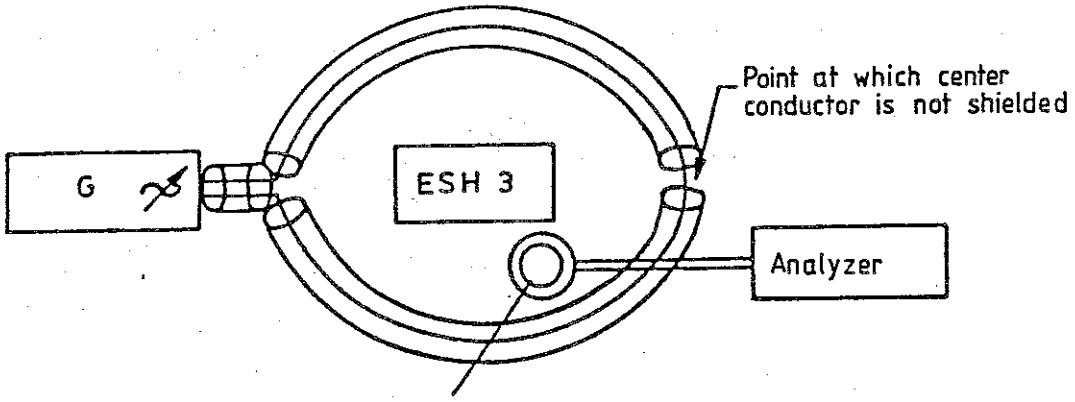
The spurious modulation on the receive frequency is ..... < 3%

(this corresponds to a 1-kHz spurious signal of ..... > 36 dB).

3.2.14 Checking the RF Leakage

Place the Test Receiver ESH 3 in a 10-turn toroidal coil (frequency range < 150 kHz) or a single-turn coil (frequency range > 150 kHz).
Connect the toroidal coil to a signal generator, the level of which is adjusted such that a field strength of 10 V/m is obtained (measured with inductive probe).

Test setup:



Inductive Probe HFH 2-Z4

Level required at the analyzer due to the conversion

factor of the probe ..... 1 mV ±6 dB corresponding to -47 dBm ±6 dB

The toroidal coil (1 turn or 10 turns) is shielded.

There is a gap in the shield at one place, to prevent a shorted turn.

3.2.15 Checking the Outputs

3.2.15.1 30-kHz IF Output

Apply signal corresponding to the upper end of the selected operating range (full-scale analog level indication) and measure at the BNC socket 48 via a high impedance (>> 1 kΩ).

Voltage ..... 2 V

Permissible error ..... ±2 dB

3.2.15.2 75-MHz IF Output

Settings on the ESH 3: RF attenuation 40, 41 : 0 dB

Frequency : > 1 MHz

Change a connection on the Mixers 1 and 2 board (Y9) to activate the amplifier.

Connect RF input 45 to generator output 44.

Select TWOPORT mode by means of key 38 and measure the output level at BNC socket 49 .

Output level ..... 30 mV

Permissible error ..... ±3 dB

3.2.15.3 AM Demodulator Output

Apply signal of 50% modulation depth (modulation sidebands are within the IF passband) to RF input 45 and measure at BNC socket 50 via a high impedance (>> 10 kΩ).

V_{pp} ..... 0.5 V

Permissible error ..... ±3 dB

3.2.15.4 FM Demodulator Output

Apply signal of exactly known frequency to RF input 45 of the ESH 3. Tune the test receiver to this frequency and measure at FM demodulator output 51:

Voltage ..... 0 V

Permissible error ..... ±25 mV

When tuning the receiver to higher frequencies the voltage should increase by 10 mV with every 100-Hz step. Conversely, when tuning the receiver to lower frequencies the voltage should decrease by 10 mV with every 100-Hz step.

Detune the receiver by 5 kHz and measure voltage at BNC socket 51:

Voltage ..... 0.5 V

Permissible error ..... ±50 mV

3.2.15.5 Level Output AV./PEAK

Settings on the ESH 3: Indicating mode 35: AV. or
PEAK or
MIL

Apply signal corresponding to upper end of operating range (full-scale analog level indication) to RF input 45 of the ESH 3. Measure output voltage at BNC socket 53 via a high impedance (>> 10 kΩ):

Voltage ..... 5 V

Permissible error ..... ±75 mV

With CISPR indicating mode:

Voltage ..... 2 V

Permissible error ..... ± 75 mV

3.2.15.6 Level Output CISPR

Same as under 3.2.15.5.

This output (BNC socket 52) includes a low-pass network for simulation of moving-coil-meter response according to CISPR Publ. 1 and 3.

3.2.15.7 Frequency Offset Output

Same as under 3.2.15.6, but voltage higher by a factor of 10 (BNC socket 54).

3.2.16 Check of Operation Using External Reference

Settings on the ESH 3:

Left-hand switch 55 down: external reference

Right-hand switch 55 down/up: 5 MHz / 10 MHz

Apply external standard frequency of 5 or 10 MHz to BNC socket 55 on the rear panel of the receiver. Carry out performance check in accordance with section 2.2.3.

3.2.17 Checking the Recorder Output

Setting on the ESH 3: Scan 25: ON

a) Call up MIN. LEVEL 27 for recorder calibration
and measure output voltage at pins 3 and 4 of socket 58:

Voltage	0 V
Permissible deviation	+0.1 V

b) Call up MAX. LEVEL 26 for recorder calibration
and measure output voltage at pins 3 and 4 of socket 58:

Voltage	+10 V
Permissible deviation	≦ 5%

3.2.18 Checking the IEC-bus Output

- Connect an IEC-bus controller, such as the PCA to the IEC-bus input 57.
  Check all device functions using setting instructions in accordance with section 2.3.21.
  Check the indication of the Remote state, and function of LOCAL key 24.

- Select Talk Only mode by means of switch 56 and connect printer in Listen Only mode to the IEC-bus socket 57.
  Switch on all the test routines by means of the SPEC. FUNC. key 12 ("21", "31", ..., "81").
  Press TALK key 19 to initiate and check data output on printer.

3.3 Electrical Maintenance

Owing to its design the ESH 3 requires very little electrical maintenance:

- Check frequency accuracy (see section 5.3.1.4.2) and readjust reference oscillator once every year.
- Check the calibration level (see section 5.3.10.2) once every year.
- Check NiCd battery BA1 on the computer board Y2 (voltage: 3.6 V) every six months.

3.4 Mechanical Maintenance

The ESH 3 uses a minimum of moving parts. It therefore requires only very little mechanical maintenance. However, frequent use of the ESH 3 in vehicles will make mechanical maintenance necessary more often than if the unit is used only in the lab.

The following maintenance work should be carried out:

- Clean front panel with a soft cloth dipped in alcohol.
- Check that all cable and plug-and-socket connections as well as screws are tightened down properly.

3.5 Storage

The Test Receiver ESH 3 can be stored over an extended period of time at temperatures between -25°C and +70°C. At high temperatures and high relative humidity, seal the receiver with plastic material or waxed paper to minimize any ill effects.

After the receiver has been stored for some time at high relative humidity proceed as follows:

- Unscrew the external top and bottom covers.
- Unscrew the internal top and bottom covers.
- Allow the receiver to dry for a period of 4 to 6 hours at a temperature of between +40 and 45° C.
- Carry out performance check in accordance with section 2.2.3.

4. Circuit Description

4.1 Electrical Function of the Individual Boards

(See block diagram 335.8017 FS as well as overall circuit diagram 303.8017 S sheets 1 and 2)

The RF Test Receiver ESH 3 is a triple heterodyne receiver covering the receiving range from 9 kHz to 30 MHz with 16 subranges set by internally switched filters arranged before the 1st mixer stage. The 1st IF is 75 MHz, the 2nd IF 9 MHz and the 3rd IF 30 kHz. The front panel and the Display (Y1) + Computer (Y2) boards form a mechanical unit. The Synthesizer 1 (Y5) and Synthesizer 2 (Y4) boards produce the required mixer frequencies and determine the receive frequency. From this receive frequency, which is read out on the front panel, the logic switching signals for the 16 different RF filters on the Filter 1 (Y7) and Filter 2 (Y8) boards are produced by the Filter Control (Y6) board. In the Mixers 1 and 2 (Y9) board, the filtered input signal is converted to the 1st and the 2nd IF and passed through IF filters. Conversion to the 3rd IF is accomplished on the Mixer 3 (Y11) board. The indicating range of the receiver is adjusted to the level of the signal to be measured in steps of IF attenuation in Mixer 3 (Y11) and by means of the RF Attenuator (Y16) which is driven from the Attenuator Control (Y13). The Indication and AF Demodulation (Y12) board demodulates the 3rd IF signal and produces a DC voltage proportional to the signal level. For calibration of the receiver, the Calibration Generator (Y10) is provided producing a calibration signal at the receive frequency from the 3rd IF and the various oscillator signals.

The Motherboard is used on the one hand to provide the electrical interconnection between the boards and on the other hand the mechanical support for the boards.

The +5-V supply for the subassemblies Synthesizer 1 and Synthesizer 2 is derived from the +12-V line by means of a voltage regulator.

4.1.1 Display Unit (Y1)

(See circuit diagram 335.8400)

In addition to the keys for operation and setup of the receiver and the associated LEDs for indication of the current device function, the following facilities are provided on the Display Unit:

- 13-digit alphanumeric indication for output of the measured data, entry and output of setting data and output of error messages (13)
- 6-digit display of current receiver frequency (20)

- 3-digit 7-segment displays for readout of the selected RF attenuation (8) and indication of beginning, centre and end of the demodulator operating range (14)
- Analog level indication over selected operating range (14)
- Analog indication of frequency offset of input signal from the receiver centre frequency
- Differential current sink for the suppression of supply voltage disturbances due to heavy load fluctuations.

The alphanumeric indication for output of the measured data and entry and output of setting data consists of 13 5x7 dot-matrix displays which are driven in columns in multiplex operation. For this purpose, the single-chip microprocessor B67 is used which is connected to the main processor via the FIFO store interface B54-B55. The data transfer is interrupt controlled and is accomplished by asynchronously entering and outputting ASCII character strings into and from the first-in-first-out stack store.

The slave processor decodes the ASCII characters against a reference table into the five information columns for the LED dot-matrix displays which are successively loaded into the 13 8-bit latches (B25 to B37) by multiplex clock control of the internal timer of the processor and displayed by triggering the respective transistors T1 to T5. A separate clock cycle drives the decimal points via T6.

In addition to the alphanumeric indication, the microprocessor controls the LEDs for the indication of the selected device functions GL1 to GL37 via the I/O expander ICs B57 to B59. The internal processor software also comprises blinking routines for individual LEDs and for the complete alphanumeric display to identify operator errors and overload of the test receiver.

The 6-digit display of the current receiver frequency (in MHz with fixed decimal point) is obtained by means of the LED ICs B18 to B23. They include latches and decoders as well as integrated current sources for the LEDs. The frequency information is transferred from the output ports of the Computer board via ST1 to the Display Unit.

With the exception of S46 (Local), all the keys are connected to the keyboard and display IC B61 via the demultiplexer B62. The keyboard IC is directly connected via the data and system bus and ST2 to the main processor on the computer board. For certain keys (S8, S16, S19 to S21) automatic key

repetition is provided by the ICs B41 to B45 permitting pulses for the keyboard IC to be obtained at time intervals of first 600 ms, then 300 ms and finally every 150 ms if the key is held down.

The 3-digit 7-segment displays for readout of the selected RF attenuation and indication of the beginning, centre and end of the demodulator operating range (B1, B2 to B4) are also driven and multiplexed by the keyboard and display IC via the demultiplexer B63 and the driver transistors T7 to T13.

The analog frequency offset display consists of 16 LEDs which are driven from the IC B66. The analog level indication consists of 31 LEDs which are driven from B64 and B65. The analog voltage for both displays is taken from the Analog board to the Display Unit via the Computer board (ST1 and ST2). Going outside either end of the operating range and centre tuning are indicated separately via the individual LEDs GL38, GL39 and GL88.

The differential current sink B71-B72 controls the shunt transistor T16 which via R87 levels out load fluctuations caused by multiplexing and the changing indications, thus suppressing interference on the 5-V supply line of the test receiver.

4.1.2 Computer Board (Y2)

(See circuit diagram 335.8800 S)

The microprocessor B2 on the Computer board is the heart of the digital control circuit of the Test Receiver ESH 3. The data bus, the address bus and the control lines of the processor are buffered via the driver ICs B1, B3 and B6. The Reset input is directly connected to the +5-V voltage monitor of the analog power supply to ensure a defined start of the program run when switching on the receiver.

Since the lower addresses are multiplexed with the data bus in the 8085 processor, the octal latch B5 is used as an intermediate address memory. The program memory consists of four 4-kbyte EPROMs and additional memory chips on the Memory board which is connected to the Computer board via BU4 and ST3. The entire lower 32-kbyte address area is reserved for the resident program range. Address decoding takes place via B4 in 4-kbyte steps.

The upper 32-kbyte address space serves for controlling the peripherals, the I/O ports and the RAM. Address decoding takes place via B7. For the I/O ports the decoders B23 to B25 are also used, in conjunction with the I-O/M control line of the processor.

The RAM capacity is provided by a 512-byte CMOS memory (B9-B10-B12-B13) which is powered from the NiCd battery BA1 while the receiver is switched off to safeguard the data. Moreover, a 256-byte volatile working memory is provided on the peripheral chip B30 which can be used for the stack area and for intermediate and auxiliary variables.

The complex peripheral chip B17 connects the microprocessor data bus to the IEC-625 interface located on the rear panel of the test receiver. Data transfer in both directions is interrupt controlled and takes place via the 16 internal write and read registers of the IEC-bus IC. The eight data lines, five control lines and three handshake lines are terminated in accordance with the standard by the special drivers B18 to B21 which are connected via BU8 to the chart recorder control circuit and via the rear panel socket to the IEC bus.

The IEC-bus address plus the code for the chart recorder, if used, is read in via BU7 and input port B46 when switching on the receiver and acknowledges through output port B45. A change in the input data is recognized by the 8-bit comparator B49 and converted into an interrupt request which is sent to the processor. The processor, in turn, reads in the new information, processes it and returns it via the output port. The same principle is used to process the test antenna/probe code and applicable conversion factor at the antenna supply socket 47 via ST12 and recognize a change, if any (B47, B48 and B50).

The priority encoder B82 and the 8-bit register B31 handle the interrupt requests and the hardware side of generating the required start addresses RST1 to RST7. Some interrupt lines are gated with the output port B80 via a logic AND function so that these interrupts can be disabled during certain software routines by using a suitable bit pattern.

On account of their high priority, overload indication from the mixers, the monitoring circuits of the oscillator and synthesizer loops and the quasi-continuous tuning control signal are applied to the separate interrupt inputs RST5.5 to RST7.5 of the microprocessor. The signals from the monitoring circuits can be read in at the input port B54 and the signals from the comparators for the power supply voltages in the analog power supply ST9 can be read in at the input port B53.

The line from the STOP key 28 is brought out separately as is that from the LOCAL key 24 which is not connected to the keyboard unit of the front panel; they are debounced and taken via the flip-flop B55 to the input port B81.

Quasi-continuous tuning of the Test Receiver ESH 3 is effected via the tuning sequencer 568.7811 whose output signals are routed via ST 11. The pulses of the Hall sensors of the tuning sequencer are conditioned by B64, B66 providing the CLOCK and UP/DOWN signals for the binary counters 357 and 358.

The current count can be polled by the microprocessor via the input port B56. Every first count pulse arriving after a readout operation of the processor triggers the monostable B71, which produces an interrupt request via the flip-flop B65 with a delay of about 50 ms. This prevents continual, unnecessary interrupting of the main program during fast tuning.

The output ports B33 to B35 are used for outputting the current receiver frequency to the front panel display and to the two synthesizers. The remaining logic signals for setting the RF circuitry are produced at the output ports B36 to B38 and B51 and B52.

In addition, two D/A converters, which furnish the analog output values for driving a YT, XY or radiomonitoring receiver, are provided on the computer board. The receive frequency is taken via output ports B43 and B44 to the 10-bit D/A converter B40, whose analog output is buffered by the operational amplifier B41. The Y analog voltage for level indication is produced by the 8-bit D/A converter B39, which obtains its input information from output port B42. It is also buffered via an operational amplifier. The logic signals for recorder control (pen lift, format advance) from port B44, and the two analog voltages, are taken via BU7 to the recorder control output on the rear panel of the receiver. The ground of the D/A converters and the ground of the A/D converter circuit are run separately from the general digital ground to avoid interference on these lines.

The A/D converter circuit consists of the sample/hold amplifier B77, the A/D converter proper B26 and the peripheral chip B30, whose port lines are used for reading in the converted analog voltage and driving the converter ICs. The +5-V reference voltage is obtained from the high-accuracy +10-V supply

via the op-amp B22 and T1. The divider chain B27 and B28 produces the 250-kHz clock frequency necessary for the 10-bit A/D converter. The flip-flops B29 ensure synchronization of the start/stop signals with the clock frequency.

The data bus of the microprocessor and the control lines are taken to the front panel via BU2, where they are connected to the slave processor for controlling the alphanumeric readout and to the keyboard and display IC for scanning the keys.

4.1.3 Analog Circuit (Y3)

(See circuit diagram 336.0710 S)

4.1.3.1 General

The Analog circuit is used to select the various demodulated voltages to match the output levels and the level to the A/D converter as well as for evaluation of the various signals (e.g. logarithmization, frequency deviation and modulation depth measurement, control of analog level and offset indication).

All circuit paths are controlled via CMOS switches. Except for a few gate circuits (which can be readily seen in the circuit diagram), the µP system of the ESH 3 handles the control of the circuit via output ports; i.e. gating required for the various measurement routines is accomplished via software.

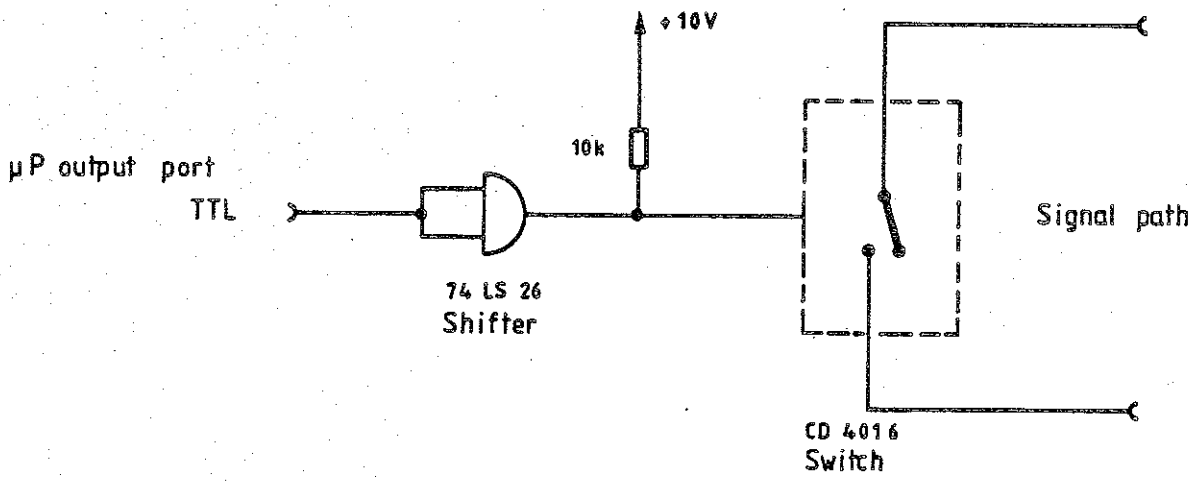


Fig. 4-1 CMOS switch control

4.1.3.2 Signal Path for Level Measurement

The demodulated signal is applied to the input via ST1/17a. Window comparator B1/I, B1/II delivers logic H to pin 21b when the input voltage has reached 2 V ±2 mV at the end of the Cal. command. The analog memory B1 in the 3rd mixer is used for this purpose with the control amplifier B1/III. In the CISPR 1 and CISPR 3 modes the comparator B1/IV supplies a negative output voltage to the gate of T10 which is thus cut off increasing the charging time constant for the analog memory.

With $\overline{\text{CISPR}}$ (= $\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$) the input signal is applied via the switch B6/I or with CISPR via pin 17b, B6/II to the non-inverting amplifier B2/I, which in conjunction with B2/II, B6/III, B6/IV and B7/I forms a programmable amplifier whose switchable gain +1 and +2 can be measured at test pin 18a (for switch control see Fig. 4-1).

B17, T2, B18, B3/I form a logarithmic converter with an input or output voltage range from 0.4 to 4 V. The linear signal is applied via B7/III, and the logarithmized signal via B7/II to the amplifier B3/II which is used as a low-pass filter. Output 7a is used for driving the LED array used for the analog level indication. If $V < 0.355$ V, the comparator B3/III causes via T3 the min.-level LED to light and if $V > 3.55$ V, B3/IV causes via T4 the max.-level LED to light. From the output of B2/I, the signal is applied via B8/III to the sample & hold amplifier for measuring the minimum and maximum levels for AM measurement or via B20/I and B14/III directly to the sample & hold amplifier for level measurement.

4.1.3.3 Signal Path for Frequency Offset Measurement

The offset voltage from -5 V to +5 V is applied via ST1/14b to the differential amplifier which supplies an output voltage from 1 to 4 V. This output voltage is available at 11a via the amplifier B4/IV which is provided with a low-pass filter. B4/II is a calibration amplifier for B19 (analog memory). It is activated through B13/I and T5 during frequency offset calibration process, charging the storage capacitor in B19, the voltage on which controls B4/I.

The calibrated frequency offset voltage of +5 V is output via 8b.

The window comparator B5/I to B5/II supplies a logic L signal to output 5b when the ESH 3 is tuned to centre frequency, or controls the center-tuning indicator via T9. The frequency offset voltage is applied via B8/I and the buffer amplifier B14/III to pin 3a (to sample & hold amplifier).

When measuring frequency deviation, B21 and B14/I are activated for positive peak deviation and B22 and B14/II for negative peak deviation.

B9/I and B9/II serve for discharging the peak-value rectifier.

4.1.3.4 AF Amplifier

The AF is applied to the DC-voltage-controlled volume control B25 via 18b. B23 is the integrated AF amplifier which is switched in via T7 and T8.

In Table 4-1, the logic functions are listed that are required for switching on the desired CMOS switch (+10 V at the control input).

Table 4-1

B6/I	:	$\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$
B6/II	:	CISPR moving-coil meter simulator = CISPR 1 V CISPR 3
B6/III	:	CISPR 1 V CISPR 3 V PEAK (3 s) V Log 40 V LOG 60
B6/IV	:	AV $\wedge$ 20 dB = CISPR 1 $\wedge$ CISPR 3 $\wedge$ PEAK (3 s) $\wedge$ Log 40 $\wedge$ Log 60
B7/I	:	PEAK (3 s) V Log 40 V Log 60 V CISPR 1 V CISPR 3
B7/II	:	$\overline{\text{Log 40}} \wedge \overline{\text{Log 60}}$
B7/III	:	Log 40 V Log 60
B8/I	:	$\overline{\text{Deviation}}$
B8/II	:	$\overline{\text{m}}$
B8/III	:	m
B9/I	:	Discharge
B9/II	:	Discharge
B20/I	:	$\overline{\text{Level}}$
B20/II	:	$\overline{\text{m, f(+)}}$
B20/III		$\overline{\text{m, f(-)}}$

4.1.4 Synthesizer 2 (Y4)

(See circuit diagram 303.7850 S)

This subassembly consists of

- the 60-MHz reference oscillator,
- the interpolation oscillator for the synthesizer 1 and
- the second mixer oscillator (66 MHz).

4.1.4.1 60-MHz Reference Oscillator

The 60-MHz reference oscillator is a high-precision crystal oscillator using transistor T10, the temperature of the crystal being internally controlled by means of a PTC resistor. This oscillator crystal reaches its final accuracy within 30 seconds thanks to its low thermal capacity.

The buffer T11

- converts the interpolation oscillator 5.0 to 5.0999 MHz up to 65.0 to 65.0999 MHz and
- drives the ECL divider B31 (functions as a 1/10 divider).

B33 (1/10) is driven via B32 (1/6). It supplies a reference frequency of 100 kHz which is taken to the Synthesizer 1 (Y5) via the motherboard. The other reference frequencies, 1 kHz for the interpolation oscillator and 500 Hz for the 2nd oscillator, are produced via the divider chain B34, B42 and B41. A further 500-Hz reference output on the motherboard supplies the filter control board, the calibration generator, the 3rd oscillator and the A1 demodulator.

The frequency of the crystal oscillator can be varied in the internal operating mode by applying a DC voltage to the crystal fine-tuning circuit GL30, GL31 and L70. For crystal oscillator adjustment procedures see section 5.3.1.4. The typical temperature stability of the oscillator is about $\pm 4 \times 10^{-6}$ over the temperature range from -10 to +45°C. The maximum tuning error at the highest receive frequency (29.9999 MHz) is thus about ±120 Hz. To fulfill still more stringent frequency accuracy requirements, it is possible to synchronize the ESH 3 via the BNC socket EXT. REF. 55 with an external standard frequency of either 5 or 10 MHz. Depending on the external reference frequency, the division ratio of the switchable divider B39-B38-B40 is set to either 50 or 100 by means of the switch 55 on the rear panel of the receiver. The phase is compared in the phase discriminator B36. Integrator B35 produces the control voltage for the crystal fine-tuning circuit, which is applied via B37 (B37 acts as changeover switch between the variable voltage from the Display Unit and the synchronization voltage).

4.1.4.2 Interpolation Oscillator

The low-microphony interpolation oscillator T3 delivers an adjustable frequency of 50.000 to 50.999 MHz. Via the buffer stages T4-T7-T8 an ECL 1/10 divider (B21) is driven so that at the output of T9 a signal of 5.0000 to 5.0999 MHz is available, with microphony and sideband noise improved by a factor of 10, for conversion in BM1. Another ECL divider (B19) is driven in parallel with B21. Together with B20 and the necessary logic control it forms a 1/100 or 1/101 divider, which is driven via the 2-decade down counter B24 and B25. The divider is preset by the frequency-setting of the receiver and the 1-kHz and 0.1-kHz values for frequency tuning. In addition, the up/down counter controls the division ratio of B18 - adjustable between 500 and 509 -, the first two decades of this division ratio being hardwired. The output frequency from B18 is compared with the reference frequency of 1 kHz in B16. The current pulses from the phase comparator B16 are integrated in the control amplifier B15 and control the varicaps in the oscillator T3 via an appropriate filter network. B17 produces a signal which gives an indication of synchronization of the overall control loop. The functioning of this circuit is explained in some detail in section 4.1.10. The functioning of the various synthesizer loops is explained by a tuning example given in section 4.1.5.

4.1.4.3 Mixer Oscillator

The signal of 66 MHz required for conversion from 75 MHz to 9 MHz is derived from a crystal oscillator whose frequency of which can be varied by ±1.5 kHz for SSB reception.

The buffer T2, which is driven by the crystal oscillator T1, supplies 7 ±2 dBm to the 2nd mixer on the board Y9 and at the same time controls the ECL divider of the synchronization circuit B1. This control circuit operates analogously to that of the interpolation oscillator, but the reference frequency is only 500 Hz and the division ratio 132000 ±3 (driven via B9).

4.1.5 Synthesizer 1 (Y5)

(See circuit diagram 303.7715 S)

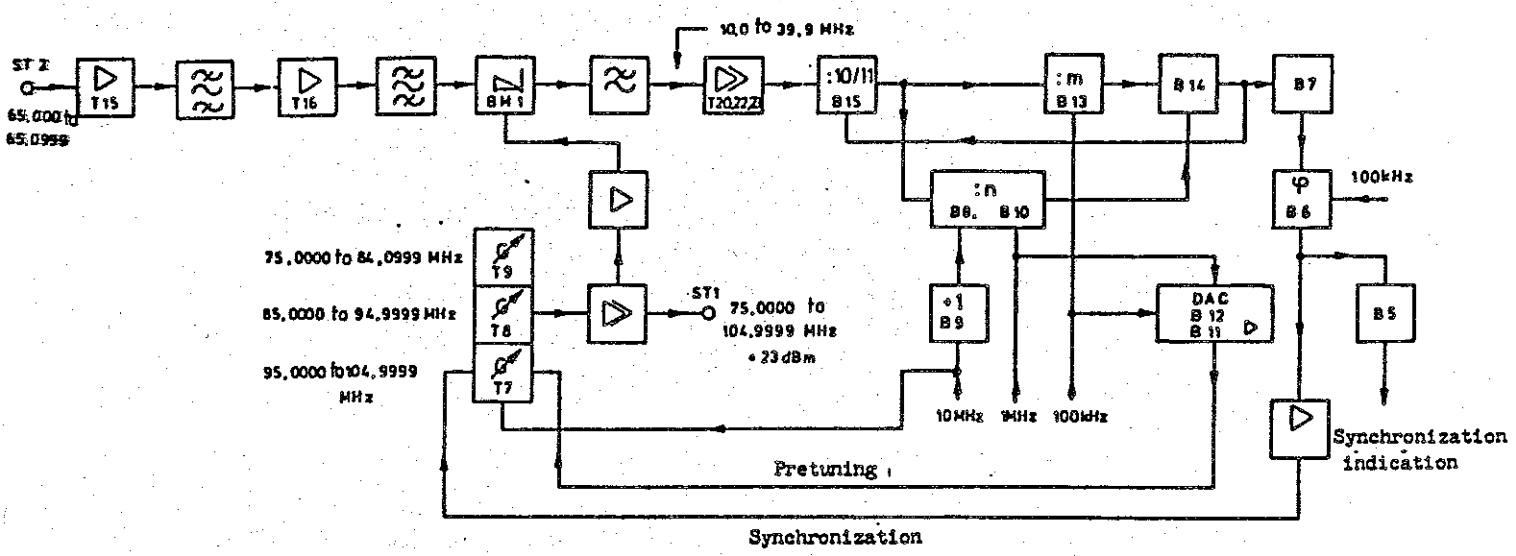


Fig. 4-2 Block diagram of the Synthesizer

The interpolation signal, of frequency 65.0 to 65.0999 MHz, supplied by the synthesizer 2 (Y4) is applied via ST2 to a selective amplifier with a bandwidth of about 1 MHz. When the signal has passed through the amplifier T15-T16, it is largely free from mixer products (60 MHz) and the 2nd sideband (55.0 to 54.9001 MHz), and it is mixed with the signal of the 1st BFO of the ESH 3 (75 to 104.9999 MHz) in the mixer BM1. The resulting sum product is terminated via a high-pass filter and the difference product passes via a low-pass filter to the amplifier T20 to T23 where it is boosted and converted to ECL level. This signal (10.0 to 39.9 MHz) is divided down to about 1 to 4 MHz in the IC dividers (SP 8695B) (1/10 or 1/11), and divided down to 100 kHz in the programmable low-power Schottky dividers with a division ratio adjustable from 100 to 399. B7 acts as a pulse stretcher. B9 adds "1" to the most significant digit of the applied receive frequency to equalize the receive frequency and the division ratio. The phase of the divided-down signal is

compared in B6 with the phase of the 100-kHz reference frequency from synthesizer 2. B5 produces a signal which indicates synchronization of the control loop (LOW = not synchronized, HIGH = synchronized). The output stage of the phase discriminator B6 drives the control amplifier B3, which acts as an integrator, with current pulses depending on the phase relationship of the two signals.

The 1st oscillator of the ESH 3 comprises three oscillators each of which covers about 10 MHz. The oscillator required is selected by appropriate gating circuits fed from the most significant digit of the programmable divider. The practically noisefree oscillators are coarsely pretuned (B12, B11) with the aid of a D/A-converted voltage derived from the 100-kHz and 1-MHz decades. This same voltage is also applied to the Filter control board Y6 and is 0 V for 0 x 1 MHz and 0 x 100 kHz and +7.5 V for 9.9 MHz. Largely freed from residual AC voltage by an appropriate filter, the D/A voltage controls the series-connected quad diodes of the individual oscillators. Synchronization is carried out by the voltage arriving from B3, which has been largely freed from residual AC voltage caused by the 100-kHz reference frequency and its harmonics. The control bandwidth is approximately 500 Hz which cuts out the greater part of the microphony of the oscillators brought about by mechanical vibrations. Sideband noise is about 138 dB/1 Hz 10 kHz away. The low-noise amplifier T10-T11-T12 boosts the oscillator signal to about +23 dBm in the frequency range 75 to 105 MHz, which is then fed to the 1st mixer (in Y9) of the receiver.

Numerical example:

The receiver is tuned to the frequency 12.3456 MHz. The 123 digits arrive at the synthesizer 1 (Y5). A further "1" is added to the "1" by means of B9 which makes a "2". This "2" switches on the oscillator by means of T8 (85 to 95 MHz) via B1, B2, T2, T5 and sets the presettable down counter B8. The figure "2" of the frequency setting is taken to B10 and sets it as the figure "3" sets the counter B13. (B12 converts the digital information "23" to a proportional DC current which in turn is converted to a DC voltage by B11, which among other things coarsely tunes the 1st oscillator.) B15 functions as a 1/10 or 1/11 divider which is kept in the 1/11 mode by B13 until B13 has counted down to "0". It is changed over to the 1/10 mode via B14 III. The preset counter chain B10, B8 is driven in parallel with B13. When it has counted down to "0", it sets B15 again to the 1/11 mode via B14 IV and the process starts again.

The effective division ratio for the above example:

$$\text{division ratio } 1 = 3 \times 11 + (22 - 3) \times 10 = 33 + 190 = 223.$$

The figure combination "456" is delivered to the synthesizer 2 (Y4). The divider B19/B20 functions as a 1/100 or 1/101 divider. The "6" sets the down counter B24, the "5" sets B25, the "4" sets B18, the next to most significant digits of which are fixed at 50... . Hence, the effective division ratio is:

$$\text{division ratio } 2 = 56 \times 101 + (504 - 56) \times 100 = 5656 + 44800 = 50456.$$

The oscillator T3 is synchronized to the frequency 50.456 MHz. This frequency is divided by 10 (B21) and after mixing it with 60 MHz 65.0456 MHz is obtained.

The lock-in frequency of the 1st oscillator is given by

$$223\ f_{\text{ref 1}} + 65.0456\ \text{MHz} = 87.3456\ \text{MHz}.$$

Since the 1st oscillator operates at a frequency that is higher than the receive frequency f_{receive} by the 1st IF:

$$f_{\text{receive}} = f_{\text{1st osc.}} - f_{\text{1st IF}} = 87.3456 - 75.000 = 12.3456\ \text{MHz}.$$

Typical pulse shapes and durations at points of major interest for the above setting of synthesizer 1 are shown in Fig. 4-3.

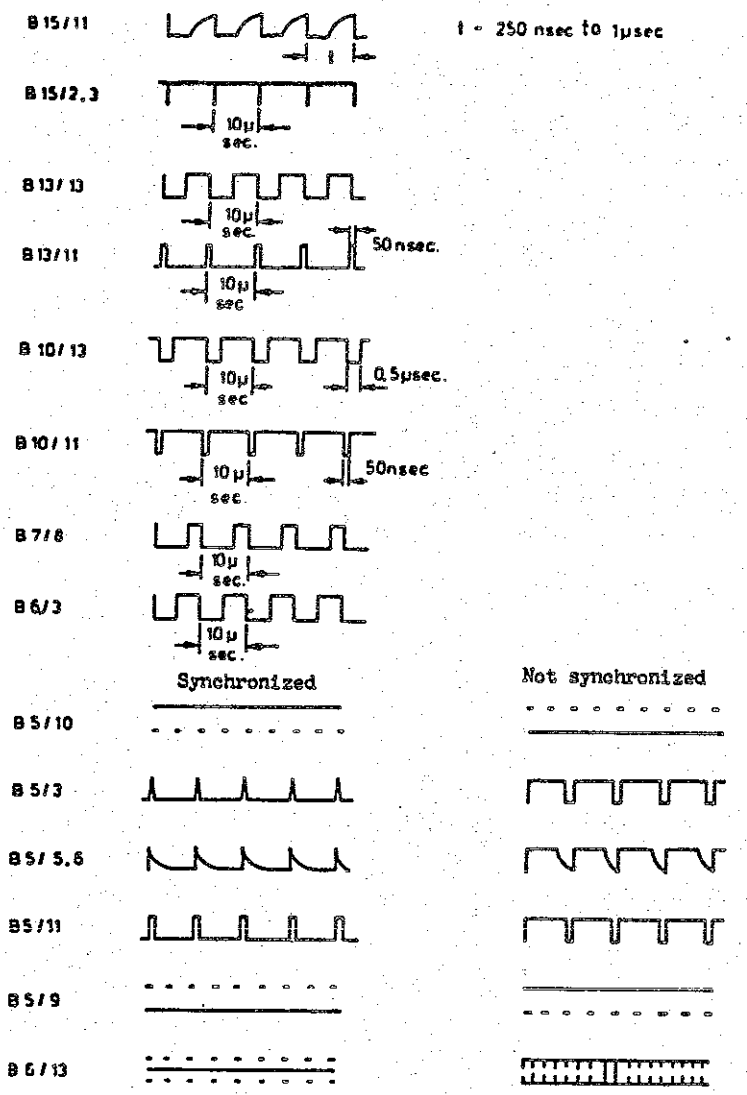


Fig. 4-3 Typical pulse shapes and durations

4.1.6 RF Preselection

The RF preselection in the ESH 3 consists of three related boards:

Filter Control (Y6)
Filter 1 (Y7)
Filter 2 (Y8)

4.1.6.1 Filter Control (Y6)

(See circuit diagram 303.7915 S)

The Filter Control performs the following three main tasks:

- Determination and selection of input filter required for the current tuning frequency.

- Generation of a tuning voltage for the tracking filters in the frequency range 10 to 29.99 MHz from the D/A-converted pretuning voltage fed to the 1st oscillator.
- De-energizing filter relays during setting procedure.

The total frequency range of the ESH 3 is subdivided into 16 filter ranges, the ranges 1 to 14 being fixed tuned while ranges 15 and 16 are tracking.

Table 4-2

Range	f_1 (MHz)	f_2 (MHz)
1	0.01	0.1499
2	0.15	0.1999
3	0.2	0.2799
4	0.28	0.3899
5	0.39	0.5399
6	0.54	0.7499
7	0.75	1.0499
8	1.05	1.4499
9	1.45	1.9999
10	2.0	2.6999
11	2.7	3.6999
12	3.7	5.1999
13	5.2	7.1999
14	7.2	9.9999
15	10.0	19.9999
16	20.0	29.9999

where f_1 is the lower cutoff frequency of a range and
f_2 is the upper cutoff frequency of a range.

The Filter Control board receives the tuning frequency read out on the front panel via the Motherboard (Y18) in the form of 14 bits for the upper four decades:

10-MHz decade (2 bits)
1-MHz decade (4 bits)
100-kHz decade (4 bits)
10-kHz decade (4 bits).

Two diode matrices on the Filter Control board store the 16 lower and the 16 upper cutoff frequencies. The ESH 3 determines which range must be selected as follows:

By comparing the magnitude of the tuning frequency f_M with that of the lower cutoff frequency f_1 (in B1 to B4) and that of the upper cutoff frequency f_2 (in B5 to B8) of the particular range selected, the procedure is controlled by the following simple mathematical functions:

a) $f_M > f_2$:
The selected range is too low.

b) $f_M < f_1$:
The selected range is too high.

c) $f_M > f_1$, but $< f_2$:
The selected range is correct.

The ranges are switched by applying a 500-Hz clock pulse to a decade up/down counter (B9) which controls a 1-out-of-16 decoder (B10). The decoder B10 drives the diode matrices and the switching transistor for the selected range. The direction of the B9, as well as its inhibition after the range determination has been accomplished, is controlled by B11. The transistors T1 and T2 prevent the range relays from being successively cut in after the receiver has been switched on for first-time adjustment.

For generation of the tuning voltage for the ranges 15 and 16, a DC voltage between 0 and +7.5 V, produced in the Synthesizer 1 (Y5) from the 1-MHz and 0.1-MHz decades by D/A conversion, is applied to the Filter Control board (Y6) via the Motherboard (Y18). It is converted to a voltage between +3 and +25 V by a network made up of resistors and operational amplifiers B12 to B14, the input/output relationship of this network being chosen so as to linearize the voltage/frequency characteristic of the tracking filters.

4.1.6.2 Filter 1 (Y7)

(See circuit diagram 303.7015 S)

Filter 1 (Y7) contains the filter ranges 1 to 8 (corresponding to the frequency range 10 kHz to 1.45 MHz). The tasks of the filters 2 to 8 are identical with those of the filters 9 to 16. Except for filter range 1 (10 kHz to 150 kHz), which covers more than one decade, special circuitry has been added to improve the harmonic distortion of the input mixer.

4.1.6.3 Filter 2 (Y8)

(See circuit diagram 303.7415 S)

The subassembly Filter 2 (Y8) contains the filter ranges 9 to 16 (corresponding to the frequency range 1.45 to 29.9999 MHz).

The tasks of the filters are as follows:

- Improve the harmonic distortion of the 1st mixer.
  This means the filter has to provide attenuation at frequency $f_K = \frac{f_2}{2}$, approximately 20 dB with the filters selected.
- Limit the pulse bandwidth (6-dB bandwidth) at the receiver input, above all in the frequency range 10 to 30 MHz to relieve the 1st mixer.

If a range > 8 is selected, the individual filter ranges are switched on via the reed relays RS17 to 34 and the filter 1 is cut off.

4.1.7 1st and 2nd Mixers (Y9)

See circuit diagram 303.6019 S (model 52)
839.9035 S (sheet 1 and 2) (model 56)

Note: The figures given in brackets refer to model 56 (e.g. T2 (V111) denotes transistor T2 in model 52 and V111 in model 56).

This board largely determines the dynamic characteristics of the ESH 3 (harmonic distortion, intermodulation, 1-dB compression, crossmodulation) as well as its performance with respect to image-frequency rejection, oscillator reradiation and IF rejection. The input signal passes through a 9-section Chebishew low-pass filter with a cutoff frequency of about 35 MHz which ensures a rejection of the oscillator frequency from 75 to 104.9999 MHz and of the image frequency from 150 to 179.999 MHz of better than 70 dB. From there, the signal passes via a link to the first mixer which, for model 52, is a high-power mixer (B1) receiving via ST3 an oscillator power (+23 dBm) from the synthesizer 1 (Y5). The 1st mixer of the ESH 3 (model 56) is made up of an 8-diode IC V101 and the balance-to-unbalance transformers T4 and T5. The oscillator power is provided (+23 dBm) via T4. The V101 amplifier generates a 50 Ω termination for the LO gate for all oscillator frequencies. The RF signal is routed to the 8 diodes and the IF signal is taken off via T5. An optimum symmetric design and a specially selected group of 8 diodes ensure an LO suppression of the mixer of > 66 dB. The reduced oscillator power for the reconversion in the tracking generator is available at ST4 (X4) via R94, R95 (R208, R209).

The signals generated in the IF gate of the 1st mixer (above all $f_{1st\ osc}$/ $f_{sum} = f_{1st\ osc} + f_{receive}$, $f_{difference} = f_{1st\ osc} - f_{receive} = f_{IF} = 75$ MHz) are routed to the first IF amplifier T1 (V111) and the overload detection circuit T2 (V200) via ST9 (X9). This circuit simultaneously amplifies f_{sum} and $f_{difference}$ and - after rectification - takes them to a fast comparator B4/I (N4/A) whose rise time is low as against the maximum RF bandwidth of the receiver. The output pulse from the comparator is taken via a pulse stretcher (B8/I) to the Control Board (Y3) for further processing.

T14 (V140) and T15 (V150) amplify the 1st IF with a bandwidth of approx. 2 MHz. The IF signal, e.g. for an IF panoramic monitor, is available at the output ST13 (X14). The IF signal amplified by T1 (V111) passes through a diode limiter (for protection of the crystal filter B2), an attenuator and the following lowpass filter (for suppression of self-generated spurious) to the two-stage low noise amplifier T3 (V300) and T4 (V500). The following lowpass filter suppresses additional self-generated spurious.

The 75-MHz IF signal is converted to the 2nd IF of 9 MHz in the 2nd mixer with the aid of the 2nd oscillator whose frequency is 66.000 MHz, 66.0015 MHz or 65.9985 MHz depending on the type of demodulation. The oscillator power of +7 dBm = 5 mW is applied via St5 (X5). A reduced oscillator power is available at ST6 (X6) for reconversion in the calibration generator (Y10). The sum product $f\Sigma$ = 75 MHz + 66 MHz = 141 MHz obtained at the output of the mixer is amplified in T6 (V60) and after rectification, comparison and pulse stretching taken to the Control Board (Y3). The difference product 75 MHz - 66 MHz = 9 MHz separated by means of the series-resonant circuit C31, C32 and L17 is taken to the amplifier T11 to T13 (V110, V120, V130) via the low-noise and high-level amplifier T7 to T10 (V700, V800, V90, V100) by means of the diode switch for the IF bandwidths and subsequently via a lowpass filter to the output St7 (X7). The maximum IF bandwidth is determined by B2 (6-dB bandwidth about 9.5 kHz) and the two next smaller bandwidths by B7 and B6.

4.1.8 Calibration Generator (Y10)

(See circuit diagram 303.6319 S)

The calibration generator performs the following tasks:

a) Produces temperature-independent input signal of constant level at the tuning frequency of the receiver for calibration of receiver gain (output ST1: -67 dBm).

b) Supplies a second signal of the same frequency and at a level that permits two-port measurements over as wide as possible a level range (output ST2: -27 dBm).

c) Supplies a filtered amplitude-limited output signal at the exact frequency of the input signal (but displaced in phase due to internal time delays) for remote frequency measurements (output ST2: -27 dBm).

4.1.8.1 Sinewave Calibration with AV., PEAK Indication

The signal (4th oscillator with sinewave calibration or the limited last IF with remote frequency measurement) applied to ST4 is mixed with the 3rd oscillator:

$$f_{3rd\ IF} + f_{3rd\ osc.} \longrightarrow f_{2nd\ IF}.$$

The signal obtained at the 2nd IF is so heavily attenuated at ST5 by the well-balanced design of the mixer B1, the return loss of T2 and the attenuator R2-R3-R4 that it does not disturb the ESH 3's indicating circuitry.

$f_{2nd\ IF}$ is boosted in T1. Its spectrum can be improved to meet stringent requirements with respect to suppression of non-harmonic spurious frequencies for special applications, by retrofitting a filter. After further amplification in T5, the 9.0-MHz signal is taken to B3 where it is mixed with the 2nd oscillator which obtains its required level from the two-stage amplifier T3, T4 with a high return loss.

The signals at f = 66 MHz $\pm$9 MHz are amplified in T7 and taken to the filter B4 which passes them on to T12 almost unattenuated on account of its selectivity about the 75-MHz component (= $f_{1st\ IF}$). The boosted 75-MHz signal is applied to T14 whose gain is adjustable by means of GL6. In B5 the 75-MHz signal is mixed with the 1st oscillator signal, which is coupled out via the non-interactive amplifier T13, T15.

As a result, a signal is obtained at the tuning frequency of the receiver:

$f_{receive} = f_{1st\ osc.} - f_{1st\ IF}$ = 10 kHz to 30 MHz. It passes through a 7-section Chebishev low-pass filter which heavily attenuates $f_{1st\ osc.}$ and $f_{1st\ osc.} + f_{1st\ IF}$, and is then taken to the broadband amplifier T16-T17-T19-T20. The boosted signal is rectified in GL10 and after temperature compensation by means of GL9 and B7 its voltage is compared with the variable voltage at the input of B6/I. The resulting difference voltage is amplified in B6/I making for frequency-independent level control. Addition of a temperature-dependent adjustable current to the currents into the + or - input of B6/I provides temperature compensation.

The output signal from T19-T20 (-1 dBm) is split into two paths:

- Path 1 (ST2) is used for two-port and remote frequency measurements
- Path 2 (ST1) is used for internal calibration of the receiver.

R110 (CAL.CORR.) permits the readout to be set to 80 dB(μV) when making two-port measurements.

4.1.8.2 Pulse Calibration (CISPR 3: f < 150 kHz; CISPR 1: f ≥ 150 kHz)

The 500-Hz TTL signal supplied by synthesizer 2 (Y4) is divided by 20 (CISPR 3) or 5 (CISPR 1) in a programmable 1/5 or 1/4 divider. Needle pulses with a pulse repetition rate of 25 or 100 Hz are produced, whose pulse width is adjustable with R89 (CISPR 3) or R91 (CISPR 1). R124 is used for temperature compensation. The output pulse from B12 passes to the voltage follower T21 and via RS1 to the calibration output ST1.

According to CISPR 3, a pulse of 13.5 µVs is required for calibration which should give an indication of +60 dB(µV) = -47 dBm at an IF bandwidth of 200 Hz.

According to CISPR 1, a pulse of 0.316 µVs is required for calibration which should likewise give an indication of +60 dB(µV) = -47 dBm at an IF bandwidth of 9 kHz.

Since the Receiver ESH 3 is internally calibrated with a sinewave level of -67 dBm, the internal pulse generator must supply pulses that are smaller than the specified CISPR pulses by 20 dB.

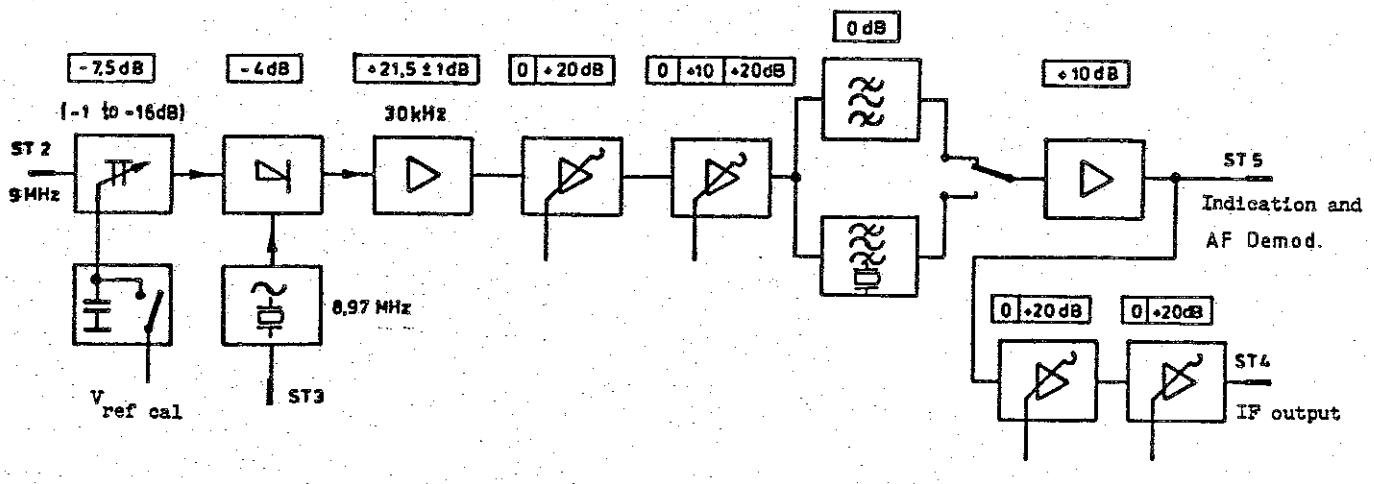
The frequency response of the pulse generator at the upper frequency range limit can be varied by means of C90 for a flatter indication.

4.1.9 3rd Mixer (Y11)

(See circuit diagram 303.6219 S)

The 3rd mixer performs the following tasks:

- Corrects the gain over entire signal path between the RF input and the display during level calibration (PIN-diode attenuator with store IC B1).
- Converts 9.0 MHz to 30 kHz using a built-in 8.97-MHz oscillator (phase-locked loop with 500-Hz reference).
- Adjusts the IF attenuation in steps, 0 to +40 dB, by means of B10, B15.
- Filters out the noise before the indication and AF demodulation to preserve the overall noise figure at 500-Hz and 2.4-kHz IF bandwidth.
- Switches over to 200 Hz IF bandwidth by means of the mechanical filter B18. Indicates any overload of the stages preceding the 200-Hz filter.
- Switches the IF gain over before the IF output.



IF attenuation

"0db":	+20dB	+20dB			
"+10dB":	+20dB	+10dB	Log 60:	0dB	0dB
"+20dB":	+20dB	0dB	Log 40:	20dB	0dB
"+30dB":	0dB	+10dB	Lin :	20dB	20dB
"+40dB":	0dB	0dB	CISPR1:	20dB	0dB
			CISPR3:	20dB	0dB

Fig. 4-4 Block diagram of the 3rd mixer

The 8.97-MHz oscillator consists of a crystal oscillator which is trimmed by means of a phase-locked loop. The IF attenuation is selected by switching the feedback which sets the gain of two operational amplifiers. Two stagger-tuned active resonant circuits (B16-B21) filter out the noise.

4.1.10 Indication and AF Demodulation (Y12)

(See circuit diagram 303.6919 S)

The Indication and AF Demodulation board obtains the 30-kHz IF signal from the 3rd mixer, from which it produces signals for the level indication) as well as AF voltages (e.g. for the AF amplifier) by means of various demodulators.

In Fig. 4-5, a simplified block diagram is shown. The signal path for the indication demodulation is completely separate from the signal path for the AF demodulation.

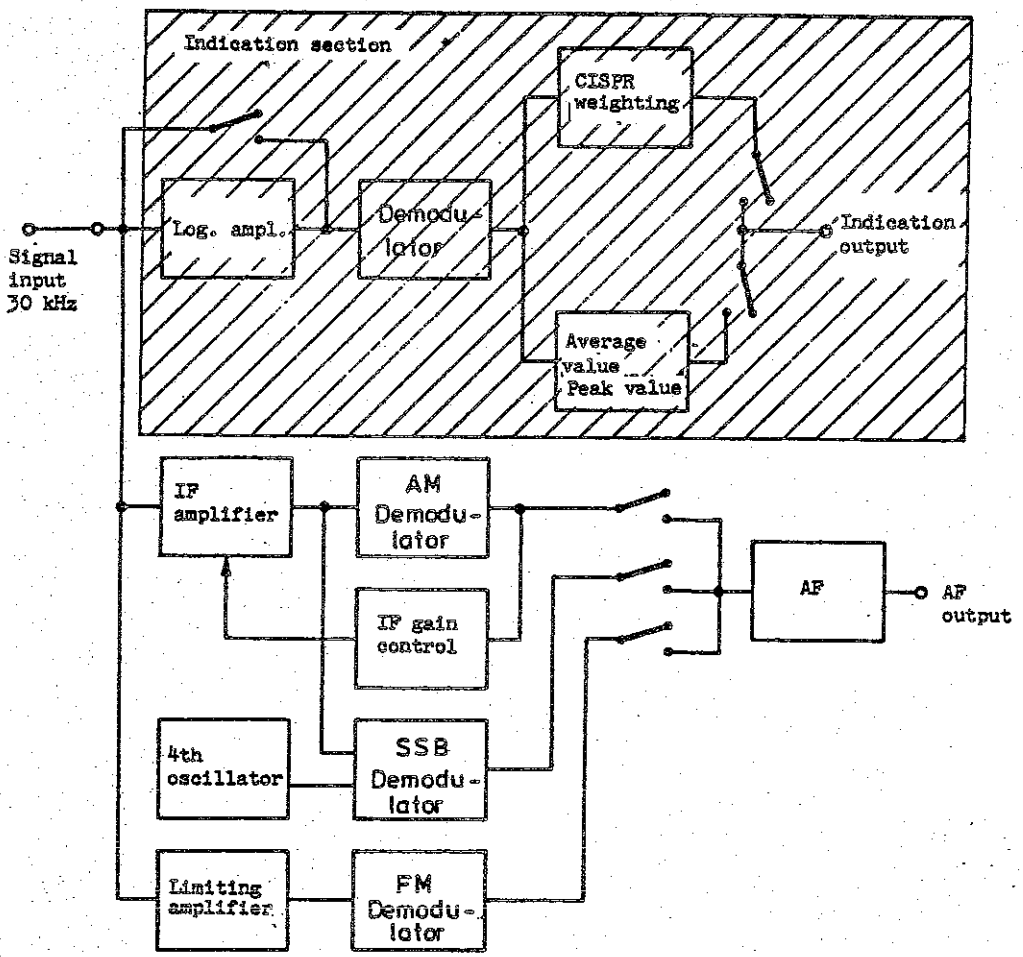


Fig. 4-5 Block diagram of indication and AF demodulation

The indication section demodulates the input signal and produces a DC voltage for level measurement. Moreover, signal weighting according to CISPR or peak value indication is possible.

To achieve a wider indicating range than 20 dB with linear demodulation, a logarithmic converter for the instantaneous value can be connected before the demodulator. In this way, the 40-dB and the 60-dB ranges are obtained.

The AF demodulation section permits reception of AM and FM as well as SSB and telegraphy signals.

The FM demodulator consists of a limiting amplifier which is followed by a PLL demodulator. It is separate from the circuit for the other demodulation modes.

The latter contains an automatic gain controlled IF amplifier. This control circuit keeps the AF voltage nearly constant even in the case of large level differences and permits easy aural monitoring of the input signal. In AM operation, the AF voltage is derived from the IF signal by means of an active rectifier which supplies at the same time the input voltage for the control amplifier.

With telegraphy and SSB demodulation, the amplified IF signal is taken to a product detector. The mixer signal is supplied by the 4th oscillator which is also included on the board. The control circuit is switched over with telegraphy and SSB demodulation and the rise and fall times are adapted to the demodulation mode selected.

Because of limiting in the FM mode and level control in the other demodulation modes, the input level cannot be determined from the volume of the AF signal. This is only possible by separate indication demodulation. The detailed block diagram of this subassembly is shown in Fig. 4-6.

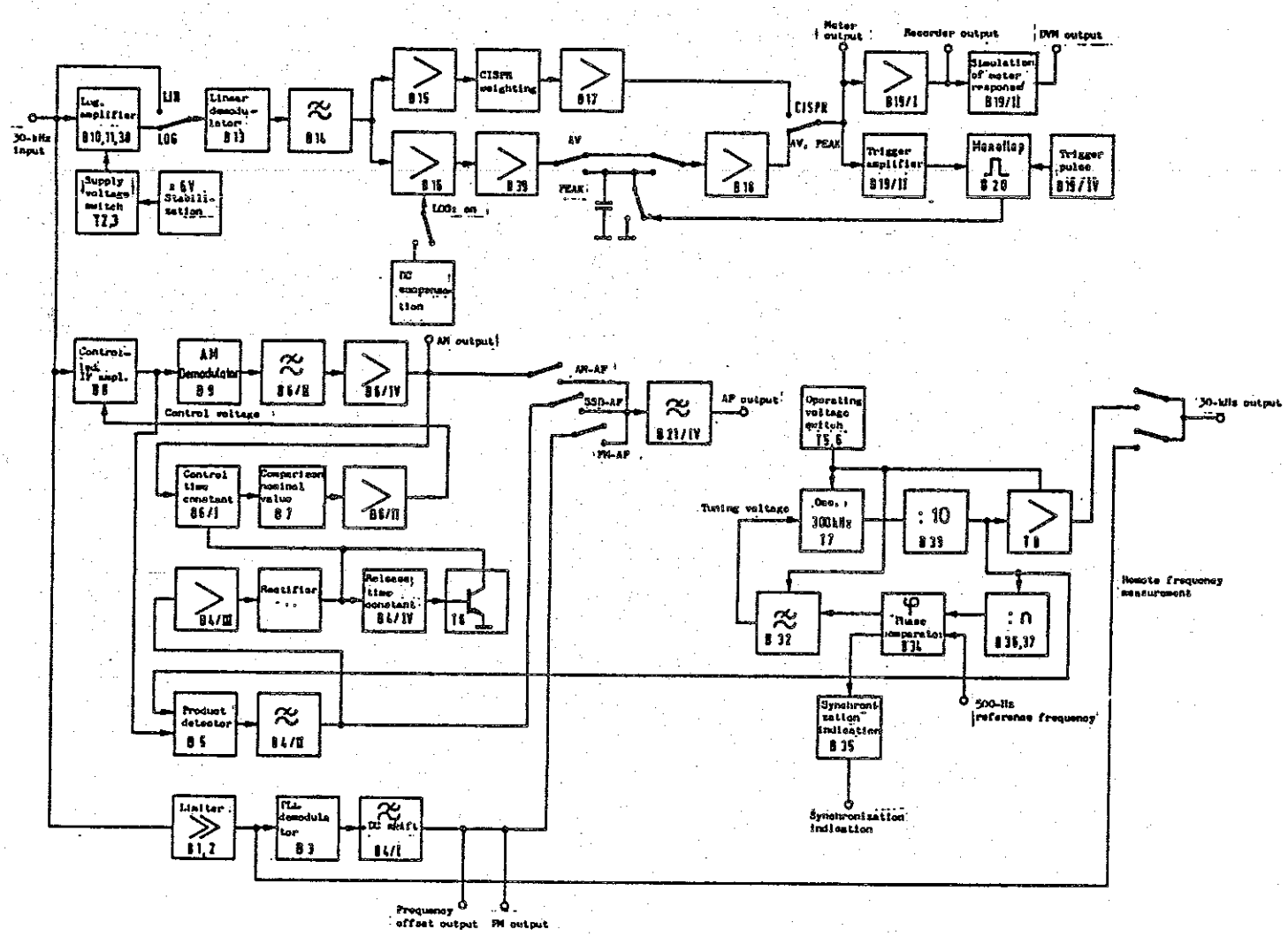


Fig. 4-6 Block diagram of indication and AF demodulation

4.1.10.1 IC Switches

For the numerous switching functions, IC analog switches are used. They are entered in the circuit diagram as normal switches with the designations S1, S2, etc. For the sake of clarity, the control circuit is drawn separately from the switches.

Depending on the requirements, two different types of IC switches are used: CD 4016 and IH 5027. An essential difference between the two types is that the CD 4016 switches on with a positive (+10 V) and the IH 5027 with a negative (-6 V) control voltage. Unlike the CD 4016, the IH 5027 does not require a supply voltage.

Table 4-3 contains a summary of the control inputs to the board. They are driven with TTL signals. The particular function is switched on if the level is at high.

The comparators B22-23-24-25 convert the TTL signals to the above mentioned levels of +10 V and -6 V required for driving the IC switches. The comparison voltage is produced by means of R239, GL67 and GL68 and amounts to 1.4 V.

OR gates formed by diodes gate the control signals. For example, S9 is to switch on with PEAK1 or PEAK3 (SP1 v SP3). The signals are gated by means of GL63-GL64-R264. The output of the OR gate is connected to the inverting input of the comparator B24/II. Since it is an IH 5027 type switch, S9 requires a negative output voltage from the comparator to switch on.

Table 4-3: Control inputs

For the indication demodulation:		
CISPR 1	Signal weighting in the indication path according to CISPR Publ. 1	
CISPR 3	Signal weighting in the indication path according to CISPR Publ. 3	
PEAK1	Peak-value measurement with 1 s hold time	With the ESH 3, only control input PEAK3 is used for switching on peak-value indication.
PEAK3	Peak-value measurement with 3 s hold time	
LOG 40	Logarithmic indication, 40-dB range, corresponding to 40-dB operating range	
LOG 60	Logarithmic indication, 60-dB range, corresponding to 60-dB operating range	

For the AF demodulation	
AM	AM demodulation
FM	FM demodulation
A0	Demodulation of telegraphy, for adjustment to zero beat
A1	Demodulation of telegraphy
USB	Demodulation of AM SSB signals, upper sideband
LSB	Demodulation of AM SSB signals, lower sideband
Other:	
RFM	Remote frequency measurement
30 kHz ON 4th oscillator at 30.0 kHz	

Table 4-4 contains a summary of all the IC switches and their respective control inputs.

Table 4-4 IC switches and switch control

Switch	No.	Type	Triggered in mode	Triggered by
S1	B31/I	IH 5027	$\overline{\text{LOG 40 v LOG 60}}$ (= LIN)	B25/II
S2	B31/II	IH 5027	LOG 40	B25/I
S3	B31/III	IH 5027	LOG 60	B25/III
S4	B27/I	CD 4016	LOG 40 v LOG 60	B25/II
S5	B29/IV	IH 5027	LOG 40	B25/I
S6	B31/IV	IH 5027	$\overline{\text{LOG 60}}$	B25/III
S7	B29/III	IH 5027	$\overline{\text{PEAK1 v PEAK3}}$ (= AV)	B24/III
S8	B29/II	IH 5027	Triggered in mode PEAK by B20	
S9	B29/I	IH 5027	PEAK1 v PEAK3	B24/II
S10	B28/I	IH 5027	CISPR 1	B23/IV
S11	B28/II	IH 5027	CISPR 1	B23/IV
S12	B28/III	IH 5027	CISPR 1 v CISPR 3	B23/II
S13	B28/IV	IH 5027	$\overline{\text{CISPR 1 v CISPR 3}}$	B23/III
S14	B30/II	CD 4016	PEAK3	B24/I
S15	B30/III	CD 4016	$\overline{\text{A1 v USB v LSB}}$ = (AM v FM v A0)	B23/I
S16	B30/I	CD 4016	$\overline{\text{CISPR 1 v CISPR 3}}$	B23/II
S17	B27/III	CD 4016	$\overline{\text{A1 v USB v LSB}}$ = (AM v FM v A0)	B23/II
S18	B28/IV	CD 4016	A1 v USB v LSB	B25/IV
S19	B26/III	CD 4016	A1	B22/II
S20	B26/II	CD 4016	FM	B22/III
S21	B26/I	CD 4016	A0 v A1 v USB v LSB	B22/I
S22	B27/II	CD 4016	AM	B22/IV
S23	B26/IV	CD 4016	A1 v USB v LSB	B25/IV

4.1.10.2 Indication Section

In the indication section, the 30-kHz IF signal applied to ST2 is processed. The following levels are permissible at ST2 for the various measurement ranges:

LIN	2 to 20 mV (rms)	corresponding to 20-dB operating range with the ESH 3
LOG 40 dB	2 to 200 mV	corresponding to 40-dB operating range
LOG 60 dB	2 to 2000 mV	corresponding to 60-dB operating range

4.1.10.2.1 Logarithmic Amplifier

A logarithmic amplifier consisting of B38 is connected before the indication demodulation. It is triggered only in the LOG 40 or LOG 60 mode. In the LIN mode, it is bypassed by S1.

The supply voltages +6 V and -6 V are produced and stabilized by T1 and T4. S4 makes contact only in the LOG 40 or LOG 60 mode causing T2 and T3 to conduct which in turn connect the supply voltages through to the logarithmic converter. In the LIN mode, T2 and T3 are cut off to save current.

The signal present at ST2 is either applied directly to the inputs A1, A2, B1, B2 or after attenuation by 30 dB or amplification by 30 or 60 dB (see Fig. 4-7). The 30-dB amplifier stages consist of the operational amplifiers B10 and B11.

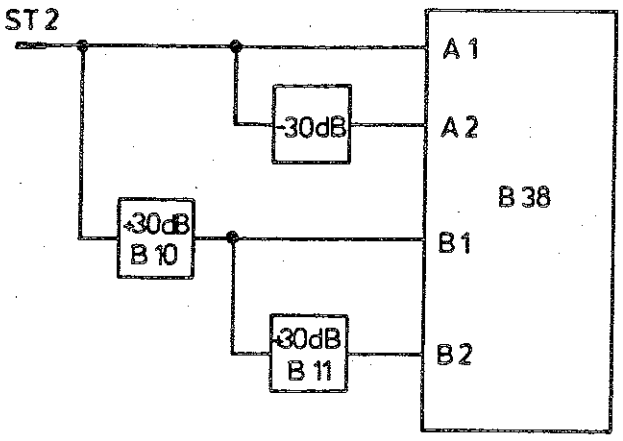


Fig. 4-7 Driving circuit of B38

R128, R123, R126 permit exact setting of the attenuation and gain, respectively of the 30-dB attenuators or amplifiers. In this manner, the logarithmic characteristic can be adjusted.

The diodes GL23 to 28 reduce the supply voltage of B10 and B11 to +4 V thus limiting the voltage at the inputs B1 and B2 of B38.

The differential amplifier B12 combines the currents at the outputs of B38. The NTC resistors R145 and R146 serve for temperature compensation of the complete logarithmic amplifier. The attenuators are connected to the output of B12 according to the measurement range selected: R138-R139-R140 in the LOG 40 mode and R137-R141-R142 in the LOG 60 mode.

4.1.10.2.2 Indication Demodulation

The signal path is the same in the operating modes LOG 40, LOG 60 and LIN (corresponding to 40-dB, 60-dB and 20-dB operating ranges) after the switches S1, S2, S3. B13 functions as an active demodulator consisting of the diodes GL85 I and II. Then the signal is taken to the balanced active filter B14 whose cutoff frequency is 10 kHz.

With an input signal of 2 mV_{rms} present at ST2 in switch position LIN, the output voltage at B14 is approximately 20 mV.

Offset compensation control R164 is used for adjusting maximum gain linearity of B14 so that the output voltage at 20 mV input voltage is exactly 10 times that at 2 mV.

After B14, the signal paths split up depending on whether CISPR or average-value (AV) or peak-value (PEAK and MIL) indication has been selected.

4.1.10.2.2.1 CISPR Meter Amplifier

B15 and B17 are the active components of the meter amplifier section which is used only with CISPR weighting. B15 is a peak rectifier. Offset compensation control R174 permits it too to be adjusted for maximum gain linearity.

It drives the RC network R190-R192-C82 whose charging time constant of 45 ms and discharging time constant of 500 ms comply with the provisions of the CISPR Publication 3. GL86 prevents the capacitor from discharging via B15.

The CISPR Publication 1 specifies a charging time constant of 1 ms and a discharging time constant of 160 ms. For this reason, the resistors R192 and R193 are added for CISPR 1.

B17 amplifies the input voltage by a factor of 10. R195 permits exact zero setting. R198 enables exact setting of the gain.

4.1.10.2.2.2 Meter Amplifier for Average- and Peak-value Indication

B16 amplifies the input signal by a factor of 10. Zero setting is accomplished with R177. R182 serves for gain adjustment. The voltages produced by means of the adjustable dividers R179, R185, R186 and R172, R187, R188 are taken via R181 to the inverting input of B16 in the operating modes LOG 40 and LOG 60. As a result, the output voltage of B16 is reduced in the LOG 40 and LOG 60 modes to ensure the same voltage range at the meter output in the LIN, LOG 40 and LOG 60 modes.

The gain of the following operational amplifier B39 is unity. GL81 prevents C97 from discharging via B39 in peak-value measurements. When measuring the peak value, S9 is closed. C97 is the storage capacitor for the peak value. In the PEAK 1s mode, C97 is discharged every second and in the PEAK 3 mode, every three seconds by means of S8.

When measuring the average value S9 disconnects C97 and in its place R189 is switched on by means of S7, which prevents charging of the non-inverting input of B18. The average value is calculated in the microcomputer.

Switch S8 discharges the peak-value storage capacitor C97. This switch is controlled via input SP50 directly by the allocated port on the Computer Board, depending on the selected measuring time. A discharge takes place whenever the measuring time ends. As a result, B20 has no function in the ESH 3.

4.1.10.2.3 Indication Outputs

4.1.10.2.3.1 Meter Output (ST1/a2)

S12 or S13 connects either the CISPR meter amplifier or the meter amplifier for average- and peak-value indication to the output ST1/a2. When making average-value and peak-value measurements, the voltage range is 0.2 to 2 V with an input signal of

2 mV to 20 mV in the LIN mode	(20-dB operating range)
2 mV to 200 mV in the LOG 40 mode	(40-dB operating range)
2 mV to 2 V in the LOG 60 mode	(60-dB operating range)

at ST2.

No logarithmic measurement is possible with CISPR weighting.

4.1.10.2.3.2 Recorder Output (ST1/a6)

B19/I produces the recorder output level

0.5 V to 5 V in the AV or PEAK indicating mode
0.2 V to 2 V with CISPR weighting

from the signal at the output ST1/a2.
The output impedance is 10 kΩ.

4.1.10.3 AF Demodulation

The AF demodulation section supplies the signals for the AF amplifier and the various demodulator outputs. It contains an AM and an FM demodulator as well as a demodulator for SSB and telegraphy signals.

4.1.10.3.1 FM Demodulation

B1 and B2 boost a weak input signal by about 80 dB. Stronger signals are limited by means of GL3, GL4 as well as by GL1, GL2. The input 14 of B3 is thus driven with squarewave pulses.

A PLL circuit based on B3 demodulates the FM signals. The voltage-controlled oscillator (VCO) contained in B3 is synchronized in phase with the input signal by means of the phase comparator that is also in B3. The demodulated AF signal is the control voltage of the oscillator if a frequency-modulated signal is fed in. Fig. 4-8 shows the block diagram.

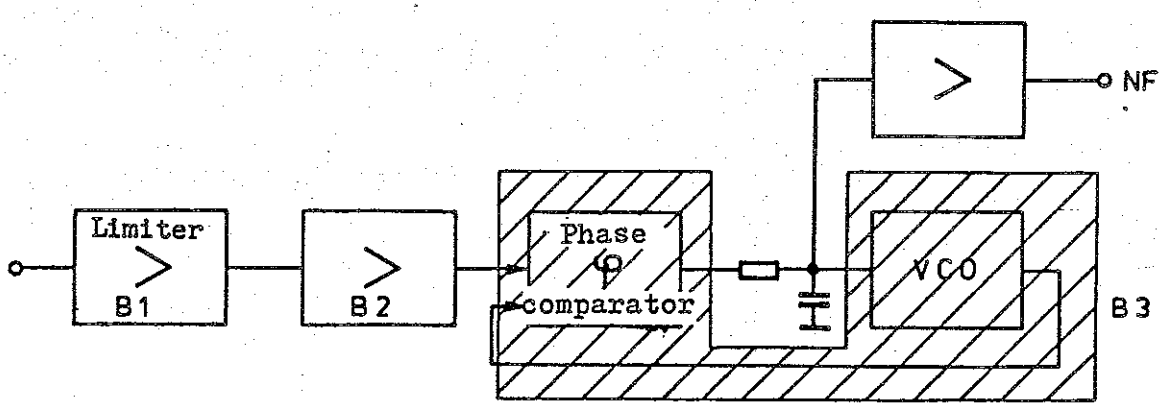


Fig. 4-8 Block diagram of the FM demodulation

C7 and the resistors at pins 11 and 12 of B3 determine the oscillator frequency. The oscillator is adjusted to the centre frequency of 30 kHz by means of R19. R17 serves for temperature compensation.

After amplification and limiting in B1 and B2, the input signal is available at input 14 of the phase comparator. The signal from pin 4 of the internal oscillator is available at input 3. The output voltage of the phase comparator at pin 2 passes through a low-pass filter to the tuning input of the oscillator.

This is also where the AF voltage is derived which is boosted by B4/II so that the voltage at its output corresponds exactly to 1 V per kHz offset from 30 kHz. It is available at the frequency offset output.

The demodulated signal is also available at the FM output ST3. On account of the voltage divider R30, R49, the voltage is here 0.1 V per kHz offset, and the source impedance 10 kΩ.

The AF voltage passes then via the voltage divider R28, R29 and the switch S20 to the AF filter comprising B21/IV. The cutoff frequency of the filter is 8 kHz. Its gain is unity. It supplies about 200 mV_{rms} to the AF output (ST1/a3) at 5 kHz deviation.

4.1.10.3.2 AM, SSB and Telegraphy Demodulation

The same AGC-controlled IF amplifier B8 (TCA 440) is used for AM, A0, A1, USB and LSB. A simplified block diagram of B8 is shown in Fig. 4-9.

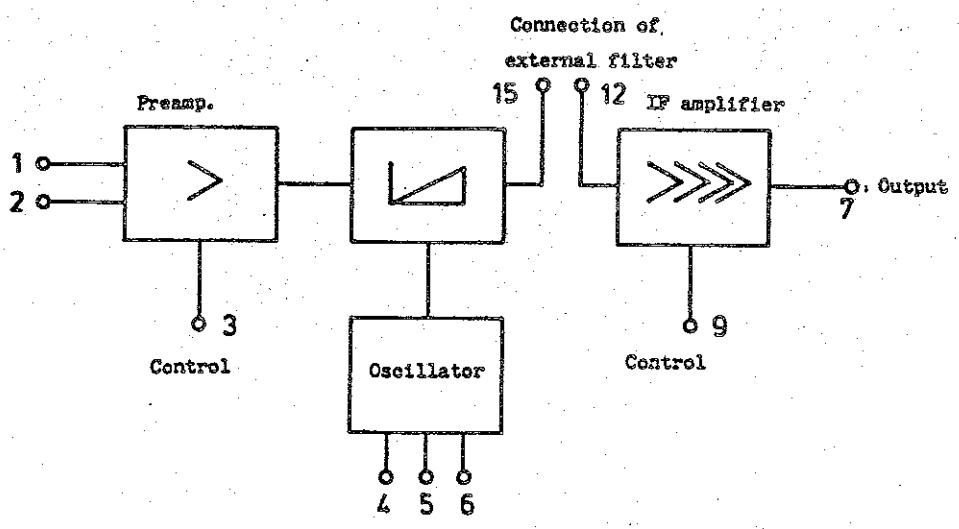


Fig. 4-9 Simplified block diagram of the B8 (TCA 440)

The internal oscillator is disabled by the connections to pins 4, 5, 6. The preamp and the IF stages operate at 30 kHz. The gain is controlled by the voltage at pins 3 and 9. A positive control voltage decreases the gain. The automatic gain control keeps the output signal at pin 7 at about 20 mV_{pp} (see sections 4.1.10.3.2.1 and 4.1.10.3.2.2).

4.1.10.3.2.1 AM Demodulation

B8 is followed by an active demodulator using B9 for AM demodulation. Then the signal is taken to the differential amplifier B6/II with a gain of 27 and an upper cutoff frequency of 10 kHz. The voltage follower B6/IV drives the AM output ST4. 1 V_{pp} at the AM output corresponds to a modulation depth of 100%. The source impedance is 10 kΩ. Fig. 4-10 shows the voltage at the AM output at various modulation depths.

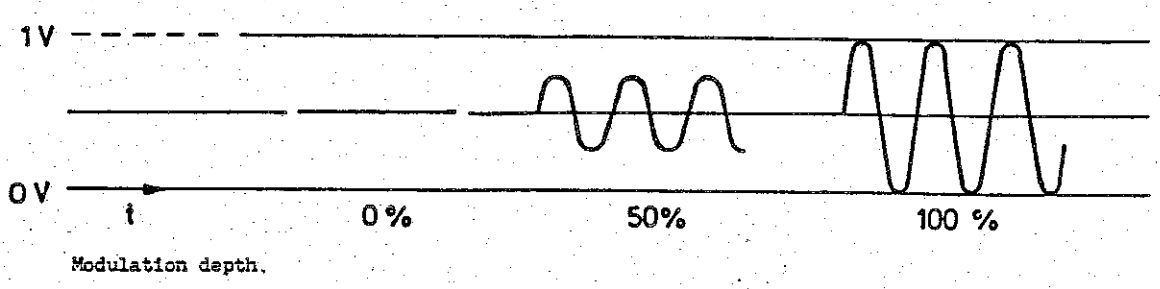


Fig. 4-10 AM output

Control with AM

The demodulated signal is further processed to obtain the control voltage. The switches S17 and S15 after the voltage follower B6/I are closed in AM demodulation. The low-pass filter R61-R64-C22 filters out the AF superimposed on the DC voltage and sets the AM control time constant of 0.5 s.

The voltage divider comprising GL20 and R67 produces the nominal control value at the inverting input of B7. B7 compares the nominal value with the actual value at the non-inverting input. B6/II boosts its output voltage for the control of B8. The voltage dividers match the levels to the two control inputs B8/3 and B8/9.

Control with AM

To generate the AM control voltage the demodulated signal is buffered by B6/IV and then transferred to the RC lowpass R61-R64-C22 via S17. This lowpass suppresses the alternating voltage component of the AF signal (time constant 0.5 s). To render interfering pulses more audible GL94 and R78 are connected in parallel to the charging resistor R61 via the switch B40. The quasi-peak value of the AF signal is used for control, so that the volume of noise is reduced. Furthermore, instead of the AF lowpass B21 the diode GL98 is cut into the AF path via the switch B41. Thus weak pulses are accentuated to such an extent that they can easily be distinguished from the noise. However, sinewave signals are distorted. If necessary, the position of link ST7 can be changed in such a way (connect 2 and 3) that the quasi-peak value is no longer the basis of control.

The control voltage is generated at the subsequent amplifier B7 by comparison of the AF centre frequency to the nominal value (voltage at GL 20). B6/III amplifies the control voltage, and the subsequent voltage dividers match it to the control inputs of the AM component B8.

4.1.10.3.2.2 Demodulation of A0, A1, USB, LSB

For the demodulation of telegraphy and SSB transmissions, a carrier produced by the 4th oscillator must be added to the IF signal (see 4.1.10.4). The output signal of the IF amplifier B8 is applied to the ring modulator B5 (pin 1) where it is mixed with the signal of the 4th oscillator which is available at pin 10.

The balanced output signal available at pins 6 and 12 is applied to the active low-pass filter B4/I (f_{cutoff} = 3 kHz). The filtered AF voltage is taken to B21/IV via S21 (see 4.1.10.3.1).

Control with A1, USB, LSB

Another difference between the demodulation of A1, USB and LSB signals and the AM demodulation is in the control of B8. With telegraphy and SSB transmissions, the signal level fluctuates heavily since the carrier is not constantly present. Hence, it is desirable that the control of the IF amplifier reacts very fast in the case of a signal increase. The fall time of the control should be longer to prevent the noise during voice transmission and keying intervals from being amplified.

The control circuitry for A1, USB and LSB has been designed with this in mind. With A0, the IF amplifier is controlled as with AM.

S18 and S23 close when A1, USB or LSB is switched on. The RC section R62-C23 determines the rise time of the control and the fall time is determined by the network B4/III-B4/IV-T6. B4/III boosts the AF signal and adds a positive DC voltage. GL8 clips the negative half-waves. In the case of slow signal changes, C23 discharges via GL6 and R54 during the negative half-wave.

The rectified AF signal is smoothed by C21. B4/IV boosts the DC voltage obtained and cuts off T6. If the signal changes suddenly by more than 20 dB, for example, during a keying interval with A1, the AF is no longer present at B4/III and C23 cannot discharge via GL6. The control voltage remains unchanged.

Only after R56 has discharged the storage capacitor C21 to below the threshold fixed by R58 and R73 does T6 conduct discharging C23. With A1, S19 switches R57 into circuit shortening the release time constant.

To avoid short pulses affecting the control voltage, a second RC section R63-R66-C23 with a short rise and fall time has been provided.

Fig. 4-11 shows the IF control with a morse code character ("n"). When the carrier is keyed, the control voltage rapidly reaches the required value. During the keying interval between dash and dot, the control voltage remains unchanged. After the dot, it "waits" for further signals to follow and will then again drop very fast.

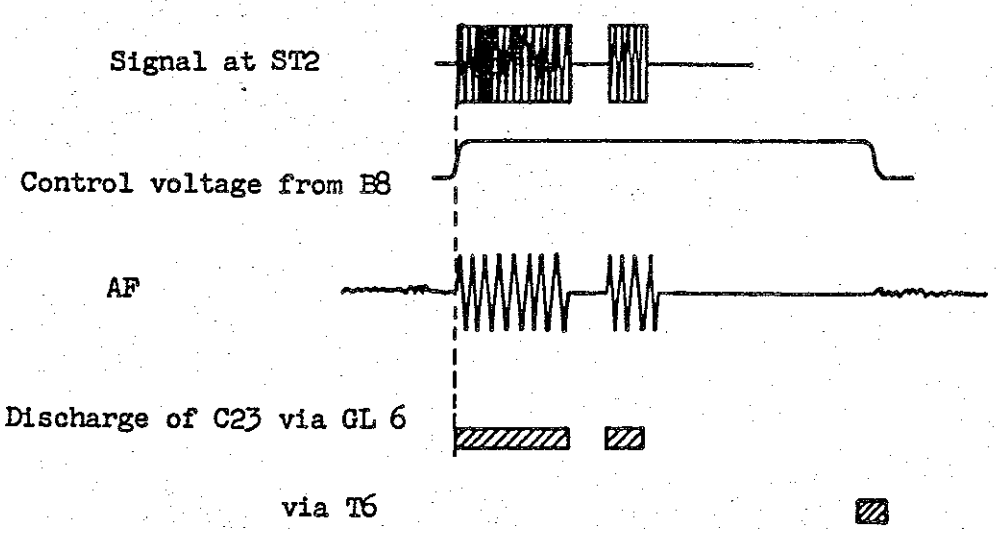


Fig. 4-11 Time function of the control voltage with a morse code character

4.1.10.4 4th Oscillator

The 4th oscillator produces the heterodyne frequency for the product detector with A0, A1, USB and LSB (see 4.1.10.3.2.2) and with 30 kHz ON, it supplies a signal to the 30-kHz output (see 4.1.10.4.5).

The frequencies of the 4th oscillator are as follows:

With	30 kHz ON	30.0 kHz
	A0	30.0 kHz
	A1	31.0 kHz
	USB	31.5 kHz
	LSB	28.5 kHz.

These frequencies are produced by a PLL referenced to a crystal.

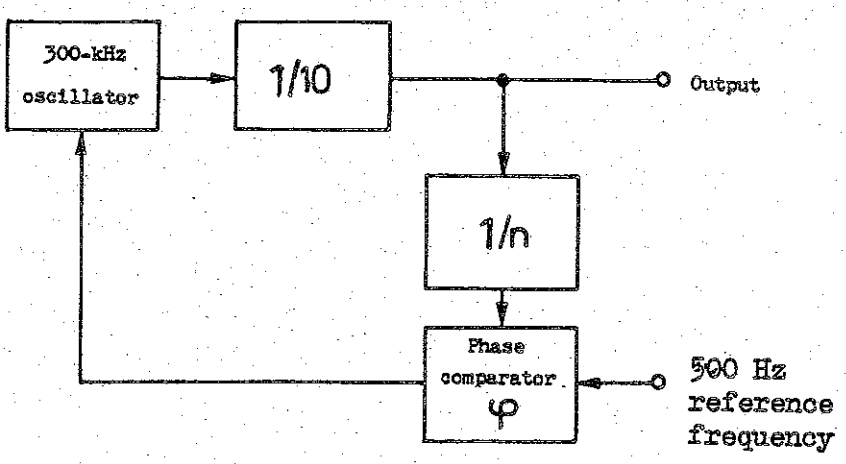


Fig. 4-12 Block diagram of the 4th oscillator

The voltage-controlled oscillator oscillates at approximately 300 kHz. The oscillator output signal is first divided by 10 and then by n, which depends on the desired output frequency. A phase comparator compares the divided signal with the 500-Hz reference frequency and tunes the oscillator to the frequency 10·n·500 Hz.

4.1.10.4.1 Oscillator

T7 is connected up as a 300-kHz Clapp oscillator. It is automatically tuned with GL90. B33 divides by 10 and its output 2 feeds the product detector. Output 14 is taken to the 30-kHz amplifier using T8 (see 4.1.10.4.5) and to the input of the divider B36.

4.1.10.4.2 Adjustable Divider

B36 and B37 form a programmable divide-by-n circuit. n is programmed via the inputs A, B, C, D. According to the formula given above, the division ratios required are 57, 60, 62 and 63. The diodes GL41 to 48 decode the control signals A0, A1, USB, LSB, 30 kHz ON. The logic levels (TTL) at the programming inputs are given in the following table:

Inputs to programmable divider:

	Frequency n kHz		B36 A B C D	B37 A B C D
A0, 30 kHz ON	30.0	60	L L L L (=0)	L H H L (=6)
A1	31.0	62	L H L L (=2)	L H H L (=6)
USB	31.5	63	H H L L (=3)	L H H L (=6)
LSB	28.5	37	H H H L (=7)	H L H L (=5)

Fig. 4-13 shows an example of the timing diagram for an adjustable divider, assuming n = 62.

B36 is BCD-encoded for 2 and B37 is preset to 6. Fig. 4-13 shows the signals at the BCD outputs of the counters. At first they have the preset values. With each positive-going edge of the clock pulse at pin 6 B36 counts down 1. On reaching 0, the "0" output of B36 (pin 12) remains LOW since it is cut off via the CF input (pin 13) which is connected to the "0" output of B37. B36 continues to count down from 0. The positive-going edge at Q4 of B36 switches B37 down by 1.

When B37 finally reaches 0, the "0" output of B37 goes HIGH and the "0" output of B36 is no longer cut off. After B36 has also counted to 0, the "0" output goes HIGH and resets the counter to 62 as it is connected to the Preset Enable inputs (pin 3). The process repeats itself.

To produce a pulse edge at the Preset Enable inputs exactly 62 edges are required at the clock pulse input of B36; i.e. the divider divides by 62 as desired.

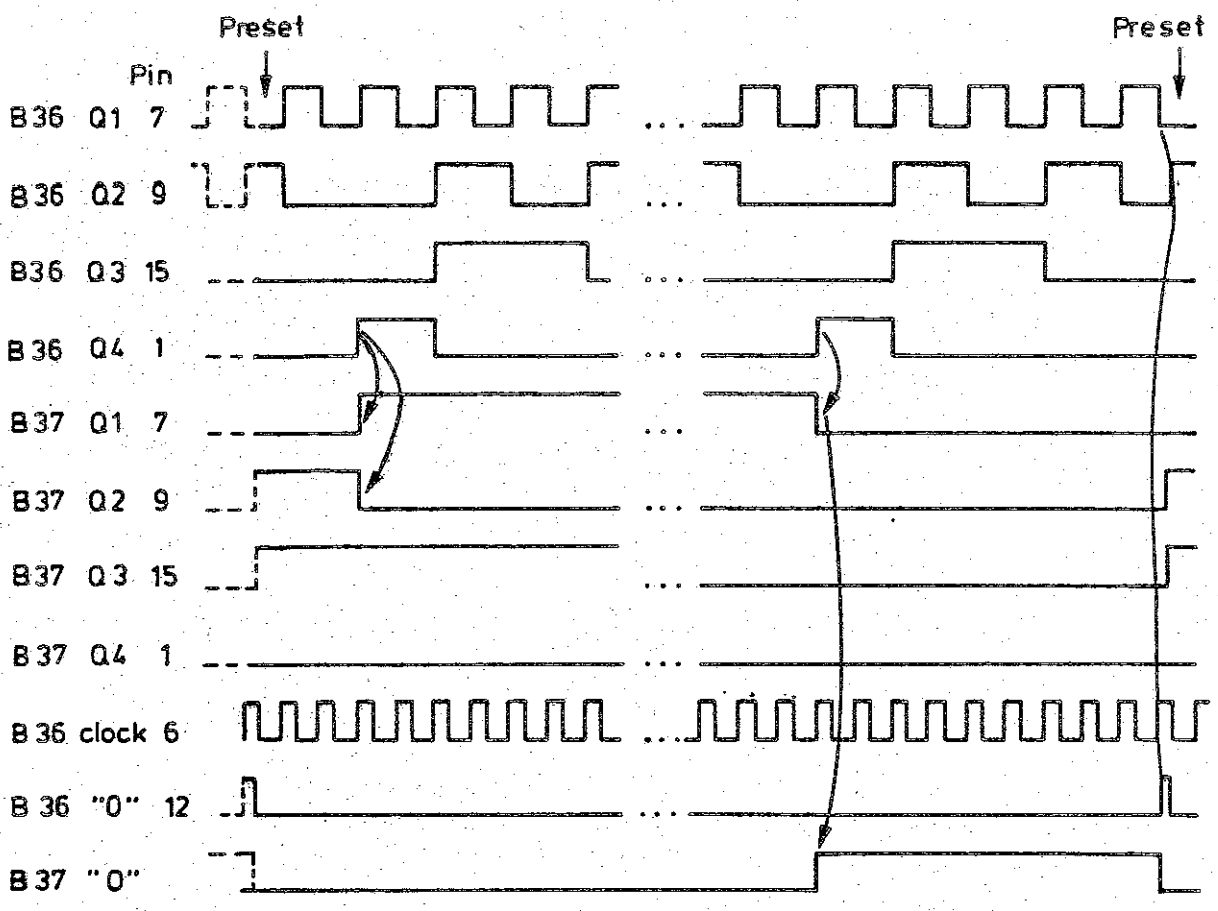
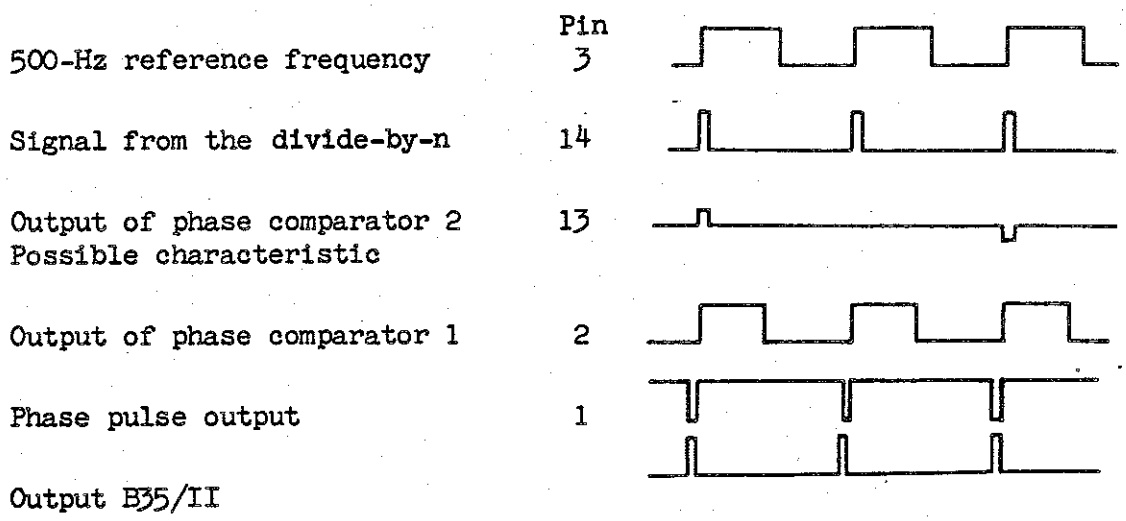


Fig. 4-13 Pulse characteristic with adjustable divider

4.1.10.4.3 Phase Comparator and Synchronization Indication

The phase comparator B34 (MC 14046) compares the divided signal with the 500-Hz reference frequency. The phase comparator 2 used in B34 responds only to pulse edges. Its function is independent of the duty cycle. It synchronizes the oscillator via the active PI (proportional-integral) controller B21.

The phase comparator used produces a phase difference of 0° at the inputs 3 and 14. From the output of the phase comparator 1 (pin 2) and the phase pulse output (pin 1), a signal for synchronization indication is obtained by means of B35/II.



The short peaks at the output of B35/II are smoothed by C121. B35/I functions as an inverter so that, when synchronized, the output of B35/I and, as a result, the Synchronization indication output go HIGH.

4.1.10.4.4 Supply Voltage Switch of the 4th Oscillator

The diodes GL35 to 40 decode the operating modes A0, A1, USB, LSB and 30 kHz ON. If one of them is selected, T6 and T4 connect a supply voltage of +10 V to the 4th oscillator which at all other times is switched off to save power.

4.1.10.4.5 30-kHz Output (ST5)

The 30-kHz output is activated by the controls signals RFM (remote frequency measurement) and 30 kHz ON. The two control signals can never occur at the same time.

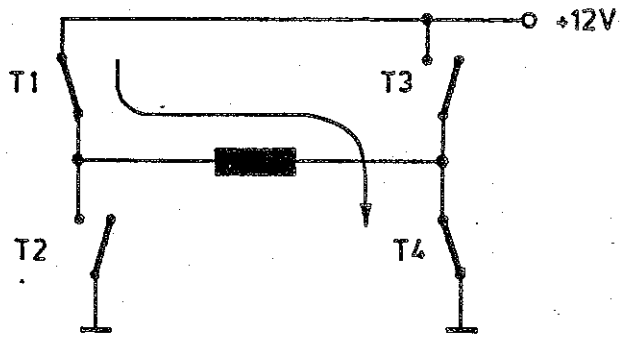
If the RFM input is HIGH, the comparator B21/II causes GL89 to conduct and cuts off GL88. The oscillator signal of the FM demodulator, which is in phase synchronization with the input signal at ST2, is then available at the 30-kHz output (See 4.1.10.3.1).

If RFM is switched to LOW and 30 kHz ON to HIGH, GL88 conducts and GL89 is cut off. The amplifier comprising T8 takes then the 30.0-kHz signal of the 4th oscillator to ST5 (see 4.1.10.4). The level at ST5 is 80 mV_{rms}.

4.1.11 Attenuator Control (Y13)

(See circuit diagram 303.6460 S)

The Attenuator Control design combines high switching speed with minimum power consumption.



Each one of the nine bridge circuits (made up of 4 transistors each) drives one of the solenoids of the RF level switch.

Nine level shifters B14 to B22 match the logic level of the preceding 5-V logic circuit to the 12-V bridge supply.
The logic using the modules B1 to B4 links the attenuation information applied to ST1 in binary code generating the necessary control signals for the level shifters B14 to B21. The monoflops B5 and B6 generate an 18-ms enable signal for the level shifter rendering a switchover of the relays.

The logic levels at the test pins B, C, D, E, F, H, I, K represent the respective nominal switching state of the attenuators. The 4-dB attenuator B22 is normally switched off. Table 5-13 in section 5.3.1.14 shows the relationship between the input levels at ST1.a2, ST1.a2 to 16 and the levels at the test pins. The monostable B5 I (150 ms) which is triggered via differential networks at the control inputs triggers in turn the switching pulse (B6 I = test point G) for switching over the attenuators. Only upon completion of this switching pulse is the new switching state stored in the latches with the clock pulse (B6 II, A).

In automatic operation, the delay is reduced to approximately 1 ms. Monostable B5/II is operative and B5/I is cut off; control line ST1.a3 = HIGH.

Monoflop B7/I ensures that the correct attenuation is connected into circuit at switch-on.

NOTE: When testing the ESH3 with it switched on, the contacts of the Control board must not touch any other potentials since this would immediately overload the unprotected bridge-connected transistors of the Attenuator Control.

4.1.12 Power Supply

(See Circuit Diagram 354.9215 S and Fig. 4-14)

4.1.12.1 Functional Description

The power supply contains the three subassemblies rectifier board, switching power supply and analog power supply, as indicated on the block diagram Fig. 5-1.

The power supply can be operated either with AC line power or with battery power of +24 V with respect to ground. In operation with AC input, a +24-V raw voltage is generated from which the switching and, in part, the analog units produce the required supply voltages for the instrument. An additional supply voltage and two reference voltages are produced for use within the power supply.

4.1.12.2 Rectifier Board

(See Circuit Diagram 355.0011 S)

The power transformer and associated rectifier are mounted directly on the rear panel of the instrument. The 24-V DC output is applied over a short line to charging capacitor C5 on the rectifier board. If the voltage on C5 rises above 40 V, thyristor V10 fires and the AC line is opened. Short noise pulses are limited by V7. The battery voltage is applied via X3, overvoltage being limited by V8 and V9.

The DC output of the power rectifier is passed on for further processing through relay contact k1 when the relay is not energized. The switchover to battery operation occurs only if the AC line voltage is insufficient, a battery voltage of the correct polarity is present, and the instrument is switched on (X4 open).

In case of overvoltage on the +12-V and +5-V supplies, thyristors V3 and V4 shortcircuit these outputs.

The lines into the switching power supply are provided with filters. Furthermore, the analog power supply is connected through 26-pole connector X18 and the loads through two 20-pole connectors X8 and X15. The circuit diagram shows the pin assignment for these connectors from the component side. The board also contains the common neutral X5 of the analog ground lines.

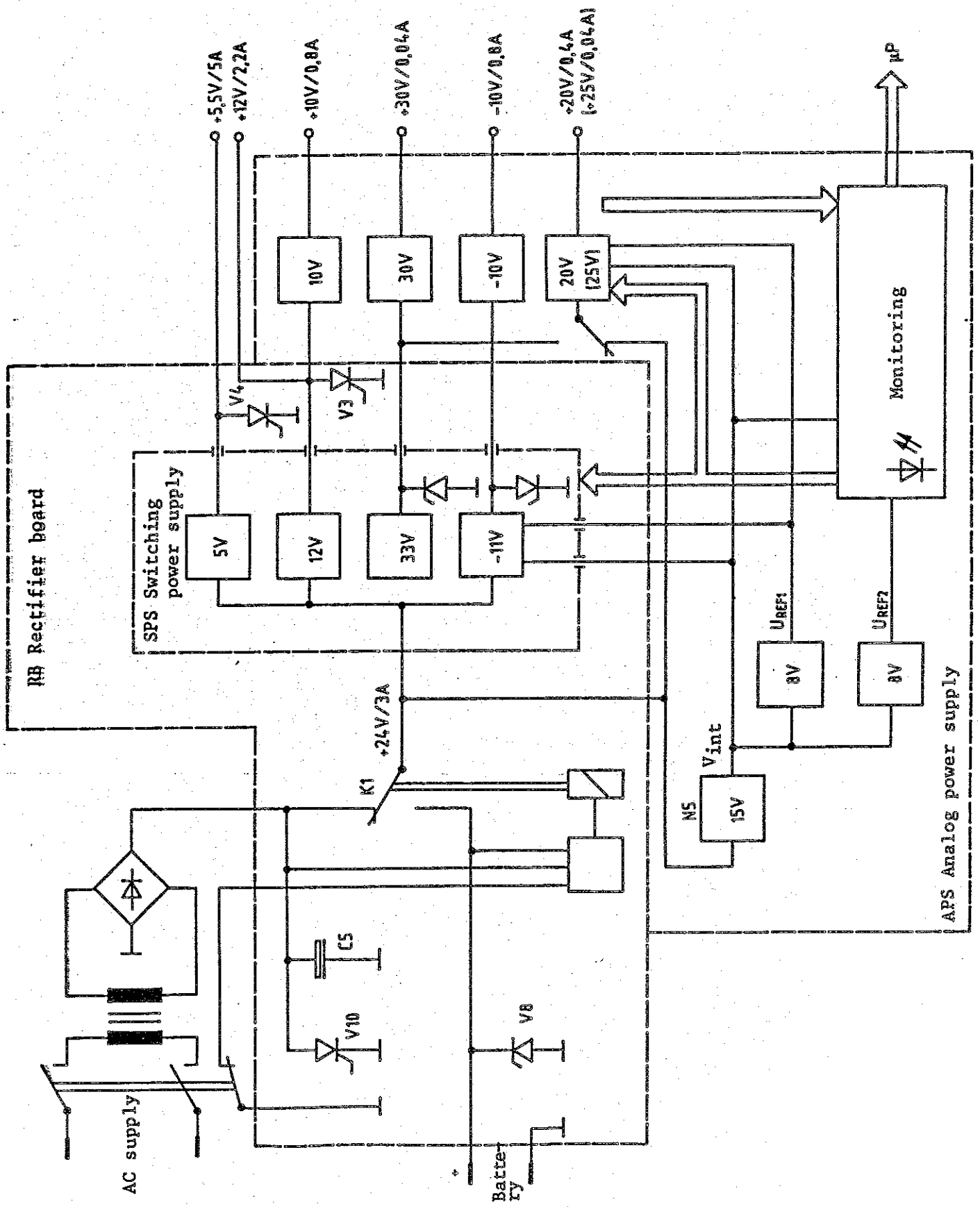


Fig. 4-14 Block diagram of power supply

4.1.12.3 Switching Power Supply

(See Circuit Diagram 354.9515 S)

The switching power supply board is contained in a closed housing to provide RFI shielding. The board generates in three separate switching regulators the output voltages +5 V, +12 and -11 V and +33 V. The regulators operate at a frequency of 200 kHz and are synchronized with each other to prevent beat frequencies.

4.1.12.3.1 Regulators +5 V and +12 V

The +5-V and +12-V circuits are practically the same, so that only the +5-V circuit will be briefly described. It is basically a regulator without transformer.

Transistor V112 is periodically cut in for a fixed time. During this time the current in choke L101 increases slowly from a given initial value. When the transistor is switched off, a slowly decreasing choke current is furnished by the free-running diode V113, so that the voltage across V113 is approximately a rectangular voltage with the amplitude of the input voltage. The duty factor corresponds approximately to the ratio of the output voltage to the input voltage, ignoring losses. A DC current with superimposed ripple flows through L101. Its mean value corresponds to the output current and its AC component is taken up by C118. The output voltage on C118 thus contains only a small ripple. Because of the on-off switching operation, the power loss in the transistor is small. For small duty factors, the loss in the Schottky diode V113 is decisive.

The VMOS transistor V112 requires a positive gate voltage of about 6 V. (A VMOS is used in this position because of the high switching frequency.) The gate voltage is generated by bootstrap circuit C110. When the parallel-connected output transistors of N101 block, V104 conducts and V102 and V112 block. The V112 source voltage is thus slightly negative because of the current voltage of V113, and capacitor C110 is charged via V100 and V101. The maximum voltage is limited by means of V115. In the switch-in phase, transistor V104 is blocked via N101, so that V102 receives base current via R104 and very quickly loads up the V112 gate. When V112 opens, the source potential rises and with it, via C110, the V102 collector voltage.

The pulse width is so regulated by the error amplifier in N101, that the output voltage remains constant. This voltage is furthermore smoothed with an additional LC filter (L102, C120). To assure the stability of the regulation, the varying component of the output voltage is picked off ahead of L102 by C121, whereas the DC component is regulated at the output via R122. The output (pin 9) of the error amplifier is terminated with R109 and C107 for phase compensation. If the potential on this connection drops, the power supply is switched off. This characteristic is used for the switch-on to obtain a soft start-up-capacitor C114 connected via V110 charges up slowly through R112, so that the duty factor increases slowly.

The voltage drop across L102 is used for current limiting. If the drop exceeds the difference input voltage of comparator N100 (set by R114 and R117), C113 discharges and functions similarly to C114 in the start-up circuit.

4.1.12.3.2 Reverse Converter

The third switching regulator functions as a reverse converter in triangle operation and generates the output voltages -11 V and +33 V when power transistor V172 is activated via the push-pull driver V175, V176. The current in the primary winding rises linearly, since no secondary current is flowing. When V172 is switched off, the secondary voltages of transformer V170 are reversed in polarity, so that diodes V173 and V174 become conducting and the output capacitors are charged. During this phase the primary voltage on the V172 drain rises to a value about twice that of the operating voltage. The overshoots, which then occur more frequently, are attenuated by the RCD network on the drain.

Voltage regulation is obtained similarly as for the +5 V and +12 V regulators by means of C185 and R185. The +33-V output is stabilized by the magnetic coupling.

The secondary current limiting is taken from L171 and functions as in the case of the regulators. A current-limiting action is also produced in the primary circuit by means of sensor resistor R177.

4.1.12.4 Analog Power Supply

(See Circuit Diagram 354.9815 S)

The analog power supply furnishes the stabilized +10-V, -10-V, +20/25-V and +30-V supplies as well as the internally used 15-V supply and two 8-V reference voltages. A monitoring circuit generates error signals and the RESET signal for the microprocessor.

4.1.12.4.1 +15-V Supply

This unit containing the integrated regulator N5 generates from the raw 24-V input the 15 V for the circuits of the power supply. The 15-V supply is confined to the power supply and thus is not subject to any external influences.

4.1.12.4.2 +8-V Reference Voltage Sources

Two independent 8-V reference voltages are generated from the +15-V supply with N8 and N9 and temperature-stabilized 6.2-V diodes V30 and V31.
The voltage levels can be adjusted with potentiometers R89 and R95.
Regulator reference V_{REF1} determines the output levels of all analog and switching power supply lines, V_{REF2} is used in monitoring these voltages.
Z-diode V45 prevents any rise in the output voltages in case of a disturbance.

4.1.12.4.3 +10-V/0.8-A Supply

The +10-V supply is obtained from the +12-V output of the switching power supply. Series regulation with collector output permits a slight difference between the input and output voltages. Voltage control is provided by N1III via driver transistor V2. This permits the generation of output voltages higher than the internal supply voltage to the amplifier.

Current limiting with current cutback is provided with sensing resistors R8 and R9 and N1IV, which blocks driver V2 in case of overcurrent. The power supply can also be switched off by an external LOW signal.

To permit use of the +10-V supply as an external voltage reference, the positive sensing lead is separately taken out via X18.16 and is connected to the output lead at the load itself. Resistor R12 prevents an overvoltage in the output in case of a broken sensing line.

4.1.12.4.4 -10-V/0.8-A Supply

This circuit is similar to that of the +10-V supply except for the polarity reversals. The -11-V output of the switching power supply is used as input voltage and for the comparison amplifier. The output of the +10-V supply serves as reference voltage, so that the two voltages are symmetrical. In this case also the sensing lead is taken out separately, via X18.10, to the load. This supply is switched off indirectly via the +10-V supply.

4.1.12.4.5 +20-V/0.4-A (25-V/0.04-A) Supply

This supply is of the same design as the +10-V supply, but, because of the higher output voltage, requires voltage dividers at the input of the current-limiting amplifier N1I. To make this supply usable in other devices, the output voltage and current limiting have been made switch-selectable. In the +20-V setting the supply is driven directly by the raw 24-V voltage, whereas for the +25-V output the +33-V supply of the switching power supply is also used.

4.1.12.4.6 +30-V/0.06-A Supply

In this circuit transistors V16 and V17 form a difference amplifier, V14 is a series transistor and V13 serves for current-limiting. This circuit is supplied from the +33-V output of the switching power supply.

4.1.12.5 Voltage Monitoring

The voltage-monitoring circuit is located on the analog power-supply board. All important supply voltages are constantly monitored in order to inform the user and the microprocessor of any disturbances in operation. Nine LEDs and eight message lines to the microprocessor are provided for this purpose. A green LED is lit to indicate normal status. It is visible from above through the instrument panelling. In case of a failure, the green LED goes out and one or more red LEDs light. If the microprocessor is still functioning, it outputs an error message to the display. Table 5-1 lists the functions of the LEDs (from left to right) and the error codes.

Table 4-4 LED Functions

LED	Designation	Condition signalized	Error code displayed
H2	+24 V	Input undervoltage	-
H1	+15 V	Internal undervoltage	-
H3	+30 V	Voltage outside tolerance limits	ERROR 14
H4	+20/25 V	"	ERROR 13
H5	+12 V	"	ERROR 12
H6	+10 V	"	ERROR 10
H7	-10 V	"	ERROR 11
H8	+5 V	"	-
H9	O.K.		-

4.1.12.5.1 Input Undervoltage

When the raw 24-V supply drops below +21 V, N6II generates a LOW signal, so that red LED H2 lights. A TRAP signal is sent to the microprocessor, via monostable D4I, and initiates a rescue routine. In order to have the +5-V and +12-V supplies available for this routine as long as possible, the -11-V/+33-V switching supply is switched off via output S3 (X18.25) and all analog supplies are switched off via transistor N7III.

Input overvoltages are prevented by circuits on the rectifier board.

4.1.12.5.2 Internal Undervoltage

The internal supply voltage is adequate so long as the input voltage is over 15 V. If the input sinks below this value red LED H1 lights, and the switching power supplies are switched off via S1, S2, S3 and the analog supplies via N7III before their regulators become inoperative.

No message appears on the display, since the required +5-V supply is already switched off.

4.1.12.5.3 Window Comparators

The regulated output voltages, +30 V, +20/25 V, +12 V, +10 V, -10 V, and +5 V, are monitored for over- and undervoltage by means of window comparators (N10, N11, N12). In case of a failure, the green LED H9 goes out and the appropriate red LED H3-H8 lights. The microprocessor receives an ERR INT signal and comparator signal, and generates the corresponding ERROR message for the display. If the 5-V comparator is involved - and only in this case - a RESET is initiated. All supply voltages except the +5-V are shut off in this case.

4.1.12.5.4 Startup and RESET

After the instrument is switched on, RESET is held at LOW via R36 as soon as a very small input voltage is exceeded. All comparators and reference voltages function with the same promptness. With an input voltage over +15 V, the internal supply level is over +13 V, so that S1 goes LOW and the +5-V supply is started up.

As the voltage rises toward its full value, the RESET flip-flop D3 is set via R137 so that RESET remains LOW even when the 5-V comparator switches to HIGH. In this case however N7IV conducts, so that red LED H8 goes out, S2 goes LOW, and the +12-V switching supply makes a soft startup.

When the input voltage has risen to over +22 V, the output of N6II goes high, releasing the third switching supply via S3 and the analog supplies via N7III.

As soon as all voltages lie within their tolerance limits, the D3 output goes LOW and the green LED H9 lights. Monostable D4II is triggered via D3I, and after it resets, the RESET flip-flop is extinguished via C24. The microprocessor is thus activated after a certain delay period during which the voltage for all instrument circuits reach the correct value. Lowpass filter R127, C23 and Schmitt trigger D3II prevent incorrect switching in the transition range of the comparators.

When the 5-V comparator responds, the RESET flip-flop is set via R137 and X14.20 goes low. The power supply thus is restored to its initial state.

4.1.13 Recorder Control

(See circuit diagram 335.9913 S)

This board is used as an interface between the Computer board and the external I/O peripherals.

4.1.13.1 IEC-625 Bus

The IEC-bus socket 1 is connected to the Computer board via ST8. Pin wiring is shown in Fig. 4-14.

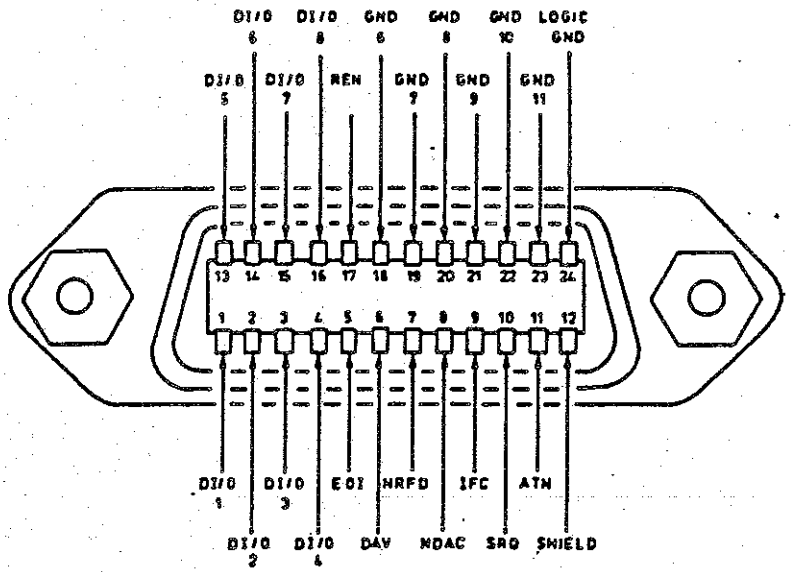
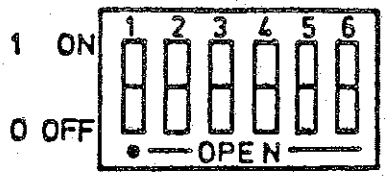


Fig. 4-15 Pin wiring diagram

The IEC-625-bus address can be selected by means of S1 on the rear panel as follows (1-32):

Switch	Value
a1	2^0 = 1
a2	2^1 = 2
a3	2^2 = 4
a4	2^3 = 8
a5	2^4 = 16



The ESH 3 is factory-adjusted to address 17.

4.1.13.2 Recorder Outputs

The recorder outputs can be derived via the 24-way female connector BU2 on the rear panel.

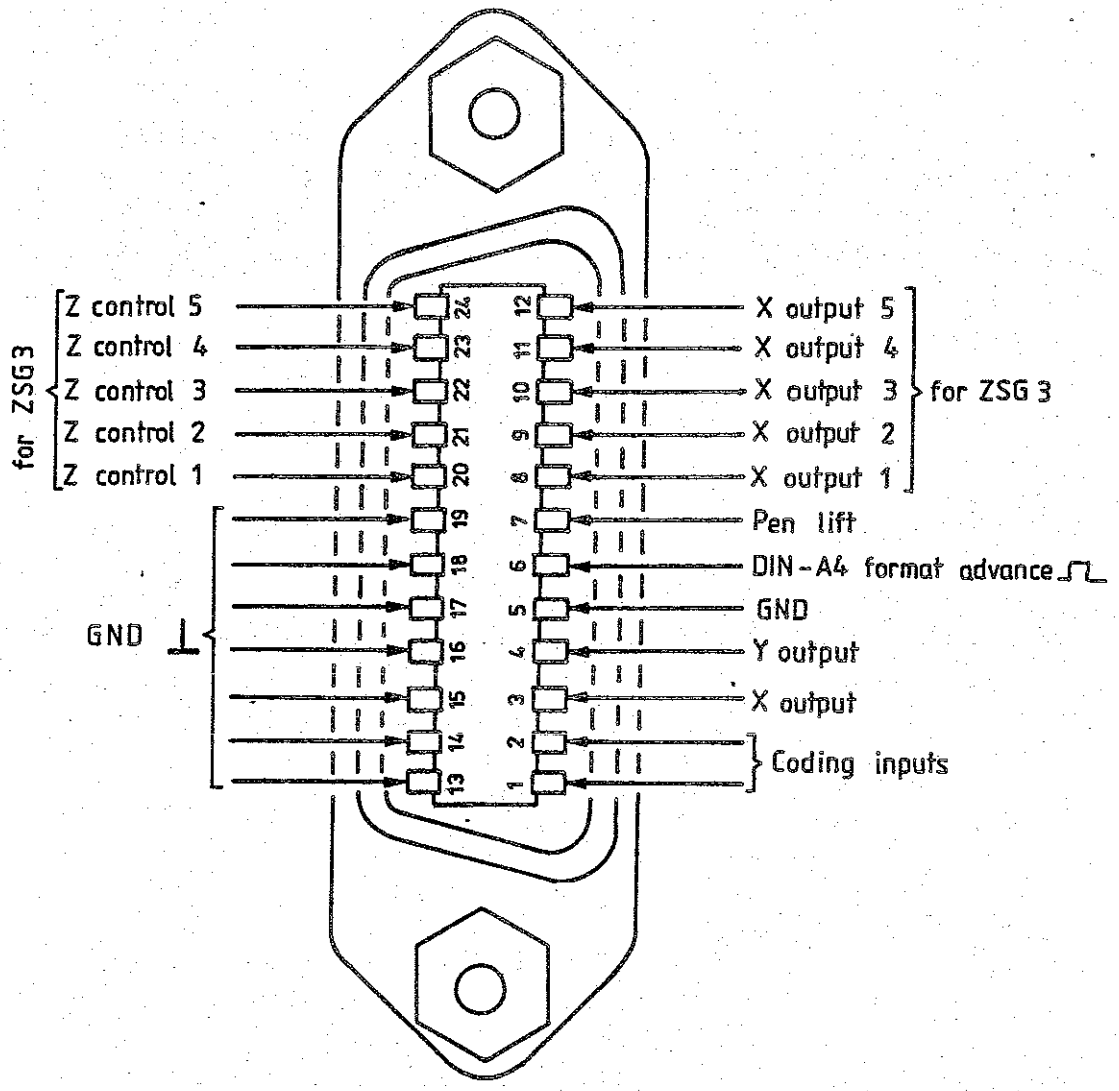


Fig. 4-16 Pin allocation of BU2

The coding lines BU2/pins 1 and 2 supply the information to the µP in the ESH 3 as to whether a recorder and if so, which type of recorder is connected.

Table 4-5 BU2

Pin 1	Pin 2	
N/C	N/C	No recorder connected
To ground	N/C	YT recorder (ZKT)
N/C	To ground	XY recorder (ZSK 2, ZSKT)
To ground	To ground	Radiomonitoring Recorder ZSG 3

The analog X signal is demultiplexed for the Radiomonitoring Recorder ZSG 3 by B1 (which converts from BCD to 1-out-of-5), which controls via level shifter B2, the CMOS switches B3/B4 (+12 V = on). The outputs are converted to low impedance via B5/B6 (I_{max} < 1 mA). B7 controls the pen lift for each channel (HIGH = Pen up).

S2 permits switching over between internal and external reference (5 MHz or 10 MHz).

The recorder control circuit is powered via ST3.

4.1.14 Attenuator (Y16)

(See circuit diagram 302.2813 S)

The Attenuator consists of a base plate on which the attenuator pads are mounted, the drive system comprising the switching contacts and a control board. Ten transmission line sections, eight attenuator pads and an input for the calibration voltage of the ESH 3 are soldered onto the base plate which is made of copper for improved heat dissipation. The transmission lines and attenuator pads are of thin-film design, using a ceramic substrate. The 1- and 4-dB steps are arranged in a T; a π-arrangement is used for the 10- and 20-dB steps and a dual π-arrangement for the 40-dB steps. The contacts of the attenuator pads and transmission lines are gold-plated for enhanced switching reliability and life expectancy. The drive system for switching over the contacts contains 9 rocker switches which are switched over by means of solenoids and kept in the final position by means of permanent magnets. Each of these rocker switches controls three switching contacts, of which one alternately interconnects the transmission lines and the other two switch the associated attenuator pad into circuit. High contact force (0.2 N) ensures reliable contacts.

4.1.15 Motherboard

The Motherboard is used for electrically connecting all the boards plugged in directly or indirectly. The circuit diagram of this board is on 335.8017 S, sheet 1.

4.2 Mechanical Construction

The ESH 3 comes as a 19" unit, 4 dimensional units in height.

To open the receiver, loosen the four Phillips type screws on the two side panels. Remove the top and bottom panels thus gaining access to screening panels which can be unscrewed.

After these panels have been removed, all the boards are freely accessible. The overall AF wiring of the plug-in boards is accomplished via the Motherboard. On account of the stringent RF shielding requirements, RF wiring is accomplished via coaxial Subminax screw-in connectors.

The front panel and the Display Unit (Y1) + Computer board (Y2) form a mechanical unit which can be removed by undoing 4 screws. After unplugging the cables, the front panel unit can be completely dismantled. The RF-shielded boards can be removed in two simple steps:

- Undo the coaxial connections on the underside of the board.
- Press board from below to unplug.

The Attenuator (Y16) is screwed down on the frame and can be removed only after undoing these screws.

Use of plug-in boards throughout and avoidance of solder connections between the individual boards makes for optimum serviceability as all the boards can be dismantled and repaired quickly with a minimum of tools.

4.3 Arrangement of the Boards

(See Fig. 4-16 (top view of receiver) and maintenance instructions on the inside of the shielding of the ESH 3)

Legend for Fig. 4-16

Board	Designation	Ident. No.
Y1	Display Unit	335.8400 S
Y2	Computer Board	335.8800 S
Y3	Analog Circuit	336.0710 S
Y4	Synthesizer 2	303.7850 S
Y5	Synthesizer 1	303.7715 S
Y6	Filter Control	303.7915 S
Y7	Filter 1	303.7015 S
Y8	Filter 2	303.7415 S
Y9	Mixers 1 and 2	303.6019 S
Y10	Calibration Generator	303.6319 S
Y11	Mixer 3	303.6219 S
Y12	Indication and AF Demodulation	303.6919 S
Y13	Attenuator Control	303.6460 S
Y16	Attenuator	303.2813 S
Y20	Power Supply	303.3210 S
Y21	Memory Board	336.0778 S

4.4 Location of Trimming Components

Board	Reference No.	Function
Y1	R1	Zero adjustment of analog frequency offset indication
	R47	Intensity of upper LED array, analog level indication
	R51	Zero adjustment of analog level indication
Y2	R5	A/D converter adjustment: full-scale deflection
	R6	A/D converter: reference voltage
	R12	Sample/hold amplifier offset
Y3	R33	Frequency offset (gain)
	R37	Offset } Logarithmic converter for
	R40	Gain } 20-dB analog indication
	R98	Offset mod. depth and Δf (-)
	R99	Offset mod. depth and Δf (+)
	R111	Frequency correction
Y4	L4	Frequency of 2nd oscillator
	L21, C42	Characteristic of 100-Hz loop
	L68	Frequency of reference oscillator
Y5	L12, C3	Characteristic of 75-to-85-MHz osc.
	L13, C13	Characteristic of 85-to-95-MHz osc.
	L14, C23	Characteristic of 95-to-105-MHz osc.
Y6	R58, R70, R79, R92, R106	Tuning voltage of RF filters 15 and 16
Y7	-	
Y8	L79, L78 C162, C164	Adjustment of tracking of RF filter 16
Y9	R63, C53, C56	Gain and ripple, 500 Hz
	R69, C64, C67	Gain and ripple, 2.4 kHz
	R76	Gain and ripple, 10 kHz

Board	Reference No.	Function
Y10	R84	Level of sinewave generator
	R110	Calibration correction
	C90	Frequency response
	R91	Adjustment of pulse width for f > 150 kHz (CISPR 1)
	R89	Adjustment of pulse width for f < 150 kHz (CISPR 3)
	R77	TC correction for sinewave generator (do not change setting)
Y11	C4	Frequency 3rd oscillator
	R20	Gain 30 kHz
	R102	Gain 200-Hz bandwidth
Y12	R139	Gain of log amplifier with LOG 40 dB
	R142	Gain of log amplifier with LOG 60 dB
	R164	Adjustment of linearity of B14
	R174	Adjustment of linearity of B15
	R177	Zeroing of B16
	R182	Adjustment of gain of B16
	R186	Compensation DC voltage with LOG 40 dB
	R188	Compensation DC voltage with LOG 60 dB
	R195	Zeroing of B17
	R198	Adjustment of gain of B17
	R19	Adjustment of centre frequency of PLL demodulator
Y20	R26	Adjustment of 10.00-V reference voltage

5. Repair

5.1 Measuring Instruments and Auxiliary Equipment Required

The measuring instruments and auxiliary equipment required are listed in Table 5-17.

5.2 Failure Location

In the following test, instructions are given for locating typical possible trouble sources. See also section 2.3.20 which describes the error messages that can be produced by the software of the Test Receiver ESH 3 when it identifies certain trouble sources.

Section 5.3 contains adjustment procedures and instructions for checking the various boards. For checking the performance specifications of the receiver refer to section 3.

5.2.1 No Response at Switch-on or Readout Makes no Sense

a) Failure symptoms:

At switch-on, the 13-digit display, frequency indication, RF attenuation and demodulator operating range indication, the analog indication and the individual LEDs associated with the device functions do not light up, the readouts obtained make no sense or there are combinations that make no sense, or there is no response to the push of a key.

b) Locating the fault:

- Check the LEDs which monitor the supply voltages of the Analog Power Supply.
- Check the following plug-and-socket connections:
  ST9 (Computer board/Analog Power Supply),
  BU3 (Computer board/Display Unit) and
  ST15 (Motherboard/Analog Power Supply)
  BU4/ST3 (Computer board/Memory board).
- Check the voltage on the Computer board:

ST9	3a,b/4a,b/5b	5 V ±5%
ST9	6a,b	+12.0 V
ST9	7a	+10.0 V
ST9	7b	-10.0 V

- Check the voltage on the Display Unit:

ST3	9 to 13	+5 V
ST3	14	-10 V
ST3	15 to 16	+12 V

- Check the links B1 to B5 on the Computer board and the shorting link ST1 on the Display Unit.

- Check the microprocessor on the Computer board:

RESET input	ST16/3 and B2/36	HIGH potential
CLOCK output	B2/37	3-MHz TTL level
RD and WR outputs	B2/32 and B2/31	Pulses, depending on program

and carry out signature analysis testing as described in 5.3.1.2.

- Check the microprocessor on the Display Unit:

RESET input	ST2/7 and B67/4	HIGH potential
PROG. input	B67/25	Pulses depending on program

and carry out signature analysis testing as described in 5.3.1.1.

5.2.2 Receiver Fails to Self-calibrate

a) Failure symptom:
After the CAL. button 15 has been pressed, the calibration process is interrupted by an error message (time exceeded).

b) Locating the fault:

Settings on the ESH 3: Indicating mode 35 : AV.
Operating range 33 : 20 dB

The supply voltages and 500-Hz and 100-kHz reference frequencies must be checked.

- Check the level and the frequency in the TWOPORT mode 38.
  Level into 50 Ω ..... -27 dBm ±1 dB

- Check the level and the frequencies at the four inputs of the calibration generator Y10 as follows:

Inputs:

ST4:	31.5 kHz 31.0 kHz (depending on demod. mode) ...	-15 dBm (±1 dB)
	30.0 kHz 28.5 kHz	
ST5:	8.97 MHz	-13 dBm (±1 dB)
ST6:	66.0015 MHz 66.0000 MHz	-15 dBm (±1 dB)
	65.9985 MHz	
ST3:	Receiver frequency +75 MHz	-15 dBm (±1 dB)

Outputs:

ST2:	Receiver frequency	-27 dBm (±0.3 dB)
ST1:	Receiver frequency	-67 dBm (±0.3 dB)

- Connect RF socket 45 to GEN. socket 44 with a BNC cable. Set RF attenuation 40, 41 to 10 dB:

Attenuator (Y16)	BU2	-37 dBm (±1 dB)
Filter 2 (Y8)	ST8	-38 dBm (±1 dB)
Mixers 1/2 (Y9)	ST7	-2 dBm (±3 dB)

- Set RF attenuation and IF attenuation 40, 41 to 50 dB and 40 dB, respectively.

  RF level at ST5 of Mixer 3 (Y11) ..... -22 dBm (±3 dB)

- Voltage on pin ST1/a2 of the Indication and AF Demodulation board (Y12) ..... +1 to +2 V

The analog level indication 14 must give about full-scale deflection (right-hand scale end).

If not, the fault is in the AGC amplifier of the Analog Circuit (Y3) or in the Mixer 3 (Y11).

5.2.3 Receiver Self-calibrates but Indication Incorrect in AV. Mode

Settings on the ESH 3: Operating mode 38 : TWOPORT.
All other settings same as under 5.2.2.

Level at BU2 of the Attenuator Y16 ..... -67 dB ±0.3 dB

The fault is in the feedback amplifier on the Analog Circuit board (Y3) (reference).

5.2.4 Receiver Self-calibrates but Indication Incorrect in CISPR Mode

Apply 2 mV EMF at receive frequency.

Level indication 13 ..... 60 dBµV

If the indication is incorrect, check the following functions:

- Demodulation and weighting of the indicated signal on the Indication and AF Demod. board (Y12).
- IF bandwidths of Mixer 3 (Y11) and Mixers 1 and 2 (Y9).
- Calibration pulses produced by the Calibration Generator (Y10).

If the indication is correct, check the IF bandwidths of Mixer 3 (Y11) and Mixers 1 and 2 (Y9).

5.2.5 Error Messages of ESH3 and Possible Causes

ERROR 01

The frequency entered is too high (> 30 MHz).
→ Operating error

ERROR 02

The frequency entered is too low (< 0.009 MHz).
→ Operating error

ERROR 03

The error 03 may occur during the brief calibration if the overall gain of the receiver deviates by more than 0.5 dB from the value determined in the course of the last total calibration. By this error message the user is requested to carry out a total calibration. The message does not implicate a device error.

ERROR 05

Level calibration at 1 MHz during the brief or total calibration cannot be terminated within the internally fixed time (deviation from nominal value: >6 dB).

Possible causes:

→ Error of calibration generator. Check as described in sections 5.3.1.10 and 5.2.2.
→ Error in signal path. Check as described in 5.2.2.

ERROR 07

This error may occur during total calibration. The error message informs the user of a correction value exceeding the specified tolerance. If level calibration at 1 MHz is not possible, the ERROR 05 message appears.

During calibration in the Talk-only mode, all correction values can be output to a printer via the IEC bus (printer address: Listen Only). All correction factors up to the last valid value are printed out before the calibration is aborted, thus enabling the user to find the cause of error.

Separated by a blank line, the correction values are printed out in the following sequence:

- Correction values for gain at the different bandwidths and correction values for CISPR 1 (f > 150 kHz) and CISPR 3 (f < 150 kHz; altogether 4 values):
  2.4 kHz,
  500 Hz (1 kHz for model 56),
  200 Hz,
  CISPR 1
  CISPR 3

- Linearity correction values for 20-dB operating range
  (3 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- Linearity correction values for 40-dB operating range
  (5 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- Linearity correction values for 60-dB operating range
  (7 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- MIL correction value for 10-kHz IF bandwidth
  (1 value; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 4 dB).

- Frequency-response correction values (for frequency and level)
  With a deviation of > 6 dB from the nominal value (= 0 dB), the calibration is aborted; if the deviation is > 4 dB, the indication flashes.

In case of aborted calibration, proceed as follows to find the cause:

If an appropriate printer is not available, the source of error can be found by observing the calibration process.

If ERROR 07 occurs at the beginning of the calibration (receiver at 1 MHz), carry out the following tests:

▶ **Check the calibration generator:**

Settings on the ESH 3: Frequency 1: MHz
Generator: ON

Connect a power meter to the generator output.
→ Level at generator output: -27 dBm ± 0.3 dB

If an error has been found, check the calibration generator as described in section 5.3.1.10.2.

▶ **Check the gain at all IF bandwidths:**

Settings on the ESH 3: Frequency: 1 MHz
Generator: ON

Connect the generator output to the RF input using a short BNC cable.
→ Select the IF bandwidths successively. The level indication is 0 ± 6 dB at every IF bandwidth (abort criterion; ideal value < ± 2 dB).

In case of an error, check the 1st + 2nd mixer PCB (5.3.1.9.5 to 5.3.1.9.8) and the 3rd mixer PCB (5.3.1.11.8).

- **Check the CISPR indication:**

Settings on the ESH 3: Frequency: 1 MHz
Generator: OFF
Indication mode: CISPR
RF attenuation: 40 dB
IF attenuation: 30 dB

Apply a sinewave signal (1 MHz, 60 dBµV) to the RF input.

→ The receiver indicates 60 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).
Apply the CISPR-1 standard pulse (100-Hz pulse frequency) to the RF input (see 3.2.1.4).
→ The receiver indicates 60 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

Set the frequency to 100 kHz and the RF attenuation to 20 dB.
Apply a sinewave signal (100 kHz, 40 dBµV) to the RF input.
→ The receiver indicates 40 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

Apply the CISPR-3 standard pulse (25-Hz pulse frequency) to the RF input (see 3.2.1.3).
→ The receiver indicates 40 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

- **Check the indication linearity:**

Settings on the ESH 3: Frequency: 1 MHz
IF attenuation: 40 dB
RF attenuation: 50 dB
IF bandwidth: 200 Hz
Indication range: 20 dB

Increase RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max.
(abort criterion; ideal value < 1 dB).

Select 30-dB RF attenuation and 40-dB indication range.
Increase RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max.
(abort criterion; ideal value < 3 dB).

Select 10-dB RF attenuation and 60-dB indication range.
Inrease RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max.
(abort criterion; ideal value < 3 dB).

In case of an error, check the indication section on the indication and AF demodulation PCB as described in 5.3.1.12.2.

When the calibration is aborted while the frequency response is measured, check the preselection filter on the filter 1 or filter 2 PCB, depending on which filter is in circuit when the abort occurs. The cut-off frequencies of the filters are specified in Tables 5-2 (section 5.3.1.7) and 5-3 (section 5.3.1.8). Check according to 5.3.1.7 and 5.3.1.8.

If no error is found in the input filters, check the oscillator level at input ST3 (X3) of the 1st + 2nd mixer PCB (nominal value: + 23 dBm ± 2 dB).

ERROR 08:

The memory register called up with RCL is not occupied.
→ Operating error

Voltage supply errors:

ERROR 10:

Error in + 10-V supply. The voltage is either not available or not within tolerance. The + 10-V LED on the power supply lights.
→ Remove power connector from motherboard. If the + 10-V LED goes out, one of the PCBs is faulty, if it remains lit, trace the error in the power supply.
→ In case of a PCB error, remove the PCBs one after the other until the error has disappeared.

ERROR 11:

Error in -10-V supply. The voltage is either not available or not within tolerance. The -10-V LED on the power supply lights.
→ Trouble-shooting analogous to that of ERROR 10.

ERROR 12:

Error in + 12-V supply. The voltage is either not available or not within tolerance. The + 12-V LED on the power supply lights.
→ Trouble-shooting analogous to that of ERROR 10.

ERROR 13:

Error in + 25-V supply. The voltage is either not available or not within tolerance.
→ Power consumption too high or short circuit on one of the PCBs
synthesizer 1,
synthesizer 2,
mixers 1 + 2 or
analog circuit.
→ Error in power supply.
Remove the PCBs one after the other until the error has disappeared.

ERROR 14:

Error in +30-V supply. The voltage is either not available or not within tolerance.
→ Power consumption too high or short circuit of filter control PCB.
→ Error in power supply.

ERROR 20 to ERROR 41:

These errors are operating errors. They are defined in Table 2-6 of the ESH 3 Operating Manual.

Synthesizer errors:

ERROR 51:

The 1st oscillator (75 to 105 MHz) on the synthesizer 1 PCB does not lock.

Trouble-shooting:

- Check 65-to-65.1-MHz, -16 ±2-dBm signal at ST2.
- Check 100-kHz reference at ST1.b18 (TTL level).
- Check 65-MHz amplifier on synthesizer 1 PCB according to section 5.3.1.5.4.
- Check 10-to-40-MHz amplifier on synthesizer 1 PCB according to section 5.3.1.5.5.
- Check the oscillators according to section 5.3.1.5.

ERROR 52:

The 50-to-51-MHz interpolation oscillator on the synthesizer 2 PCB does not lock.

Trouble-shooting:

- Check setting of int./ext. reference switch on rear panel of receiver.
- Check reference oscillator of synthesizer 2 according to section 5.3.1.4.2.
- Check 50-to-51-MHz oscillator according to section 5.3.1.4.3.

ERROR 53:

The 2nd oscillator (66 MHz) on the synthesizer 2 PCB does not lock.

Trouble-shooting:

- Check int./ext. reference switch on rear panel.
- Check reference oscillator of synthesizer 2 according to section 5.3.1.4.2.
- Check 66-MHz oscillator of synthesizer 2 according to section 5.3.1.4.4.

ERROR 54:

The 3rd oscillator (8.97 MHz) on the mixer 3 PCB does not lock.

Trouble-shooting:

- Check 500-Hz reference at ST1.b1 of 3rd mixer. In case of error, check synthesizer 2.
- Check 8.97-MHz oscillator of 3rd mixer according to section 5.3.1.11.2.

ERROR 55:

The 30-kHz oscillator on indication and AF demodulation PCB does not lock.

Trouble-shooting:

- Check 500-Hz reference at ST1.ab1 of indication and AF demodulation PCB. In case of error, check synthesizer 2.
- Check 30-kHz oscillator on indication and AF demodulation PCB according to section 5.3.1.12.2 h.

Several errors at a time:

If several error messages appear at the same time, they generally have a common source. The following table lists the secondary errors occurring as a result of synthesizer errors.

Source	Secondary error
Reference oscillator not available	ERROR 51, 52, 53, 54, 55
ERROR 51	-
ERROR 52	ERROR 51, 53
ERROR 53	-
ERROR 54	-
ERROR 55	-

Table 2-6 Error code list

01	Frequency entered above limit
02	Frequency entered below limit
03	CAL:CHECK Comparison frequency response correction/ current value ≥ 0.5 dB, occurs after an aborted total calibration, for example.
04	No listener on IEC bus (fault in IEC-bus controller)
05	Level or offset calibration is not accomplished within fixed time (hardware error)
07	Correction value at CAL. TOTAL > 6 dB; total calibration aborted.
08	Memory register not occupied on RCL
10 11 12 13 13	+10 V -10 V +12 V +25 V +30 V Failure of a supply voltage (the failure of the +5-V supply voltage is not indicated)
20 21 22 23 24 25	Current register Register 1 Register 2 Register 3 Register 4 Register 5 At start of automatic frequency scan, one or more values are not defined.
30 31	START frequency > STOP frequency START frequency = STOP frequency and XY recorder or ZSG 3 connected
32	MAX. PEGEL ≤ MIN. PEGEL
33	SPEC.FUNC. 61 X axis logarithmic and fstop : fstart < 1.4
40	ZSG 3 error: Error message if SPEC.FUNC. 61 is selected for SCAN RUN with ZSG 3
51	Synthesizer 1: 1st oscillator has not locked
52	Synthesizer 2: 50-to-51-MHz oscillator has not locked
53	Synthesizer 2: 2nd oscillator has not locked
54	Mixer 3: 3rd oscillator has not locked
55	Indication and AF demodulation: 30-kHz oscillator has not locked

5.3 Adjustment and Performance Check of the ESH 3

5.3.1 Adjustment of the Various Boards

To facilitate measurements on and adjustment of the boards normally plugged directly into the motherboard of the ESH 3, Rohde & Schwarz supply the Service Unit ESH2-Z7 (IN 338.4112) which permits operation of these boards outside of the receiver.

5.3.1.1 Display Unit

5.3.1.1.1 Supply Voltages

Pin	Voltage	Current
ST3.1 to .7	Ground	-
ST3.9 to .13	+5 V	max. 2 A
ST3.15 to .16	+12 V	approx. 50 mA
ST3.14	-10 V	approx. -10 mA

5.3.1.1.2 Frequency Indication

- Enter BCD-coded frequency information at ST1.1 to ST1.23.
- Check the resulting frequency indication (B18-B23).

5.3.1.1.3 Analog Level Indication

- Apply analog voltage GND to ST3.8 and 0.355 V to 3.55 V to ST2.12.
- Adjust R51
  for the first (left-hand) LED (GL40) to light up at 0.355 V and
  the last (right-hand) LED (GL43) to light up at 3.55 V.
- Adjust R47
  until the intensity of the right-hand LED array (GL42, GL43) is the same as that of the left-hand LED array (GL40, GL41).
- Apply a logic L to ST1.4 and ST2.8 and check the MIN. LED (GL38) and the MAX. LED (GL39) respectively.

5.3.1.1.4 Analog Offset Indication

- Apply analog voltage GND to ST3.8 and 1.0 V to 4.0 V to ST1.24.
- Adjust R1
  for the two centre LEDs (GL44, GL45) to light up at 2.5 V.
- Apply a logic L to ST1.16 and check the FREQUENCY OFFSET LED (GL88).

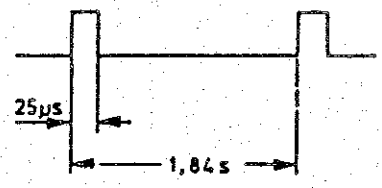
5.3.1.1.5 Signature Analysis

The microcomputer B67 contains a signature analysis program which can be activated by changing the connection of the link ST4, and which permits checking the digital driving circuit for the 5 x 7 dot matrices and all

the LEDs which indicate the device settings. First check visually that all the LEDs and dot matrices light up.

To do so:

- Change the connection of link ST4.
- Reset the processor B67 by momentarily connecting ST7.1 to ground.
- Check the clock pulses at ST7.3:



- Connect the signature analyzer to ST5 and set as follows:

  START: " ⌐‾_ "

  STOP: " ⌐‾_ "

  CLOCK: " ⌐‾_ "

  Subsequently check the board against the above diagram and signature analysis table.

5.3.1.1.6 Keyboard and Display Interface

The keyboard and display chip B61, which is a self-contained unit, is driven directly from the main processor on the Computer board and is covered by the test and signature analysis of the latter. The test is therefore carried out in conjunction with the Computer board and the relevant signature analysis table (section 5.3.1.2.2.1).

5.3.1.1.7 Difference Current Sink

- Switch on signature analysis in accordance with 5.3.1.1.5 (all the LEDs and dot matrices light up).
- Connect oscilloscope to ST3.1 to 7 (GND) and ST3.9 to 13 (+5 V) and watch screen display.

5.3.1.2 Computer Board

5.3.1.2.1 Supply Voltages

Pin		Voltage	Current
ST9	1a/1b/2a/2b	Ground	-
ST9	3a/3b/4a/4b/5a	+5 V	approx. 2 A
ST9	6a/6b	+12 V	approx. 50 mA
ST9	7a	+10 V	approx. 100 mA
ST9	7b	-10 V	approx. 100 mA

5.3.1.2.2 Signature Analysis

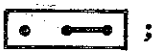
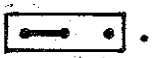
Free-running and software-driven signature analysis is used in fault location when testing the Computer board, which constitutes a complex digital system. With free-running signature analysis, the processor must cyclically scan its entire address range, and the start/stop signal for the signature analyzer originates directly from the address bus.

With software-driven signature analysis, a cyclic control program for all the peripheral chips is stored in the EPROMs, making for more thorough individual testing.

5.3.1.2.2.1 Free-running Signature Analysis

An initial but effective test of the Computer board can be carried out using free-running signature analysis. In this signature analysis mode, the feedback between the processor and the EPROMs memory is interrupted (bus driver B6), and driver B83 is activated, which produces a NOP instruction in every read cycle of the processor. The signatures are used for checking the processor and the EPROMs as well as the driver chips and the address decoder chips.

Settings and checks:

- To select the free-running mode, change over the connection of the links BR2 and BR5 to the position shown: BR2  ; BR5  .
- Reset the processor by: momentarily applying a logic L to ST16.2 (normally at H level); or switching the unit off.
- Check the CLOCK output B2.37 of the processor:
  3-MHz clock signal at TTL level.

- Check the signatures of the address bus.

- Connect the signature analyzer to ST14.

  Settings on the 5004A:

  START ⌐¯|_ , STOP ⌐¯|_ , CLOCK ⌐¯|_

  Signatures B2.21 to B2.28 (≙ A8 to A15) and B5.4,
  B5.6 to B5.21 (≙ A0 to A7):

A0	UUUU	A8	HC89
A1	5555	A9	2H70
A2	CCCC	A10	HPP0
A3	7F7F	A11	1293
A4	5H21	A12	HAP7
A5	OAFA	A13	3C96
A6	UPFH	A14	3827
A7	52F8	A15	755U

  Check these signatures on the chips B1, B4, B7 as well as on the EPROMs B8, B11, B14, B15 and the socket BU4 on the Memory board.

- Check the signatures of the data bus.
  Connect signature analyzer to ST13 (contents of EPROMs).

  Settings on the 5004A:

  START ⌐¯|_ , STOP ⌐¯|_ , CLOCK _|¯⌐

All the signatures are listed in the table given in the Appendix.
After the test has been accomplished, reconnect the links BR2 and BR5 in the original positions.

5.3.1.2.2.2 Software-driven Signature Analysis

The next step in testing the Computer board is a special test program provided in the EPROMs:

- Change the connection of link BR1.

- Reset the processor by momentarily applying a logic L to ST16.3.

- Check the signatures of the peripheral chips against the table given in section 5.3.1.2.2.1.

- Check the staircase signals (0 V to +10 V) at the two D/A converter outputs via B41, on the oscilloscope.

After the test has been accomplished, reconnect the link BR1 in the original position.

5.3.1.2.3 A/D Converter

All the voltages to be measured or applied are with respect to ST9.10b.

A special test routine of the processor software can be used for adjustment of the A/D converter B26, B27. For this purpose, EPROMs B8, B11, B14, B15 must be fitted, and the Memory board must be connected to BU4, just as for the signature analysis.

By changing the connection of the link BR6 and resetting the processor (logic L at ST16.3), the A/D converter continually receives start-of-conversion pulses, and its output is continuously read out.

- Adjust the reference voltage at MP3 to +5.000 V (±1 mV) by means of R6.
- Adjust the sample/hold amplifier B77:
  Connect the sample/hold input ST5.22 to ST9.10b. Adjust the voltage at MP6 to 0 V (±1 mV) by means of R12.
- Adjust the A/D converter B26:
  Apply a voltage of +5.000 V (±1 mV) to input ST5.22. Adjust the gain of the A/D converter by means of R5 such that the logic level at B30.1 is just at the switching point between H and L (= A/D converter value 1023).

  The value of the A/D converter is output directly to the 13-digit display of the Display Unit. After the adjustment has been accomplished, reconnect link BR6 in the original position.

5.3.1.3 Analog Circuit Board

5.3.1.3.1 Supply Voltages

	Pin	Voltage	Current
ST1	22a	+10 V	approx. 50 mA
	22b	-10 V	approx. -10 mA
	23b	+5 V	approx. 25 mA
	24b	GND	
	23a	+12 V	0/7.5 mA with AF off/AF on
	24a	+25 V	< 1 mA

5.3.1.3.2 General

All analog switching functions are performed by means of CMOS switches, a logic H = +10 V at the control input of the CMOS switch corresponding to ON and a logic L = < 1 V corresponding to OFF.

For driving the required inputs (Table 4-1), TTL levels must be applied which are converted to 0 or 10 V by means of level shifters.

If switches off, the resistance of the CMOS switches is > 10 MΩ, and if switched on approx. 300 Ω.

NOTE: Analog DC voltage values given assume a supply voltage of +10 V ±1%.

5.3.1.3.3 Analog Level Path

5.3.1.3.3.1 Level Calibration

- After the supply voltage has been applied, apply a variable voltage (0.2 to 2 V) to ST1/17a.
- Measure the voltage at B1/III pin 3 by means of a digital voltmeter. V_{center} = 2 V with a tolerance of ±0.02 V. While the input voltage being measured is at V_{center} ±20 mV, a +5-V signal (H level) must appear at ST1/21b signifying calibration complete.
- If $V_{in} < V_m$, the output of the comparator B1/III pin 1 should be approx. +9 V and if $V_{in} > V_m$ it should be approx. -5 V.
- If the logic signal CISPR 1 v CISPR 3 is applied, the output B1/IV pin 9 should be -9 V, and if the logic signal $\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$ is applied, it should be +9 V.

5.3.1.3.3.2 Programmable Amplifiers B2/I, B2/II

- Switch on B6/I and B6/IV (AV., 20 dB).
- Apply 2 V to ST1/17a. The voltage measured at the analog level output 7a via B6/I, B2/I, B7/III, B3/II should be 3.55 V ±2% and the voltage measured at B2/II pin 15 should be 4 V ±2%.
- Apply a logic L to the input (ST1 pin 2b).
- Measure voltage at the output to the sample/hold amplifier (ST1 pin 3a). It should be 2 V ±2%.

- When B6/III is turned on (log 40 dB or log 60 dB or etc.; see Table 4-1), the voltage at B2/II pin 15 should rise to 8 V ±2%.

5.3.1.3.3.3 Adjusting the Logarithmic Converter

- Apply a variable DC voltage to pin 17a and switch on B6/I by means of B7/I.
- Switch on LIN (B7/II).
  Adjust with a digital voltmeter at pin 18a and measure at pin 7a.
- By alternately adjusting R37 and R40, the following requirements must be met:

Pin 18a	0.4 V →	pin 7a	0.355 V ±1%
(V_{input})	4.0 V →	(V_{output})	3.55 V ±1%.

- Repeat these adjustments alternately until these values are reached.

5.3.1.3.3.4 Max. Level and Min. Level

For test setup see 5.3.1.3.3.3.

If the input voltage is less than 0.4 V, the MIN. LEVEL LED must light up (comparator output B3/III pin 9 approx. +9 V).

If V_{in} > 4 V, the MAX. LEVEL LED must light up (comparator output B3/III pin 4 approx. +9 V).

If these LEDs do not light up as required, check T3, T4 and the signal path up to the LEDs of the Display Unit.

It must be possible to scan the entire analog level indication LED array with the V_{in} setting range 0.4 to 4 V. Beyond these range limits, the LEVEL MAX. and LEVEL MIN. LEDs must light up.

5.3.1.3.4 Frequency Offset Signal Path

5.3.1.3.4.1 Offset Calibration

- After applying the supply voltage to the board, connect a voltage source with a control range of ±5 V EMF (Z_{source} = 10 kΩ) to ST1/14b. Set V_{in} to 0 V.
- Apply +5 V to ST1/5a (CAL. button).

- After this voltage has dropped (St1/5a = < 0.8 V), measure with a digital voltmeter at ST1/11a (2.5 V ±1%).
- Press CAL. button 15 and then measure.
- Repeat this process until with V_{in} (ST1/14b) = +5 V, 4 V ± 1% is obtained.
- Final testing: Set to the limit values and measure (after offset calibration).

V_{in}	V_{out} (2%) ST1/11a	V_{out} (2%) ST1/8b	V_{out} (TTL) ST1/5b	LED offset centre
0 V ±0.025 V	2.5 V	0 V	+5 V	ON
-5 V	1 V	-5 V	< 0.8 V	OFF
+5 V	4.0 V	+5 V	< 0.8 V	OFF

5.3.1.3.4.2 Peak-value Rectification

- Connect ST1/14b to ground and switch in B8/II ST1/4a = High ($\overline{m}$).
- Connect digital voltmeter to B14/I pin 15 and set 2.5 V by means of R99.
- Connect digital voltmeter to B14/II pin 1 and set 2.5 V by means of R98.
- When a logic (TTL) H is applied to 10a (peak value 50 ms), the output voltage must drop to a maximum of $V_{orig.}/2$ (storage capacitor).
- When logic H is applied to select m, Δf(-) at ST1/1a and m, Δf(+) at ST1/1b, no voltage difference must occur (< 25 mV).
- The calibrated frequency offset signal (see 5.3.4.1) can be directly connected through to the output ST1/3a.
- The level can be taken to the peak-value rectifier via B8/3 (AM measurement).

5.3.1.3.4.3 Frequency Correction Voltage

NOTE: Vary R111 only if the frequency of the mother oscillator is to be calibrated (pulled) for the synthesizers of the ESH 3 (the frequency responds only very slowly). If the frequency cannot be pulled, the setting range of R111 at ST1/20a, which should be +1 V to +9 V, can be checked using a digital voltmeter at ST1/20a.

Calibrate frequency:

- Select TWOPORT mode on the ESH 3 and connect a high-precision frequency counter to the generator output.
- Adjust by means of R111 the counter frequency to that set on the ESH 3.

5.3.1.3.4.4 AF Amplifier

- Apply supply voltage.
- Apply AF signal (V_{in} = 50 mV/1 kHz) to ST1/18b.
- Connect an oscilloscope to ST1/19a. V_{out} should be approximately 12 V_{pp} if ST1/21a (volume control 50 kΩ) is connected to ground and no loudspeaker is connected.
- Apply a logic H to ST1/13a (+5 V) to switch off the AF amplifier (T7 is cut off).
- Measure gain Voltage gain = approx. 33; P_{out} = approx. 0.33 W into 16 Ω.

5.3.1.4 Synthesizer 2 (Y4)

5.3.1.4.1 Supply Voltages

Pin	Voltage	Current
ST1,b24	Ground	-
ST1,b23	+5.25 V ±0.1 V	approx. 110 mA
ST1,a22	+10 V ±0.1 V	approx. 25 mA
ST1,a23	+12 V ±0.5 V	approx. 60 mA
ST1,a24	+25 V ±0.2 V	approx. 6 mA
ST1,b22	-10 V ±0.1 V	approx. 3 mA
ST1,ab19	+1 to +9 V	approx. <1 mA

5.3.1.4.2 Reference

- Remove ST5. Connect spectrum analyzer to ST3. f = 60 MHz, level: approx. -20 dBm.
- Adjust L68 so that the oscillator starts oscillating and the frequency is 60 MHz if +5 V is present at ST1.ab19.
- Set maximum level by means of C160.

- Vary voltage at ST1.ab19 between +1 and 9 V at the same time checking the spectral purity of the signal.

- Check the TTL reference signals at

  ST1.b18 : f = 100 kHz
  ST1.ab1 : f = 500 Hz
  B41,1 : f = 500 Hz
  B41,3,13 : f = 1 kHz

- Apply external reference signal to ST4 (f = 5/10 MHz) from 1-V, 50-Ω source. Frequency error better than 2×10^{-6}.

- Apply +5 V corresponding to external reference to ST1.a2 and b2.

- Measure frequency at ST3, the accuracy of which must be equal to that of the external reference.
  This frequency must not change when the voltage at ST1.ab19 is varied between +1 and +9 V.

- Connect the spectrum analyzer to BU1 pin 8 and ground, which permits detailed display of the spectral purity of the reference oscillator.

- Unwanted oscillations of T1 and T3 must be avoided by short circuiting the coils L4 and L21, respectively.
  Discrete non-harmonic spurious signals should be down > 80 dB.
  Sideband noise 10 kHz away should be down > 140 dB/Hz.

5.3.1.4.3 50-to-51-MHz Oscillator

- Connect spectrum analyzer to ST5 R116/ground.

- Remove shortcircuit across L21.

- Adjust frequency to 50.05 MHz, connecting ST1.a3 to a14 as follows:
  H = a3, a5
  L = a4, a6 to a14.

- Set C42 to mid-position.
  Check level at ST5: ..... -10 dBm ±2 dB at 5.005 MHz
  (Adjustment by means of R117)
  Check at ST1.b13:
  H = oscillator is synchronized
  L = oscillator is not synchronized.

If oscillator not synchronized, then use a scope to check the logic levels or oscillograms at the points given, by reference to the circuit diagram:

B19, pin 11
B20, pin 8
B22, pin 6
B24, pins 1, 3, 10, 13, 4, 12
B25, pin 12
B18, pin 23
B16, pin 14
B16, pin 3 — 1 kHz if synchronized
B16, pins 13, 12
B17, pins 11, 8, 9, 2

- Check voltages at B15:
  Pin 3: +2.5 V ±0.2 V
  Pin 7: +25 V ±1 V
  (Adjust by means of C24:)
  Pin 6: +6.5 V ±0.3 V.

- Apply required logic levels to vary the frequency between 50.000 and 50.999 MHz and watch at the same time the synchronization indication (b13).

- Check the spectral purity:
  Discrete non-harmonic spurious signals ..... down > 80 dB
  Sideband noise 10 kHz away ..... > 140 dB/Hz
  Level at ST3: f = 65.0000 to 65.0999 MHz ..... -16 dBm ±2 dB

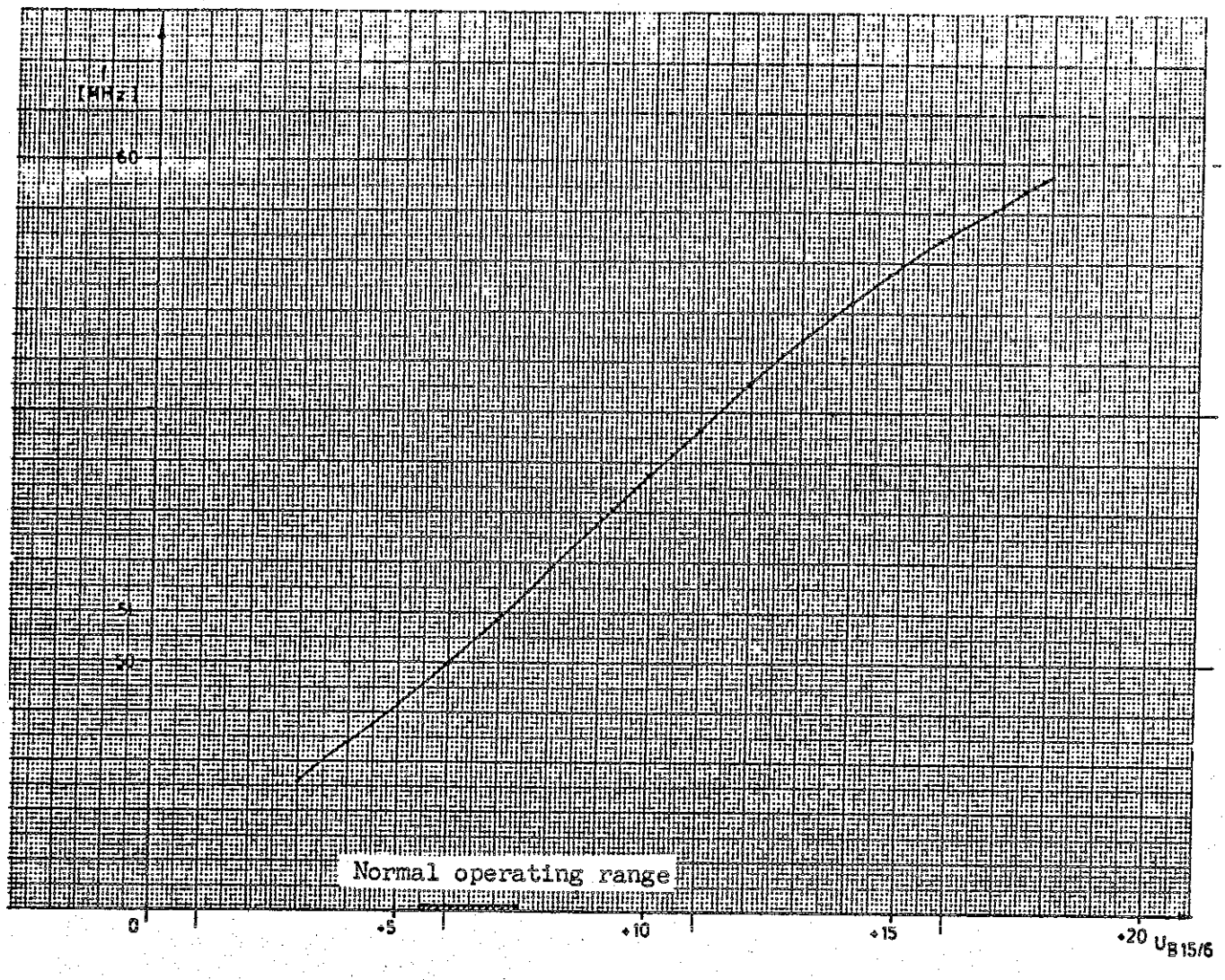


Fig. 5-1 Typical tuning characteristic of the 50-to-51-MHz oscillator

5.3.1.4.4 66-MHz Oscillator

- Connect spectrum analyzer to ST2.
- Remove short-circuit across L4.
- Rotate core of L4 inwards until the oscillator starts to operate.
  Adjust C13 for maximum.
  Level at ST2 into 50 Ω ..... +7 dBm ±2 dB
  Frequency: corresponds to frequency of Q1.
- Check synchronization indication ST1.b14:
  H = oscillator synchronized
  L = oscillator not synchronized.

If oscillator not synchronized, then use a scope to check the logic levels or oscillograms at the points given, by reference to the circuit diagram:

B1, pin 11
B2, pin 8
B3, pin 6
B10, pins 1, 3, 10, 13, 4, 12
B5, pin 23
B7, pins 14, 3, 1, 2, 13
B8, pins 10, 5, 6

- Check voltages at B6: pin 3: ..... +2.5 V ±0.2 V
  pin 7: ..... +25 V ±1 V
  pin 6: ..... see illustration

- Apply a logic H to ST1.b3: The frequency is increased by 1.5 kHz.

- Apply a logic H to ST1.b4: The frequency is decreased by 1.5 kHz.

- Check the spectral purity:
  Discrete non-harmonic spurious signals ..... down > 80 dB
  Sideband noise 10 kHz away ..... down > 140 dB/Hz

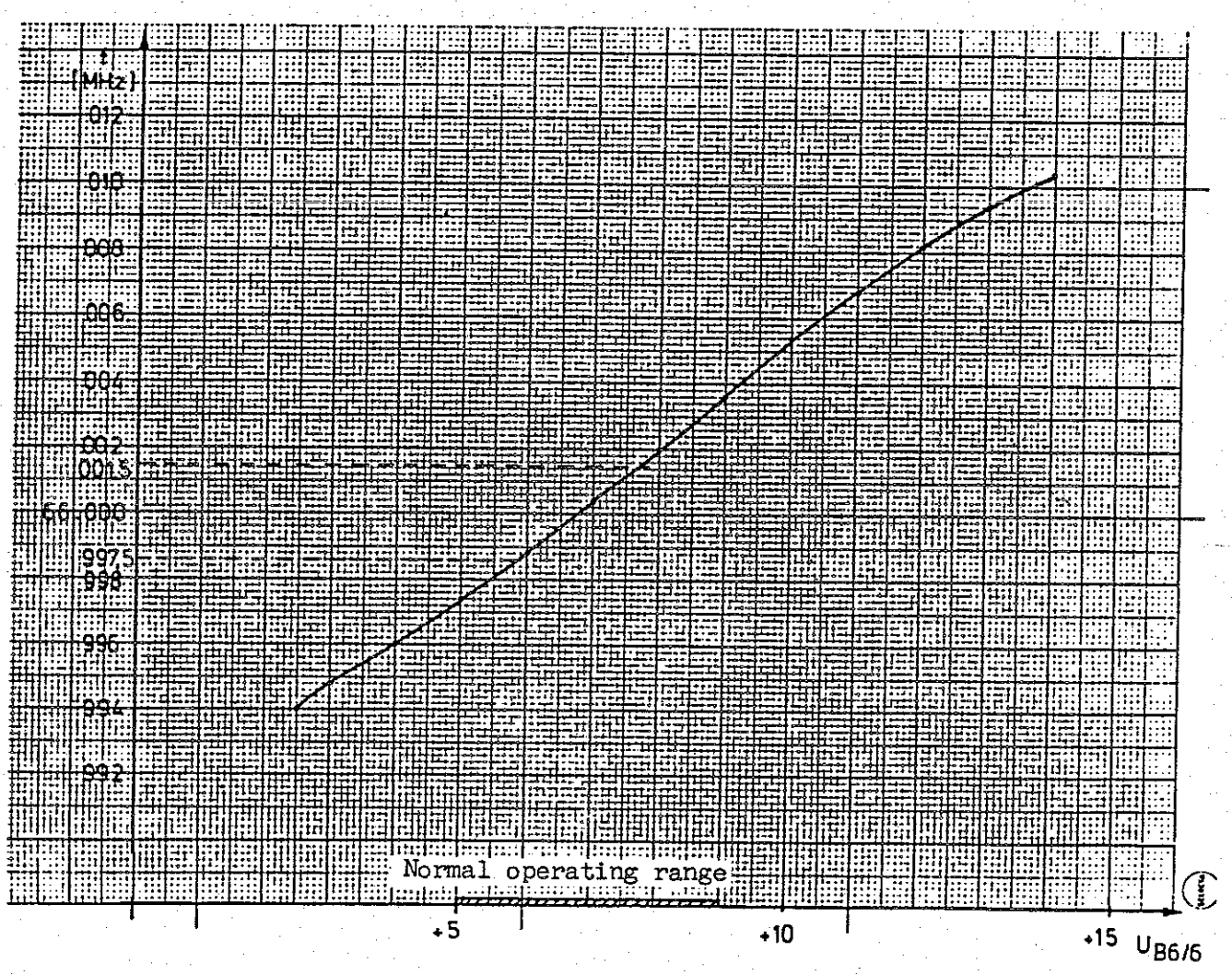


Fig. 5-2 Typical tuning characteristic of the 2nd oscillator (66 MHz)

5.3.1.5 Synthesizer 1 (Y5)

5.3.1.5.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1, b24	Ground	-	-
ST1, b23	+5.25 ±0.1 V	approx. 105 mA	0
ST1, a22	+10 ±0.1 V	approx. 35 mA	
ST1, a23	+12 ±0.2 V	max. 75 mA	0
ST1, a24	+25 ±0.1 V	approx. 4 mA	0
ST1, b22	-10 ±0.1 V	approx. 6.5 mA	0
St1, b18	TTL	< 1 mA	100 kHz
ST1, a7	TTL	< 1 mA	-
b8	100-kHz decade		-
a9			-
b10			-
a11	TTL	< 1 mA	-
a12			-
b13	1-MHz decade		-
a14			
a16	TTL	< 1 mA	-
a15	10-MHz decade		-
ST2	-17 dBm ±1 dB	-	65.0 to 65.1 MHz

5.3.1.5.2 Adjustment of 75/85/95/105-MHz Oscillators

- Connect frequency counter (50 Ω) to ST3.
- Remove B3 and connect R15 to +10 V.
  The oscillators are controlled by the TTL levels at the input lines of the decades depending on the receive frequency, and pretuned by a D/A-converted voltage.
- Check the pretuning voltage at ST1, a17 and R16:

	ST1,a17	R16
All decade inputs at logic L	0 ±5 mV	3.8 V ±20 mV
All inputs of the 100-kHz and 1-MHz decades at logic H	7.4 V ±0.2 V	17.8 V ±0.8 V

- The tuning range is adjusted by means of the variable capacitor, and the initial frequency is adjusted by means of the variable inductance (see Fig. 5-7 in the appendix).

Oscillator	Decade driving signal	Adjust with
75 to 85 MHz	0.000 to 9.9 MHz	C3, L12
85 to 95 MHz	10.0 to 19.9 MHz	C13, L13
95 to 104.0 MHz	20.0 to 29.9 MHz	C23, L14

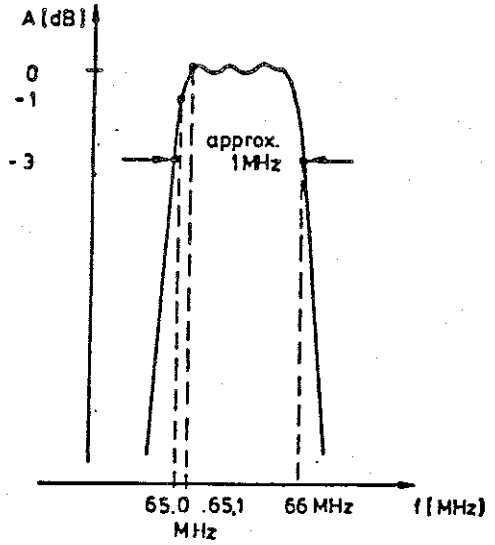
5.3.1.5.3 Adjustment of Output Level

- Connect spectrum analyzer (50 Ω) to ST3.
- Switch the decades in 1-MHz steps.
- Adjust the output level by means of C38 over the frequency range from 75 to 105 MHz to ..... +23 dBm ±2 dB

5.3.1.5.4 Adjustment of 65-MHz Amplifier

Connect sweep generator (50 Ω) to ST2 and apply
level of ..... -17 dBm
Frequency range ..... 60 to 70 MHz

Connect display section of the sweep generator to ST7. Make coarse adjustment of L31, L32, L33 for maximum at 65.5 MHz. Connect sweep generator to ST7 (via capacitor). Level and frequency same as above. Connect display section to ST6. Make coarse adjustment of L36, L37, L38 for maximum at 65.5 MHz. Connect sweep generator to ST2. Make final adjustments to reach selectivity curve shown below.



5.3.1.5.5 Adjustment of 10-to-40-MHz Amplifier

Apply signal between 65 and 65.1 MHz with a level of 16 ±1 dBm to ST2.

Check level at ST5 with the aid of a spectrum analyzer while varying the oscillator frequency between 75 and 105 MHz

Required level ..... -21 dBm ±2 dB

Frequency ..... 10 to 40 MHz

Check level at ST4 with the aid of a spectrum analyzer by varying the oscillator frequency between 75 and 105 MHz

Required level ..... +2 dBm ±3 dB

5.3.1.5.6 Checking the Synchronization Indication

Synchronization indication ..... logic L

(B3 removed)

5.3.1.5.7 Checking the Synchronization

Insert B3.

Apply 100-kHz reference (crystal-controlled, with low sideband noise).

Synchronization indication ..... logic H

Voltage at R15 (depending on f) ..... > +3 to < +19 V

5.3.1.5.8 Checking the Sideband Noise

The signal at ST2 should have minimal sideband noise.

1 kHz away ..... down typ. 90 dB/Hz

10 kHz away ..... down typ. 135 dB/Hz

The 100-kHz reference must be crystal-controlled with low sideband noise.

The typical sideband noise characteristic is shown in Fig. 5-3.

Excessive variations at A can be corrected by varying the gain of B3 (R95).

If there are considerable, abrupt frequency changes or warm-up transients, then that points to problems with the oscillators.

Required rejection of discrete signals over the range 0 to 50 kHz from the carrier (measured at an analyzer IF bandwidth of 10 Hz) ..... typ. > 100 dB

Time required for synchronization after any change in frequency ..... < 100 ms

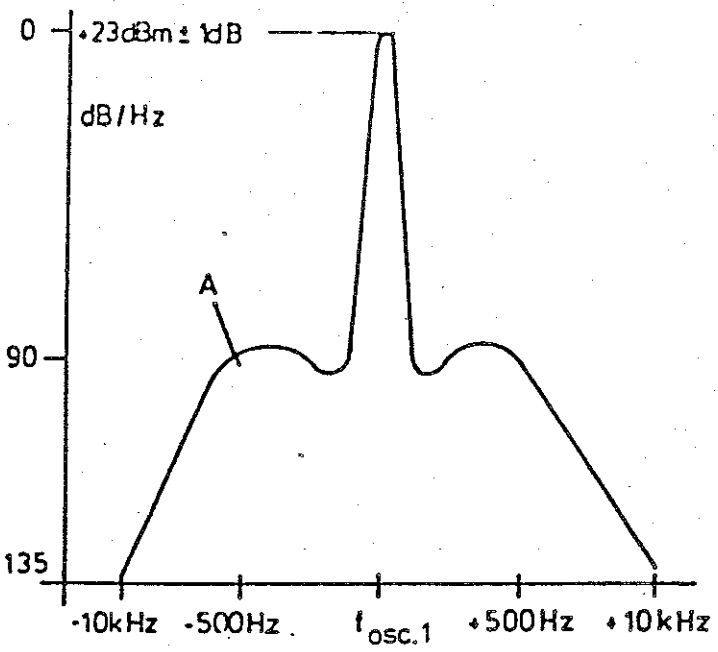


Fig. 5-3 Characteristic of typical sideband noise

5.3.1.6 Filter Control (Y6)

5.3.1.6.1 Supply Voltages

Pin	Voltage		Current	Frequency
ST1.b24	Ground		-	-
ST1.b23	+5.25 V	±0.1 V	approx. 3 mA	0
ST1.a22	+10 V	±0.1 V	approx. 1.5 mA	0
ST1.a24	+30 V	±0.5 V	approx. 0.7 mA	0
ST1.b22	-10 V	±0.1 V	approx. 3.5 mA	0
ST1.b17	0 to 7.5 V		< 1 mA	0
ST1.ab1	TTL		-	500 Hz

5.3.1.6.2 Checking the Digital Section

Connect ST1.b20 via 470 Ω to ground.

Apply logic levels to pins ST1, 3 to 16.

Truth table

f(MHz)	Range	High level St1, a...	ST1, a2
0 to 0.14	1	21	L
0.15 to 0.19	2	19	L
0.2 to 0.27	3	17	L
0.28 to 0.38	4	15	L
0.39 to 0.53	5	13	L
0.54 to 0.74	6	11	L
0.75 to 1.04	7	9	L
1.05 to 1.44	8	7	L
1.45 to 1.99	9	6	H
2.0 to 2.69	10	8	H
2.7 to 3.69	11	10	H
3.7 to 5.19	12	12	H
5.2 to 7.19	13	14	H
7.2 to 9.99	14	16	H
10 to 19.99	15	18	H
20 to 29.99	16	20	H

While the range is being selected, St1.b20 is at low level.

Maximum time required for range selection ..... < 35 ms.

5.3.1.6.3 Checking the Analog Section (Pre-adjustment)

Increase the input voltage at ST1.b17 in steps of 75 mV from 0 V to +7.4 V. The resulting output voltage at ST1.a4 and the trimmers used are shown in Table 5-1.

Table 5-1

Input voltage (V)	0	+0.75	+3.75	+6.75	+7.4
Adjusting element	R79	R55	R70	R89	R103
Output voltage (V)	+3±0.1	+6±0.1	+13.75±0.1	23±0.1	26±0.1

Make final adjustment together with Filter 2 (Y8) for minimum input reflection coefficient in range 15.

5.3.1.7 Filter 1 (Y7)

Supply voltages:

Pin	Voltage	Current
ST1.b24	Ground	-
ST1.b23	+5.25 V ±0.1 V	approx. 30 mA

Switch in the desired filter by applying a logic H to pins ST1.a7 to a21. Adjust filters 1 to 8 for a reflection coefficient characteristic in accordance with Fig. 5-4 using a sweep-frequency network analyzer.

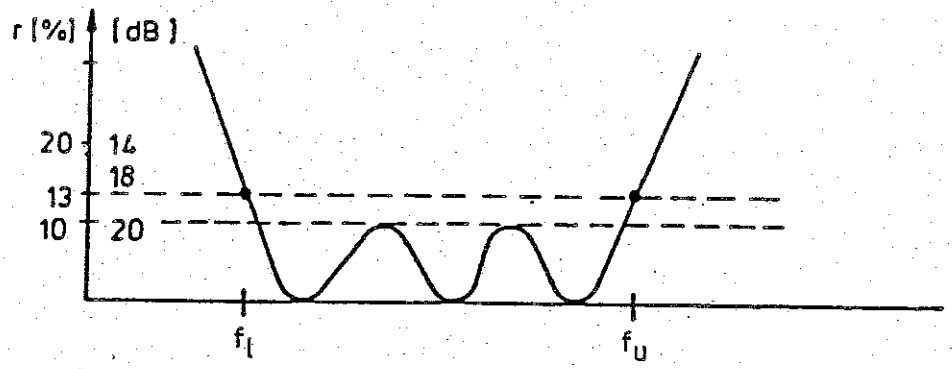


Fig. 5-4 Reflection coefficient characteristic of the fixed-tuned filters

Reflection coefficient within the filter range ..... < 10%
Reflection coefficient at the cut-off frequencies ..... < 13%
Insertion loss ..... < 0.5 dB
Attenuation at $f_u/2$ ..... > 18 dB

Test setup:

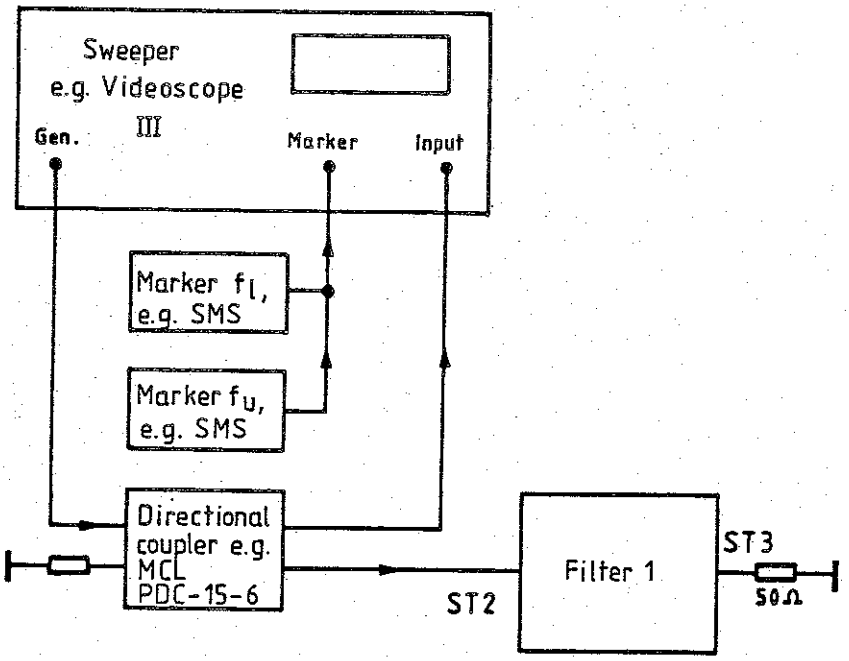


Table 5-2

Filter	Cut-off frequencies f_l	f_u	Adjust with	Logic H to ST1.a...
1	10*kHz	150 kHz	L2, L3, L4	21
2	150 kHz	200 kHz	L5, L6, L7	19
3	200 kHz	280 kHz	L10, L11, L12	17
4	280 kHz	390 kHz	L15, L16, L17	15
5	390 kHz	540 kHz	L20, L21, L22	13
6	540 kHz	750 kHz	L25, L26, L27	11
7	750 kHz	1.05 MHz	L30, L31, L32	9
8	1.05 MHz	1.45 MHz	L35, L36, L37	7

* f_l = 20 Hz for model 56 (subassembly model 53)

5.3.1.8 Filter 2 (Y8)

5.3.1.8.1 Supply Voltages

Pin	Voltage	Current
ST6.b24	Ground	-
ST6.b23	+5.25 V ±0.1 V	approx. 30/60 mA
ST6.a2	Logic H	< 0.5 mA
ST6.a4	+3 to +28 V	< 0.1 mA

Switch in desired filter by applying a logic H to pins ST6.a6, 8 to 20. Adjust filters 9 to 14 similarly to 5.3.1.7 in compliance with the following table:

Table 5-3

Filter	Cut-off frequencies f_l	f_u	Adjust with	Logic H to ST.a...
9	1.45 MHz	2.0 MHz	L40, L41, L42	6
10	2.0 MHz	2.7 MHz	L45, L46, L47	8
11	2.7 MHz	3.7 MHz	L50, L51, L52	10
12	3.7 MHz	5.2 MHz	L55, L56, L57	12
13	5.2 MHz	7.2 MHz	L60, L61, L62	14
14	7.2 MHz	10.0 MHz	L65, L66, L67	16

Feed in test signal to ST7 (terminate with 50 Ω at ST8).

5.3.1.8.2 Adjustment of Filter 15

Adjust L72, L73, C156 as follows:

f = 11 MHz, V into ST6.a4 = +6 V ±0.2 V
f = 15 MHz, V into ST6.a4 = +13.75 V ±0.3 V r < 10%
f = 19 MHz, V into ST6.a4 = +26 V ±0.3 V

6-dB bandwidth of filters 15 and 16 ..... < 6 MHz
Attenuation at $f_u/2$ ..... > 18 dB

5.3.1.8.3 Adjustment of Filter 16

Adjust L78, L79, C162, C164 for minimum reflection coefficient of the ESH 3 over the frequency range 20 MHz to 29.9999 MHz after having adjusted filter 15 using Y6.

C164: maximum effect at f_l
C162: maximum effect at f_u.

After adjustment, fix the cores of L72, L73, L78 and L79 with the cable tie provided for this purpose and secure the coils using any type of varnish or glue that is suitable for RF applications.

5.3.1.9 Mixers 1 and 2 (Y9)

Note: The pin designations in brackets (e.g. (X7)) or the component designations in brackets (e.g. (V111)) refer to model 56 of the ESH 3. Unless otherwise stated, the adjustment procedure is identical.

5.3.1.9.1 Supply Voltages

Pin	Voltage	Current
ST1.b24	Ground	-
ST1.a22	+10 ±0.1 V	approx. 10 mA
ST1.a23	+12 ±0.3 V	approx. 60 mA
ST1.a24	+25 ±0.1 V	approx. 25 mA
ST1.b22	-10 ±0.1 V	approx. 5 mA

5.3.1.9.2 Adjustment of Input Low-pass Filter

- Connect network analyzer to ST2.
- Remove BU1.
- Connect 50-Ω termination between ST8 pins 1 and 4 (r < 2%).
  Tune L1, L2, L3, L4, L5 for reflection coefficient ..... < 10%
  (over frequency range 0 to 30 MHz).

5.3.1.9.3 Adjustment of 75-MHz Amplifier

- Using R1 set operating point of T1 (V111) to ..... 22 mA ±2 mA
- Feed frequency of 75 MHz into ST9/2,3 (X9/1,2) using a sweep generator.
- Connect sweep display unit to ST10/1,4 (X10/A1,2)
- Adjust C14 for maximum at f = 75 MHz.
  Required gain ..... 22 dB ±2 dB
- Connect sweep display unit to ST14 (X14).
- Adjust amplifier T2, T14 and T15 (V200, V140 and V150).
- Adjust C117 for maximum at f = 75 MHz.
- Required gain ..... 15 dB ±3 dB
- (The ESH 3 is supplied with the 75-MHz amplifier permanently switched on (ST10 (X13) plugged on).

5.3.1.9.4 Adjustment of Diplexer of 2nd Mixer

- Connect sweep generator to ST11.2 (X11/B) and ST12.2 (X12) (50-Ω system) and adjust L18 for maximum attenuation at 9 MHz.
- Connect sweep generator to ST11.2 (X11/B) and ST7 (X7) (50-Ω system) and adjust C31 for maximum gain at 9 MHz.

5.3.1.9.5 Adjustment of 9-MHz Amplifier

Connect a sweep generator to ST11 (2,3) (X11/B) and ST7 (X7) (50-Ω system) for the adjustment.

5.3.1.9.6 500-Hz Bandwidth

- Connect ST1.a3 (X1.A3) to ground.
- Adjust R63 for maximum gain.
- Adjust C53 for minimum ripple.
- Note gain.

5.3.1.9.7 2.4-kHz Bandwidth

- Connect ST1.a5 (X1.A5) to ground.
- Set R69 to mid-position.

- Adjust C64, C67 for minimum ripple.
- Adjust R69 for same gain as with 500-Hz bandwidth.

5.3.1.9.8 10-kHz Bandwidth

- Adjust R76 for same gain as with 500-Hz and with 2.4-kHz bandwidth.
  Gain of 9-MHz amplifier ..... 27 ±1 dB

5.3.1.9.9 Adjustment of Overload Detection

- Insert BU3 and BU4. (Connect X10A to X10B and X11A to X11B)
  The 2nd oscillator (f = 66.00 MHz, level = +7 dBm ±1 dB) is connected to ST5 (X5).

5.3.1.9.9.1 Overload Detection 2

Feed 75.00-MHz signal to ST9 pins 2 and 3 (X9/B).

At a level of -22 dBm ±2 dB, the logic signal at ST1.a7 (X1.A7) should change from H to L. Adjust with R35 (increasing R35 raises the response threshold).

5.3.1.9.9.2 Overload Detection 1

Feed a signal of frequency 75 to 135 MHz into ST9 pins 2 and 3 (X9/B).

At a level of ±3 dBm ±1 dB, the logic H at ST1.a9 (X1.A9) should change to logic L. Adjust with R18 (increasing R18 raises the response threshold).

5.3.1.9.9.3 Checking the Level at ST4 (X4)

Feed +23 dBm ±1 dB (frequency range 75 to 105 MHz) into ST3.

Output level required at ST4 (X4) ..... -15 dBm ±2 dB
(Adjust with R94 (R208)).

5.3.1.9.9.4 Adjustment of the 1st Mixer

(to be carried out on model 56 of ESH 3 only).

- Connect X8.A1 to X8.B2 and X9.A1 to X9.B2.
  Terminate X2 with 50 Ω.
- Feed 1st oscillator (level to +23 ±2 dBm, frequency 75 to 105 MHz) at X3.

- Connect spectrum analyzer to X14.
- Level measured at X14 at 75-MHz oscillator frequency should be <-32 dBm (Note effect of cover on soldered side).
- An adjustment is possible by bending the terminal wires 3 and 6 of transformers T4 and T6.
- Following the adjustment, pins of T4 must be affixed using yellow UHU adhesige.
- Recheck level at X14.

5.3.1.9.9.5 Checking the Level at ST6

Feed +7 dBm ±1 dB (frequency 66 MHz) into ST5.

Output level required at ST6 ..... -15 dBm ±2 dB (Adjust with R96).

Check the following performance specifications of Y9 using test setups as in section 3.2:

Input reflection coefficient 10 kHz to 30 MHz ..... < 20%
Noise figure 100 kHz to 30 MHz ..... < 13 dB
Oscillator reradiation 75 MHz to 105 MHz ..... < 20 dBµV
Image frequency rejection 150 MHz to 180 MHz ..... > 90 dB
IF rejection 75 MHz ..... > 100 dB
IM rejection a_{d3} - 3rd order intercept point ..... > +20 dBm
(see specifications)
IF bandwidths 10 kHz, 2.4 kHz, 500 Hz
(see specifications)
Gain ..... 35 ±1 dB

5.3.1.10 Calibration Generator (Y10)

5.3.1.10.1 Supply Voltages

Pin	Voltage/Level	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	+5.25 ±0.1 V	approx. 0/65 mA	0
ST1.a22	+10 ±0.1 V	approx. 65/6 mA	0
ST1.b22	-10 ±0.1 V	approx. 3 mA	0
ST1.a1	TTL		500 Hz
ST4	-15 dBm	-	30 kHz
ST5	-13 dBm	-	8.97 MHz
ST6	-15 dBm	-	66 MHz (±1.5 kHz)
ST3	-15 dBm	-	75 MHz to 105 MHz

5.3.1.10.2 Adjustment of Sinewave Generator

- Connect +5 V to ST1.a4.
- Connect spectrum analyzer to ST2.
- Connect voltmeter to ST1.a15.
- Adjust for maximum level on the spectrum analyzer and minimum voltage on the voltmeter at:
  9 MHz by means of C9 (C10, C20)
  75 MHz by means of C45, C52, C61, C66.

The adjustment of C61, C66 is interactive.

Level at ST2 in the frequency range 10 kHz to 30 MHz .... 80 dBµV ±3 dB
(Variable with R84; measured with a power meter.) = -27 dBm ±0.3 dB

Spectral purity of the output signal at ST2:
Non-harmonic spurious signals ..... > 40 dB down

Check the control voltage at ST1.a15:
When tuning through the range from 10 kHz to 30 MHz, the voltage must not change abruptly and there must be no AC voltage superimposed on it.

Check by means of oscilloscope; typically ..... 0.8 V to 4 V

5.3.1.10.3 Adjustment of Temperature Compensation of Sinewave Generator

The temperature compensation can be adjusted in several cold/warm cycles. For the relationship between change in level and required sense of rotation of R77 see Table 5-4.

Table 5-4

Increase in temperature causes level increase. Decrease in temperature causes level drop.	Turn R77 counterclockwise.
Increase in temperature causes level drop. Decrease in temperature causes level increase.	Turn R77 clockwise.

Permissible total change in level due to change in frequency and temperature over the range from -10 to +45°C ..... < 0.5 dB

Required level at ST2 ..... 80 dBµV ±0.3 dB
= -27 dBm ±0.3 dB

over the total temperature and frequency range.

Table 5-5

Input level (measured with spectrum analyzer)

Pin	Level	Frequency
4	-15 dBm ±1 dB	30 kHz
5	-13 dBm ±1 dB	8.97 MHz
6	-15 dBm ±1 dB	66 MHz
3	-15 dBm ±1 dB	75 MHz to 105 MHz

Table 5-6

Mixer level

(measured by means of RF probe at pin 8)

Mixer	Level	Frequency
B1	0 dBm ±2 dB	8.97 MHz
B3	0 dBm ±2 dB	66 MHz
B5	0 dBm ±2 dB	75 MHz to 105 MHz

Level required at C70 (f = 10 kHz to 30 MHz, with AGC,
measured by means of high-impedance probe) ..... 5 mV ±3 dB
Level at ST7 ..... -67 dBm ±0.3 dB
Level variation by R110 ..... ±0.7 dB

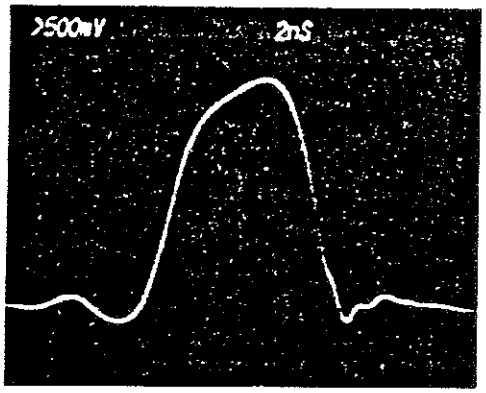
5.3.1.10.4 Checking the CISPR 3 or CISPR 1 Pulse Generator

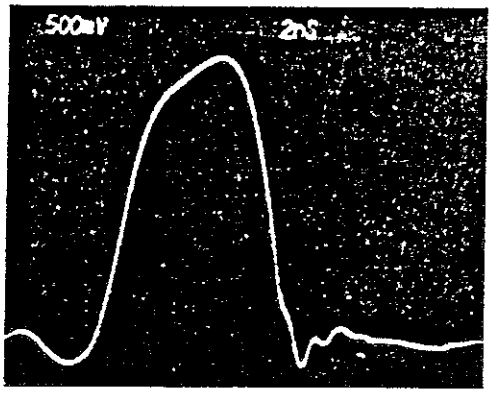
- Disconnect ST1.a4 from +5 V, and instead connect either ST1.a6 (CISPR 3) or a5 (CISPR 1) to +5 V.

- Check pulse at ST7, terminated with 50 Ω, by means of a 1-GHz oscilloscope:

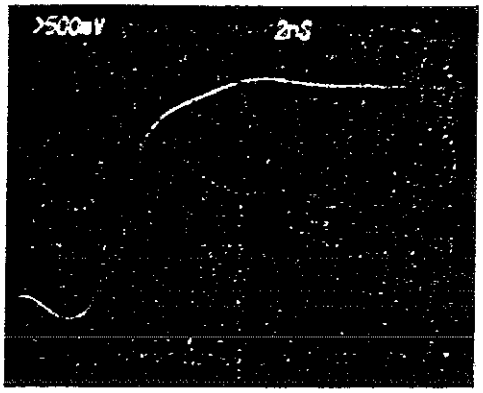
Table 5-7

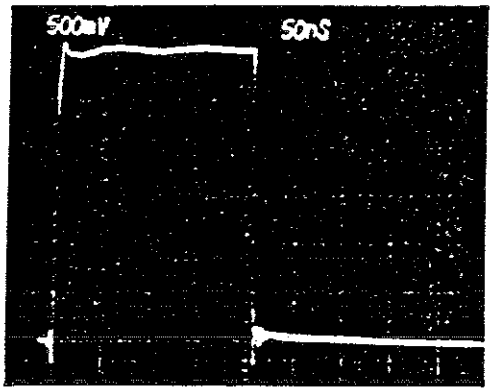
	Logic H to ST1	PRF	Pulse energy µVs (EMF) ±10%	Adjust with
CISPR 3	a6	25 Hz	1.35	R89
CISPR 1	a5	100 Hz	0.0316	R91





Rise time t_r = 3 ns
a) with CISPR 1 pulse

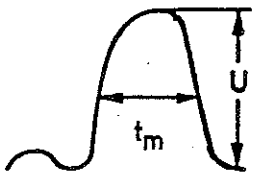




Rise time t_r = 4 ns
b) with CISPR 3 pulse

Fig. 5-5 Pulse calibration

For a rough measurement, the pulse energy can be graphically integrated or calculated according to the following simplification:



Pulse area = $V \cdot t_{50\%}$

Accordingly, with CISPR 1 pulse (Fig. 5-5a),
the pulse area = 2.8 (V) · 5.6 (ns) = 0.01568 µVs

corresponding to an EMF pulse energy of 0.03136 µVs.

This calibration pulse of the ESH 3 is 20 dB below the CISPR 1 standard pulse.

Fig. 5-5b: CISPR 3 pulse

$V \cdot t_{50\%} = 3(V) \cdot 210(ns) = 0.63\ \mu Vs$

$V \cdot t_{50\%} = 1.26\ \mu Vs$ (EMF pulse area)

Hence, this calibration pulse is 20 dB below the CISPR 3 standard pulse (13.5 µVs).

5.3.1.11 Mixer 3 (Y11)

5.3.1.11.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	-5.25 ±0.1 V	approx. 12 mA	0
ST1.a22	+10 V ±0.1 V	approx. 48 mA	0
ST1.b22	-10 V ±0.1 V	approx. 18 mA	0
ST1.b1	TTL	-	500 Hz

5.3.1.11.2 Adjustment of 8.97-MHz Oscillator

- Apply exact 500-Hz reference to ST1.b1 (TTL level squarewave; for repair purposes, use ESH 3 reference)
- Measure control voltage $V_{control}$ at R40/R41
  Adjust C43 so that $V_{control}$ ..... 5 V ±1V
  (If adjustment is not possible, vary L11 slightly)
- Measure output level on ST3 ..... -13 dBm ±2 dB
- Measure oscillator frequency at ST3 ..... 8.97 MHz
  (The accuracy of the measured value depends on the accuracy of the reference used.)
- Check synchronization indication at ST1.b2: logic H
  (loop is synchronized).

5.3.1.11.3 Adjustment of Basic Gain between ST2 and ST5

a) Initial settings:

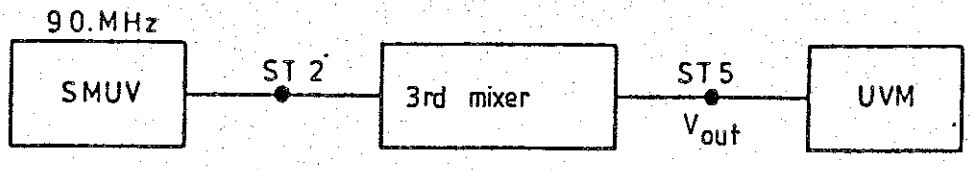
- Settings on the ESH 3:
  IF bandwidth 5: 500 Hz to 10 kHz (ST1.a11 = L)
  IF attenuation 40, 41: 40 dB

- Connect ST1.b12 to +10 V.
- Apply external DC voltage of -5 to +10 V to ST1.a12.
- Set external DC voltage to $\geq$ 4 V (= maximum gain).

V_{EMF} at ST2 with f = 9.000 MHz = 20 mV.

Measure at ST5 via a high impedance using a millivoltmeter.

Test setup:



b) Adjustment

Set output voltage V_{out} by means of R20.

V_{out} ..... 200 mV

5.3.1.11.4 Checking the Noise Filter Bandwidth

Measure between ST2 and ST5 with any IF bandwidth other than 0.2 kHz (ST1.a11 = L). Vary the signal-generator frequency to determine the upper and lower 1-dB and 3-dB cut-off frequencies of the noise filter.

Table 5-8

	$f_{cut\text{-}off\ lower}$/kHz	$f_{cut\text{-}off\ upper}$/kHz
1-dB cut-off frequencies	25 $\pm$1	35 $\pm$1
3-dB cut-off frequencies	23 $\pm$1	37 $\pm$1

The pass-band characteristic should be approximately flat and must not exhibit a dip.

5.3.1.11.5 Checking the Calibration Gain Control Range

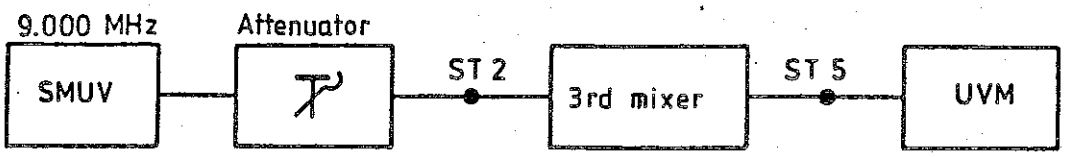
- Apply +10 V to ST1.b12 (calibration = ON).
- Feed DC voltage $V_{control}$ into ST1.a12.
- Vary the voltage at the base of T1 from 0 to +5 V.

- The gain between ST2 and ST5 should be variable between about -15 dB and 0 dB referred to maximum gain G_{max}.

  When the voltage at the base of T1 is 2 V, the gain is typically 6 dB below G_{max}.

5.3.1.11.6 Checking the IF Attenuation Steps

Test setup:



Use as accurate an attenuator as possible, such as the DPVP.

- Set $V_{control\ CAL}$ at the base of T1 again to about 2.0 V.
- Set the attenuator to 50 dB.
- Set the IF attenuation of the 3rd mixer to 0 dB (= maximum gain).
- Adjust signal generator level such that the millivoltmeter gives a deflection approximately 2 dB < 100 mV (near the 0-dB marker).
- Increase the IF attenuation of the 3rd mixer in steps of 10 dB and reduce the attenuator setting in steps of 10 dB.
- Observe deflection on millivoltmeter: The difference (= attenuation error) should be less than 0.1 dB. The sum of the attenuation errors should be approximately 0 dB.

5.3.1.11.7 Checking the IF Output Amplifier

Use the same test setup as in section 5.3.1.11.5 but measure at ST4.

- All inputs ST1.b7 to b10 = logic L.
- Adjust signal generator level so that the pointer of the millivoltmeter is on 2.0 V.
- Apply logic H to ST1.b8 and reduce the attenuator setting by 20 dB. Difference in pointer deflection ..... $\leq$ 1 dB

- Apply logic H to ST1.b7 and reduce the attenuator setting by further 20 dB.
  Difference in pointer deflection ..... $\leq$ 1 dB

5.3.1.11.8 Checking the 200-Hz Bandwidth and Adjustment of Gain

- ST1.a11 = logic H (200-Hz filter ON).
- Vary the signal generator frequency between the lower and the upper 6-dB cut-off frequency.

  $B_{6\ dB}$ ..... 200 Hz $^{+20\ Hz}_{-30\ Hz}$

- Tune to the maximum in the pass-band curve.
- Switch over to noise filter:
  Note readout on millivoltmeter.
- Switch back to 200-Hz filter:
  Adjust for same readout on millivoltmeter by means of R102.

5.3.1.11.9 Checking the Overload Detection

Settings on the ESH 3:
IF bandwidth 5: 500 Hz to 10 kHz (ST1.a11 = logic L)
IF attenuation 40, 41: 0 dB.

ST1.b11 = logic L if EMF at ST2 ..... 20 mV

5.3.1.12 Indication and AF Demodulation Board (Y12)

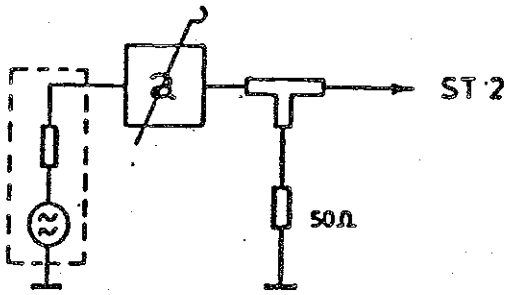
5.3.1.12.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	+5.25 V ±0.1 V	approx. 1 mA	-
ST1.a22	+10 V ±0.1 V	approx. 100 mA	-
ST1.b22	-10 V ±0.1 V	approx. 55 mA	-
ST1.ab1	TTL	-	500 Hz

5.3.1.12.2 Adjustment of Indication Section

Test setup:

Connect 30-kHz signal generator via attenuator to ST2. As ST2 is a high-impedance input, use a 50-Ω termination in parallel.



a) Linearity of B14:

Settings on the ESH 3: Operating range 33: 20 dB

- DVM check point: pin 6 of B14.
- Input voltage 20 mV; note reading (e.g. 210 mV).
- Input voltage 2 mV; vary R164 until 1/10 of the above measured value is obtained (e.g. 21 mV ±0.5 mV).
- Repeat adjustment to ensure optimum voltage setting.

b) Linearity of B15:

Settings on the ESH 3: Operating range 33: 20 dB

- DVM check point: pin 2 of B15.
- Input voltage 20 mV; note reading (e.g. 210 mV).
- Input voltage 2 mV; vary R174 until 1/10 of the above measured value is obtained (e.g. 21 mV ±0.5 mV).
- Repeat adjustment to ensure optimum voltage setting.

c) Average-value indication:

Settings on the ESH 3: Operating range 33: 20 dB
35: AV.

- DVM check point ST1.a2.
- Input voltage 20 mV; vary R182 until the DVM reads ..... 2 V ±5 mV
- Input voltage 2 mV; vary R177 until the DVM reads ..... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

d) CISPR indication:

Settings on the ESH 3: 35: CISPR
Frequency between 10 kHz and 149.9 kHz (CISPR 3).

- DVM check point: ST1.a2.
- Input voltage 20 mV; vary R198 until the DVM reads ..... 2 V ±5 mV
- Input voltage 2 mV; vary R195 until the DVM reads ..... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

e) LOG 40:

Settings on the ESH 3: Operating range 33: 40 dB
35: AV

- DVM check point: ST1.a2.
- Input voltage 200 mV; vary R139 until the DVM reads ..... 2 V ±5 mV
- Input voltage 2 mV; vary R186 until the DVM reads ..... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

f) LOG 60:

Settings on the ESH 3: Operating range 33: 60 dB
35: AV

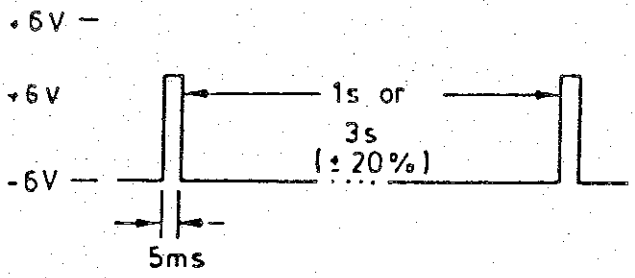
- DVM check point: ST1.a2.
- Input voltage 2 V; vary R142 until the DVM reads ..... 2 V ±5 mV
- Input voltage 2 mV; vary R188 until the DVM reads ..... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

g) Peak-reading time constants:

(With the ESH 3, determined by PEAK and the measuring time)

Settings on the ESH 3: Operating mode 38: GEN. OFF

Oscilloscope check point: B20 pin 10



h) 4th oscillator:

Feed TTL-level reference frequency of 500 Hz into ST1.ab1. Connect frequency counter to B33/2.

Table 5-9

Switch position		Nominal frequency	
A0	GEN.OFF	30.0 kHz	(±10 Hz)
A1	GEN.OFF	31.0 kHz	(±10 Hz)
USB	GEN.OFF	31.5 kHz	(±10 Hz)
LSB	GEN.OFF	28.5 kHz	(±10 Hz)
ANY	GEN.ON	30.0 kHz	(±10 Hz)

Same as above, but connect oscilloscope to ST5 instead of frequency counter.

Settings on the ESH 3: Operating mode 38: GEN.ON
Nominal level 40 mV_{rms} = 110 mV_{pp} = 15 dBm ±1 dB into 50 Ω

i) Remote frequency measurement (RFM):

- Connect a signal generator variable between 25 and 35 kHz, approx. 20 mV, to ST2.
- Select REM. FREQ. mode.
- Counter connected to ST5 should read out signal generator frequency.
- Measure nominal level at ST5 by means of oscilloscope:
  40 mV_{rms} = 110 mV_{pp} = 15 dBm (±1 dB) into 50 Ω.

5.3.1.12.3 AF Demodulation

a) FM demodulation:

Oscillator adjustment:

- Connect signal generator to ST2: 30 kHz, approx. 20 mV
- DVM check point: ST1.a4
- Vary R19 until the DVM reads 0 V (±20 mV).

Checking the FM demodulation

- Connect signal generator and DVM as for oscillator adjustment.

Table 5-10

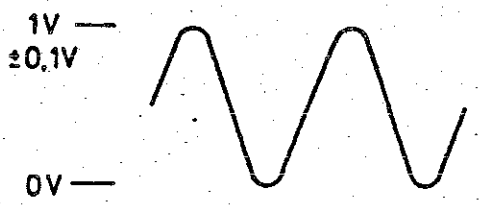
Signal generator frequency	Nominal voltage reading on DVM
25 kHz	-5 V ±0.3 V
27 kHz	-3 V ±0.3 V
29 kHz	-1 V ±0.3 V
31 kHz	1 V ±0.3 V
33 kHz	3 V ±0.3 V
35 kHz	5 V ±0.3 V

b) AM demodulation:

Settings on the ESH 3: AF demodulation 4: A3
Operating mode 38: GEN.OFF

Connect signal generator to ST2 (frequency 30 kHz, level approx. 100 mV, 100% modulation depth).

Oscilloscope check point ST4:



Vary the input voltage between 2 mV and 2 V. The voltage change at ST4 should be < 3 dB.

c) SSB demodulation:

Settings on the ESH 3: AF demodulation 4: A1
Operating mode 38: GEN.OFF
35: AV

Connect signal generator to ST2 (frequency 30 kHz, level approx. 20 mV, unmodulated).

Oscilloscope check point ST1.a3:
Nominal signal 1 kHz AF, approx. 130 mV_{rms} = 360 mV peak-to-peak (±50%).

d) SSB AGC:

Settings on the ESH 3 as for SSB demodulation, but the level at ST2 is about 100 mV.

Switch off the signal generator. It should take approximately 1 s until the AGC voltage at B8 pin 9 drops.

5.3.1.13 Performance Check of the Indication and AF Demodulation Board Y12

5.3.1.13.1 Indication Demodulation

a) Average-value indication:

Feed unmodulated 30-kHz signal V to ST2. The resulting voltages at ST1.a2 are as follows:

Table 5-11

V to ST2	Operating range		
	20 dB	40 dB	60 dB
2 mV	200 ±10 mV	200 ±20 mV	200 ±20 mV
6.3 mV	630 ±20 mV	650 ±40 mV	500 ±40 mV
20 mV	2000 ±10 mV	1100 ±40 mV	800 ±40 mV
63 mV		1550 ±40 mV	1100 ±40 mV
200 mV		2000 ±20 mV	1400 ±40 mV
632 mV			1700 ±40 mV
2000 mV			2000 ±20 mV

Amplitude-modulated signals cannot be directly measured in the 40-dB and 60-dB operating ranges. Use correction curve (Fig. 2-8).

b) Peak-value indication:

If an unmodulated input signal is applied, the same voltage is obtained at ST1.a2 as with average-value indication. A 100% amplitude-modulated signal increases the indicated value by 6 dB as against average-value indication.

c) CISPR indication:

In the frequency range from 10 kHz to 150 kHz, the signal is weighted in accordance with CISPR 3 and from 150 kHz to 30 MHz in accordance with CISPR 1. If unmodulated signals are applied to ST2, the following voltages are obtained at ST1.a2:

Table 5-12

	CISPR 1	CISPR 3
2 mV	217 ±10 mV	200 ±10 mV
10 mV	680 ±20 mV	630 ±20 mV
20 mV	2170 ±10 mV	2000 ±10 mV
Pulse weighting time constants:		
	CISPR 1	CISPR 3
Charging time constant	1 ms	45 ms
Discharging time constant	160 ms	500 ms

5.3.1.13.2 AF Demodulation

a) Demodulation outputs:

- AF output ST1.a3

  Apply 100% amplitude-modulated, or frequency-modulated (frequency deviation 5 kHz), input signal.

  AF output signal ..... 200 mV_{rms} +50 mV (Z_{out} = 5 kΩ)

- AM output ST4

  This output is used for measuring the modulation depth by means of an oscilloscope: 100% modulation depth corresponds to 1 V_{pp} ±3 dB (Z_{out} = 1 kΩ).

- FM output ST3

  At this output, the frequency offset of the 30-kHz input signal can be measured:

  5 kHz deviation corresponds to ±0.5 V (tolerance 0.03 V) (Z_{out} = 10 kΩ).

- Frequency offset output ST1.a4

  Here too, the frequency offset of the 30-kHz input signal can be measured: ±5 kHz offset corresponds to ±5 V (tolerance 0.3 V) (Z_{out} = 10 kΩ).

b) IF amplifier AGC

AM AGC time constant 0.5 s

AO AGC time constant 0.5 s

A1 hang AGC with fast decay

USB hang AGC

LSB hang AGC

c) 4th oscillator

Demodulation mode	Signal generator	Frequency of 4th oscillator
AM	OFF	switched off
FM	OFF	switched off
AO	OFF	30.0 kHz
A1	OFF	31.0 kHz
USB	OFF	31.5 kHz
LSB	OFF	28.5 kHz
any	ON	30.0 kHz

d) 30-kHz output ST5

With 30 kHz ON (GEN.ON), the frequency of the output signal is 30.0 kHz. In the REM. FREQ. (remote frequency measurement) mode, the output signal is synchronized with the input signal at ST2.

Level in both cases ..... 40 mV ±1 dB into 50 Ω

5.3.1.14 Attenuator Control (Y13)

5.3.1.14.1 Supply Voltages

Pin	Voltage	Current
ST3.ab2	Ground	-
ST3.ab1	+12 V ±0.1 V	approx. 2 A

The Attenuator Control (Y13) is preferably checked together with the RF Attenuator (Y16).

For production testing, it is advisable to use a control arrangement that permits the control levels at ST1.a2 to 16 to be switched on as desired. For checking the gating with B1 to B4 at the test points B to K, refer to Table 5-13.

(The attenuation values a are obtained by summing the attenuation values defined by the logic H signals at the control inputs of ST1.)

Table 5-13

Test point	B	C	D	E	F	H	I	K
Attenuator/dB	10	20	40	40	10	20	CAL	1
Attenuation a/dB								
0	L	L	L	L	L	L	L	L
10	H	L	L	L	L	L	L	L
20	L	H	L	L	L	L	L	L
30	H	H	L	L	L	L	L	L
40	L	L	H	L	L	L	L	L
50	H	L	H	L	L	L	L	L
60	L	H	H	L	L	L	L	L
70	H	H	H	L	L	L	L	L
80	L	L	H	H	L	L	L	L
90	H	L	H	H	L	L	L	L
100	L	H	H	H	L	L	L	L
110	H	H	H	H	L	L	L	L
120	H	H	H	H	H	L	L	L
130	H	H	H	H	L	H	L	L
140	H	H	H	H	H	H	L	L
CAL	H	L	H	H	X	X	H*)	X
1	X	X	X	X	X	X	X*)	H

*) No effect, i.e. the last setting is preserved.

It is possible to set attenuation values up to 140 dB in the ESH 3. If, when the ESH 3 is being repaired, there is any doubt as to the proper functioning of the Attenuator Control, it is recommended that the RF Attenuator be removed from the ESH 3, the base plate unscrewed and the functioning of the control be checked by observing the switching state of the contacts (for location of the attenuators, see circuit diagram 303.2813 S). An error can be tracked down with the aid of section 4.1.11.

5.3.1.15 Power Supply

5.3.1.15.1 Access to Circuits

For troubleshooting, the instrument may be operated with the power supply swung out. For this the instrument panelling is first removed. After then removing six screws on the frame, the power supply can be withdrawn horizontally. After the actuating rod of the power switch is pulled off, the power supply can be placed toward the back on the cooling body.

Note! In dismounting the power supply, only the six outermost screws may be removed, since otherwise other parts of the power supply will be loosened.

In remounting the power supply in the instrument, the flat cable must be correctly folded and the actuating rod of the power switch replaced before the power supply is moved into place and screwed to the frame.

The individual subassemblies of the power supply are best tested while connected into the instrument circuit, since all supply and control lines are then attached. The subassemblies can be swivelled apart to permit access to the components. So long as the power supply is operated for only short periods or is only partially loaded, the large heat sinks can be removed.

After the heat sinks of the analog power supply have been unscrewed, all components and test points are accessible. The solder side of the subassembly is accessible after the latter has been unscrewed. The removed subassembly must be supported in a suitable fixture to assure that no shortcircuits are possible.

For measurements on the solder side of the switching power supply board, the cover on the side of the analog power supply must be unscrewed. The analog board remains attached to the cover. For replacement of components in the switching power supply, the board is not removed, instead the entire frame is unscrewed from the rear panel. For this the two large screws on the rear side in the cooling fins and then the six small screws in the frame be removed. The frame can then be swivelled away without having to remove the leads to the rear panel. The rectifier plate must remain in place for operation of the system.

Before reassembly, the correct seating of the socket strip on X30 and the lines on the lead-through filters must be checked. The heat sink on the switching power supply must be provided with heat-conducting paste. Then the frame screws and screws in the cooling fins are loosely screwed in. After lining up the unit the frame is first tightened and then the internal heat sink.

Note! If the internal heat sink is not tightly screwed down, the switching power supply will overheat in operation.

5.3.1.15.2 Adjustment of Reference Voltages

The only adjustment points of the power supply are potentiometers R89 and R95 on the analog power supply board, with which the monitoring and regulator reference voltages can be set.

Note! This adjustment should only be undertaken if really necessary, since other circuits will then also have to be adjusted.

Reference point for all accurate voltage measurements is the ground neutral point X5 on the rectifier board. The adjustment is made by measuring the +10-V supply voltage at a point of the sensing line (motherboard X201A4) and accurately setting it with R95. If the accessories are available, the +10-V supply can also be adjusted by measuring this voltage on the sensing line at points X18.16 or X36.1 of the analog power supply board. After this adjustment, the regulator reference voltage, measurable on test connector X9.1, must have the value +8 V ±20 mV. The monitoring reference voltage at X9.3 must be set to exactly the same value by means of R89.

The other output voltages are determined by fixed resistors and cannot be separately adjusted. The -10-V supply at sensing point X201B4 on the motherboard tracks the +10-V supply with a maximum error of 10 mV. All other voltages must lie within a tolerance limit of ±2% at the power supply. It must be noted that because of voltage drops in the lines, the output of the +5-V supply is 5.5 V at its output terminals. The output voltage of the +30-V supply lies between 31 V and 40 V depending on the loading of the -11-V supply. When the -11-V supply is not loaded, the output of the +30-V supply can drop so low that the H3 LED lights. This is of no significance in normal operation.

5.3.1.15.3 Test Points of Analog Power Supply

The analog power supply has a variety of connectors, some of which are bridged with shorting links.

X31 to X38	.1-.2	connected (comparator inputs)
X5	.2-.3	connected (short-circuit link right)
X9,X10		open
X2,X4,X8,X12	.1-.2	connected for setting 20 V (short-circuit top, ESVP)
	.2-.3	connected for setting 25 V (short-circuit bottom, ESH3)

5.3.1.15.4 Check of Output Currents

In table 5-2 are listed the maximum output currents of the power supply - these may, however, not be drawn in operation. The measured current values must lie within the tolerance range of -10% to +25%.

Table 5-14a Output Currents

Voltage (nominal)	Maximum current cold	Maximum current warm	Shortcircuit current
+5 V	7 A	6 A	6 A
+12 V	4 A	3 A	3 A
-11 V	1.4 A	1.2 A	1.2 A
+33 V	0.5 A	Can only be overloaded for short period.	
+10 V	0.7 A		0.15 A
-10 V	1.3 A		0.33 A
+20 V (ESVP)	0.4 A		0.08 A
+25 V (ESH3)	0.05 A		0.01 A
+30 V	0.06 A		0.06 A

The check on analog supplies with foldback current limiting can only be made with resistors of corresponding power rating. The switching supplies can also be checked with electronic current sinks.

The sensing leads for the +10-V and -10-V supplies must be connected to the proper outputs. If these leads are not connected, the supply voltages will be about 0.3 V too high, although the voltages on the comparators are correct.

5.3.1.15.5 Check of Monitoring Circuit

When the shorting links are removed from X31 to X38, the corresponding LEDs H1 to H8 light. By applying a variable voltage to the pins .2, the limit values of the monitoring windows can be determined. The actual supply voltages can be measured at the same time on pins .1.

Note! The test with X31 may only be made if the internal supply is operating properly, since otherwise the other supplies can be switched into prohibited states.

Because of the interlocking of some of the power supplies, only one external voltage at a time must be applied and the corresponding LED observed. In case of automatic measurement the error messages are monitored at the outputs of these messages and on S1, S2, S3.

Table 5-14b Monitoring Window Data

Connector	LED	Nominal voltage	Lower limit	Upper limit	Max. shift of window
X31	H1	15 V	12.8 V	18 V No mess.	300 mV
X32	H2	24 V	↓20.8 V ↑21.3 V	40 V No mess.	400 mV
X33	H3	30 V	28.8 V	31.4 V	600 mV
X34	H4	25V (ESH3)	23.9 V	26.1 V	500 mV
X34	H4	20V (ESVP)	19.1 V	20.9 V	400 mV
X35	H5	12 V	11.4 V	12.5 V	200 mV
X36	H6	10 V	9.9 V	10.1 V	20 mV
X37	H7	-10 V	-9.9 V	-10.1 V	20 mV
X38	H8	5 V	5.1 V	5.6 V	50 mV

Table 5-14c Message Output Levels

Connector	Nominal voltage	LED	Output on	Pin	Level O.K.	Level Error	Other responses in case of error
X31	15 V	H1	S1	X18.23	0 V	>0.8 V	All the others
X32	24 V	H2	S3	X18.25	0 V	>0.8 V	All except S1,S2,12K
X33	30 V	H3	30 comp.	X14.15	high	low	-
X34	20/25 V	H4	20 comp.	X14.18	high	low	-
X35	12 V	H5	12 comp.	X14.17	high	low	-
X36	10 V	H6	10 comp.	X14.9	high	low	-
X37	-10 V	H7	-10 comp.	X14.16	high	low	-
X38	5 V	H8	S2	X18.26	0 V	>0.8 V	All except S1

The ERROR INT, TRAP and RESET outputs can be monitored simultaneously.
If all voltages are in order, ERROR INT and TRAP are low and RESET is high.

ERROR INT goes high at every error.

TRAP is high during the on-time of D4I (about 100 ms) if S3 responds.

RESET goes low when S2 responds or after TRAP has gone back to low.
RESET then goes high again only after monostable D4II, having been triggered by the negative edge of ERR INT, returns to its off-state.

The output of the 5-V comparator and of monostable D4II can be monitored on X10.

5.3.1.15.6 Notes on Troubleshooting

If the green LED in the power supply does not light, the microprocessor is blocked (by an ERROR message or RESET). The fault can be localized with help of the description for the monitoring circuit in Section 5.1.4. In any case, before any repair is attempted, it should be determined whether the error is the result of external influence (undervoltage, overload).

No LED is lit

If after instrument switch-on no LED in the power supply lights, the cause quite likely is that there is no input to the analog power supply. After check of the AC supply or battery voltage and the fuses accessible on the rear panel, the voltage on capacitor C5 of the rectifier board should be checked with the AC power supply on. Flat connectors X1 and X2 are accessible from the underside of the instrument after the panelling is removed. If a voltage is present, the power supply should be removed from the instrument and the connection to the analog power supply checked. The input voltage should also be present on regulator N5.1 of the analog power supply.

One or more red LEDs lit

The rank order of the error messages as shown in Fig. 5-2 must be observed, i.e. the higher ranking signal must be checked first. If the green LED lights when the load on the power supply is reduced or completely removed, the output currents should be checked against the values in Section 5.2.4.

Before attempting any repairs, the voltages in question and the reference voltages should be checked to eliminate the possibility of a fault in the monitoring circuit. Before opening the switching power supply, the turn-off signals S1, S2, S3 (accessible on connector X17 of the rectifier board) should be checked. If a voltage > 0.8 V is present, the corresponding switching supply is turned off.

After unscrewing the cover of the power supply, the voltages on connector X30 should be checked, in order to eliminate the possibility of a break in the connection between the switching power supply and the rectifier board.
In this condition the signals on all components of the switching power supply can be checked.

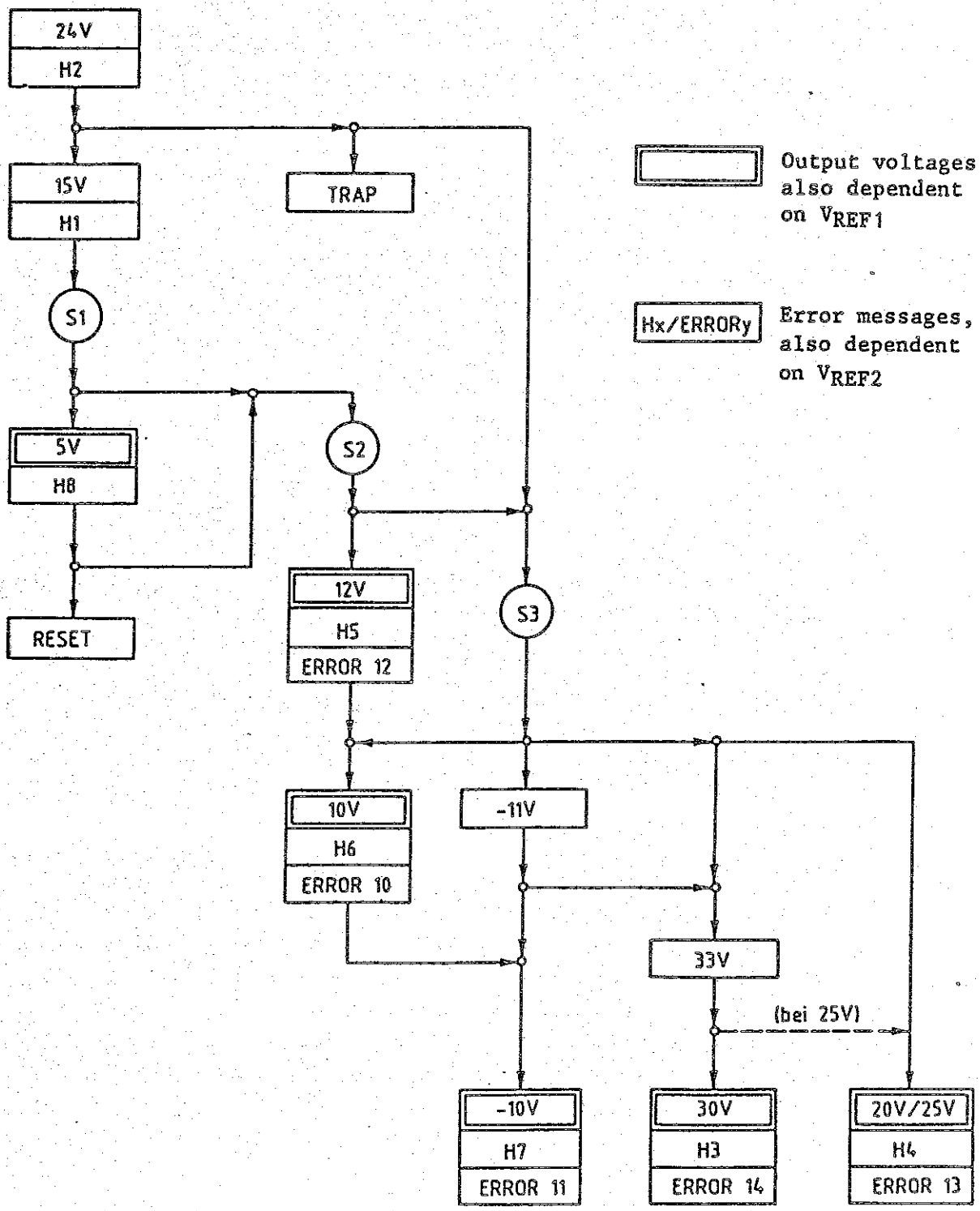


Fig. 5-6 Rank order of supply voltages and error messages

5.3.1.16 Checking the Recorder Control Board

(See circuit diagram 335.9913 S)

5.3.1.16.1 IEC-bus Section

- The IEC bus is simply connected via a flat cable (ST8) from the Computer board (BU8) to the recorder control board. For checking, unplug ST8 and use a continuity tester.

  NOTE: If the recorder control board has to be removed, protect the pins of plugs 7 and 8 against damage by sticking them in pieces of foam plastic.

- Pull out ST7 from BU7.
- Connect logic tester probe (or voltmeter) to ST7 pin 1.
- Switch on receiver and apply +5 V. Check function of the address line (a1).
- Change connections and check a2 to a5 and ton similarly.
- Connect logic tester probe or voltmeter to ST7 pin 7.
- If BU1 pin 1 is shortcircuited to ground, ST7 pin 7 should be at logic L (< 0.8 V).
- Check ST7 pin 8 with BU2 pin 2 to ground, as above.
- Check the remaining pins of ST7, by means of a continuity tester, against the circuit diagram.

5.3.1.16.2 Checking the Demultiplexer

- Unplug ST7.
- Switch on the ESH 3.
- Apply a stable voltage V = 0 to 10 V (e.g. 5 V) to B6 pin 5.
- Deliver logic L to ST7 pin 13 (penlift signal).
- Check in accordance with Table 5-15:

Table 5-15

Recorder	ST7 pin			BU2 pin					BU2 pin +)				
	12	11	10	8	9	10	11	12	10	21	22	23	24
1	H	L	L	V_{in}	X	X	X	X	L	H	H	H	H
2	L	H	L	X	V_{in}	X	X	X	H	L	H	H	H
3	H	H	L	X	X	V_{in}	X	X	H	H	L	H	H
4	L	L	H	X	X	X	V_{in}	X	H	H	H	L	H
5	H	L	H	X	X	X	X	V_{in}	H	H	H	H	L
0.6 to 8	Recorders not active								+) only for penlift				

5.3.1.16.3 Checking the External Reference Switchover

- Check the following levels using a voltmeter or logic tester probe:

Synthesizer 2/pin	Int. ref.	Ext. 5 MHz	Ext. 10 MHz
ST1/a2	L	H	L
ST1/b2	L	L	H

- Check the pulling range of the synthesizer in accordance with 5.3.1.3.4.3.

5.3.1.17 Motherboard (Y18)

Check the Motherboard in accordance with circuit diagram 303.2020 S.

5.3.1.18 RF Attenuator (Y16)

It is recommended that the RF attenuator Y16 be checked together with the attenuator control Y13.

Note: Torque range for SMA socket: 80 to 120 Ncm

- Screw down the six adjustment screws of the base plate all the way.

a) Check the residual attenuation with DC voltage.

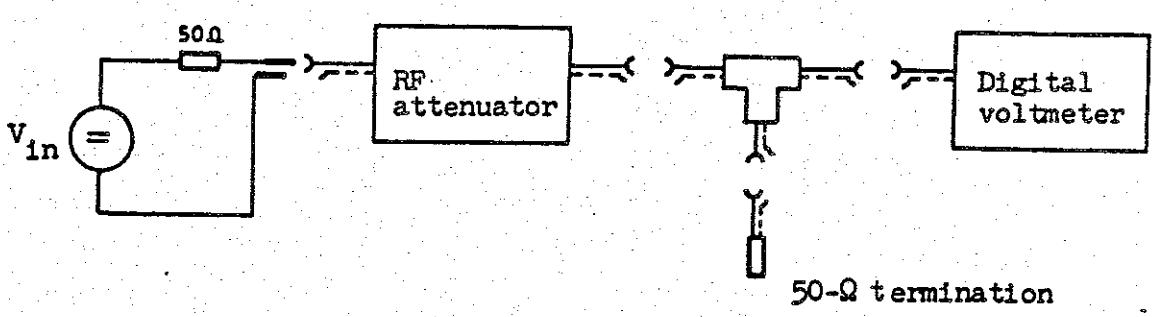
- Set the level switch to 0 dB.
- Measure the resistance between the inner conductor of the input and the inner conductor of the output by means of an ohmmeter with a resolution of 100 mΩ.
- The resistance consists of the contact resistances of the 18 switching contacts and the series resistances of the thin-film conductors. The resistance of the test setup must be taken into account. The resistance R_T should be $\leq$ 800 mΩ. The resulting residual attenuation a_0 is given by the formula

$$a_0 = 20 \log \frac{100}{100+R_T/\Omega}$$ and is < 0.07 dB.

- Then measure the resistance between the inner conductor of the calibration input and the inner conductor of the output. To do so, apply a short switching pulse across the coil of solenoid 7 which initiates calibration of the RF attenuator without switching the 10-dB attenuator pad into circuit. The resistance should be < 500 mΩ.

b) Checking the attenuator pads with a DC voltage

Test setup:



- Connect a constant DC voltage source $V \leq 5$ V with an internal resistance of 50Ω to the input of the RF attenuator.
- Measure the output voltage of the through-connected (0 dB) attenuator by means of a digital voltmeter. The attenuator is terminated with 50Ω.
- Successively set the attenuation values a = 1, 4, 10, 20 and 40 dB. The attenuator control cannot be used for this purpose; instead, short 12-V switching pulses must be applied directly to the terminals accessible on the control board. Open the connection to the attenuator control.

The attenuation actually provided can be calculated from the voltage ratios:

$$a = 20 \log \frac{V\ (0\ dB)}{V\ (a\ dB)} .$$

The maximum permissible attenuation error can be read off the below table:

Attenuator pad/dB	a_{min}/dB	Actual/dB	a_{max}/dB
1	0.98		1.02
4	3.98		4.02
10 (1)	9.96		10.04
10 (2)	9.96		10.04
20 (1)	19.94		20.06
20 (2)	19.94		20.06
40 (1)	39.92		40.08
40 (2)	39.92		40.08

The location of the individual attenuator pads is shown in circuit diagram 303.2813 S.

Since the RF attenuator is used only up to 30 MHz in the ESH2 even though it is designed for frequencies up to 2.7 GHz, there is no need for an RF check (VSWR < 1.2 at input and output in the range 0 to 1000 MHz).

5.3.2 Overall Adjustment

Prerequisites for the adjustment:

- All assemblies must be operational and adjusted as required.
- Remove Filter 2 (Y8), open it and connect it to the receiver via the Service Adapter.

5.3.2.1 Checking the Supply Voltages

Motherboard b23 ..... +5.4 V ±250 mV
Motherboard a22 ..... +10.000 V ±200 mV
Motherboard a23 ..... +12 V ±500 mV
Motherboard a24 ..... +25 V ±130 mV
Filter Control Y6, a24 ..... +30 V ±1.35 V
Motherboard b22 ..... -10 V ±400 mV

5.3.2.2 Checking the Gain of Mixers 1 + 2 (Y9) and Mixer 3 (Y11)

Settings on the ESH 3:

	39:	LIN.
Indicating mode	35:	AV.
IF bandwidth	6:	500 Hz
IF attenuation	40, 41:	40 dB
RF attenuation	40, 41:	50 dB

Connect signal generator (f < 10 MHz, level 80 dBµV ±0.1 dB, 50 Ω) to the RF input 45 of the ESH 3. Adjust the gain by means of R20 on Y11 so that at a medium gain setting (+2 V ±0.2 V) at the base of T1 (Y11) full-scale deflection is obtained.

5.3.2.3 Checking for Equal Gain with the Various Bandwidths

Settings on the ESH 3: See section 5.3.2.4

Permissible difference in the indicated voltage when selecting a new bandwidth ..... ±1 dB

Reference: 500-Hz bandwidth

Adjust the gain with

200-Hz bandwidth: on Y11 using R102
2.4-kHz bandwidth: on Y9 using R69
10-kHz bandwidth: on Y9 using R76.

5.3.2.4 Adjusting Filters 15 and 16 (Y8)

Connect the input of the receiver to a VSWR meter which can be driven from the GEN. output of the ESH 3.

a) Adjusting filter 15 for minimum reflection coefficient

Table 5-16

f	by means of R... on Y6
10.0 MHz	79
11.0 MHz	55
15.0 MHz	70
19.0 MHz	89
19.9 MHz	103

Repeat this adjustment at least once, since the settings interact.

b) Adjusting filter 16 for minimum reflection coefficient

Adjust L78, L79, C162 and C164 in the frequency range from 20.0 MHz to 29.9 MHz.

After the adjustment fasten the coils and secure the windings with a suitable varnish or glue. The board can now have the cover fitted and be inserted in the unit.

Checking the input impedance:
Filters 1 to 14: at least three readings per filter range
Filters 15 and 16: at least every 2 MHz.
VSWR with 0 dB RF attenuation ..... ≤ 2 = < 33%
with RF attenuation > 0 dB ..... ≤ 1.2 = < 10%

5.3.2.5 Checking the Reference Frequency

Tune the receiver to 29.0000 MHz. Switch on the generator and connect to a frequency counter with a frequency accuracy of better than 1×10^{-8}. After a warm-up period of > 5 min, adjust the counter display to 29.0000 MHz by means of R22 on Y1.

5.3.2.6 Adjustment of Calibration

a) Sinewave calibration

Settings on the ESH 3:			
	Indicating mode	35:	AV.
	Operating range	33:	20 dB
	IF bandwidth	6:	10 kHz
	RF attenuation	40, 41:	50 dB
	IF attenuation	40, 41:	40 dB
	Frequency	20:	1 MHz
	Operating mode	38:	TWOPORT
	Meas. time	37:	≥ 0.1 s

Connect suitable precision level meter (50 Ω), such as specially calibrated URV 4 with 50-Ω insertion unit, to the GEN. output 44.

- Set level by means of R84 on Y10.
  Required level ..... 80 dBµV ±0.1 dB
  = -27 dBm ±0.1 dB
- Press CAL. button 15 momentarily (calibration check).
- Connect the GEN. output 44 to the RF input 45.
  Required indication ..... 0 dB ±0.1 dB

b) Pulse calibration (CISPR 3)
over frequency range 10 kHz to 149.9 kHz

Settings on the ESH 3:			
	Indicating mode	35:	CISPR
	RF attenuation	40, 41:	30 dB
	IF attenuation	40, 41:	40 dB
	Frequency	20:	0.1 MHz

- Press CAL. button 15 and hold down (total calibration).
- Feed sinewave signal (0.1 MHz, 60 dBµV ±0.1 dB, 50 Ω) into the ESH 3.
  Nominal indication after fine tuning to
  maximum indication ..... 60 dBµV ±1 dB

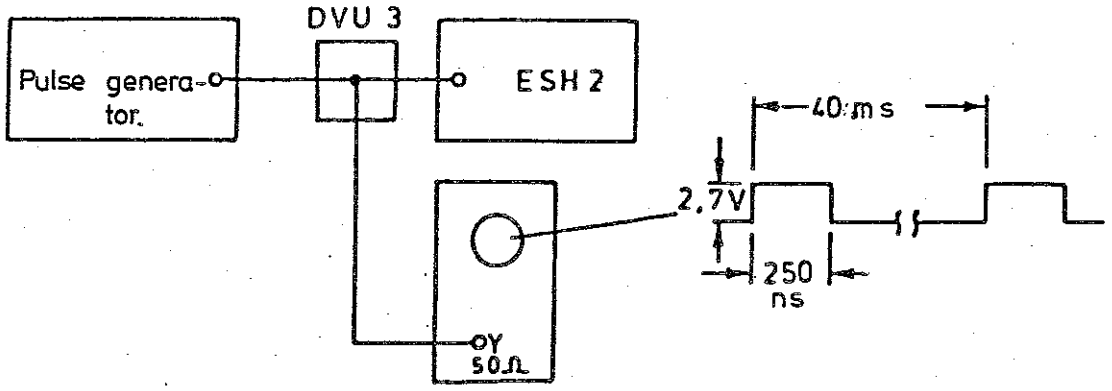
Correct, if necessary, by means of R89 on Y10:

Indicated value too high ⟶ turn R89 counterclockwise ⟶ calibrate ⟶ measure

Indicated value too low ⟶ turn R89 clockwise ⟶ calibrate ⟶ measure.

5.3.2.7 Checking the CISPR 3 Weighting Circuit

Test item:



Connect a pulse generator with an adjustable repetition frequency in compliance with CISPR 3 requirements to the input of the ESH 3. Feed a pulse with a repetition frequency of 25 Hz, a period of 250 ns and an amplitude of 2.7 V corresponding to the CISPR 3 standard pulse

$$V \cdot t = \text{approx. } 1.35\ \mu Vs\ (EMF)$$

into the input of the ESH 3.

Required indication ..... 40 dBµV ±1 dB

When varying the repetition frequency in compliance with the CISPR 3 requirements, the indication on the receiver must be within the CISPR 3 tolerance limits (Fig. 5-5).

5.3.2.8 Pulse Calibration (CISPR 1) over Frequency Range > 150 kHz

Settings on the ESH 3:				
	Indicating mode	35	:	CISPR
	RF attenuation	40, 41	:	30 dB
	IF attenuation	40, 41	:	40 dB
	Frequency	20	:	1 MHz

- Press CAL. button 15 and hold down (total calibration).
- Feed sinewave signal (1 MHz, 60 dBµV ±0.1 dB, 50 Ω) into the ESH 3.

Nominal indication ..... 60 dBµV ±1 dB

Correct, if necessary, by means of R91 on Y10:

Indicated value too high ⟶ turn R91 counterclockwise ⟶ calibrate ⟶ measure

Indicated value too low ⟶ turn R91 clockwise ⟶ calibrate ⟶ measure.

5.3.2.9 Checking the CISPR 1 Weighting Circuit

Same test setup as for CISPR 3.

Standard pulse: V • t = 0.316 µVs (EMF).

This standard pulse with a repetition frequency of 100 Hz should give an indication of ..... 60 dBµV ±1 dB

The calibration pulse generator from Schwarzbeck, Type IGU 2912 supplies a CISPR 2, 4 pulse

$$V \cdot t = 0.044\ \mu Vs\ (EMF).$$

This corresponds to a difference of -17.12 dB from the CISPR 1 pulse. The required indication on the ESH 3 must therefore be ..... 43 dBµV ±1 dB with the output attenuator of the IGU 2912 set to 60 dB.

When varying the repetition frequency in compliance with the CISPR 1 requirements, the indication on the receiver must be within the CISPR 1 tolerance limits (Fig. 5-6).

5.3.3 Final Check of the Receiver Performance Data

Check the logic functions in accordance with section 2.2.4 (operating manual) and the performance specifications in accordance with section 3.2 (service manual).

5.4 Electrical Repair

The easy-to-service ESH 3 is designed to minimize the time required to repair it. However, defective components must be replaced only with the parts designated in the relevant parts lists. Certain restrictions must be observed with the following components:

- The detector diodes GL9 and GL10 on Y10 affect the measurement accuracy and the temperature dependence of the receiver. When a repair becomes necessary, the temperature compensation must be readjusted.
- The attenuator Y16 is a thin-film unit whose components can only be replaced by the manufacturers. No attempt should, therefore, ever be made to repair it. The complete defective attenuator must be replaced.

If a great number of ESH 3s are used at one and the same location, it is recommended that a set of receiver modules be kept as replacement to minimize the down-time of the receiver concerned. The replacement of a receiver module is uncritical as the interfaces within the receiver are precisely defined. (Exception: Filter Control and Filter 2 must be replaced together.)

5.5 Mechanical Repair

Since the receiver contains practically no mechanical parts that are subject to mechanical wear and tear - with the exception of the tuning knob and the carrying handle - little mechanical repair will be required.

A normal service tool kit will do for any mechanical repair work that may become necessary.

5.6 Spare Parts

The parts lists of the various receiver modules in the appendix contain the manufacturer's identification numbers (= order numbers) of all the electrical components used. When replacing ICs, make sure to use an IC from the same manufacturer, if possible, since the differences are considerable in spite of the same designation.

To achieve optimum reliability, the boards and modules used in the receiver undergo rigid quality control prior to final assembly.
Components from other makers, such as resistors, capacitors, diodes, transistors, ICs and displays are required to comply with R&S specifications ensuring optimum reliability. It is therefore recommended that defective components should only be replaced by original components that have been passed by R&S.