4. Circuit Description

4.1 Electrical Function of the Individual Boards

(See block diagram 335.8017 FS as well as overall circuit diagram 303.8017 S sheets 1 and 2)

The RF Test Receiver ESH 3 is a triple heterodyne receiver covering the receiving range from 9 kHz to 30 MHz with 16 subranges set by internally switched filters arranged before the 1st mixer stage. The 1st IF is 75 MHz, the 2nd IF 9 MHz and the 3rd IF 30 kHz. The front panel and the Display (Y1) + Computer (Y2) boards form a mechanical unit. The Synthesizer 1 (Y5) and Synthesizer 2 (Y4) boards produce the required mixer frequencies and determine the receive frequency. From this receive frequency, which is read out on the front panel, the logic switching signals for the 16 different RF filters on the Filter 1 (Y7) and Filter 2 (Y8) boards are produced by the Filter Control (Y6) board. In the Mixers 1 and 2 (Y9) board, the filtered input signal is converted to the 1st and the 2nd IF and passed through IF filters. Conversion to the 3rd IF is accomplished on the Mixer 3 (Y11) board. The indicating range of the receiver is adjusted to the level of the signal to be measured in steps of IF attenuation in Mixer 3 (Y11) and by means of the RF Attenuator (Y16) which is driven from the Attenuator Control (Y13). The Indication and AF Demodulation (Y12) board demodulates the 3rd IF signal and produces a DC voltage proportional to the signal level. For calibration of the receiver, the Calibration Generator (Y10) is provided producing a calibration signal at the receive frequency from the 3rd IF and the various oscillator signals.

The Motherboard is used on the one hand to provide the electrical interconnection between the boards and on the other hand the mechanical support for the boards.

The +5-V supply for the subassemblies Synthesizer 1 and Synthesizer 2 is derived from the +12-V line by means of a voltage regulator.

4.1.1 Display Unit (Y1)

(See circuit diagram 335.8400)

In addition to the keys for operation and setup of the receiver and the associated LEDs for indication of the current device function, the following facilities are provided on the Display Unit:

- 13-digit alphanumeric indication for output of the measured data, entry and output of setting data and output of error messages (13)
- 6-digit display of current receiver frequency (20)

- 3-digit 7-segment displays for readout of the selected RF attenuation (8) and indication of beginning, centre and end of the demodulator operating range (14)
- Analog level indication over selected operating range (14)
- Analog indication of frequency offset of input signal from the receiver centre frequency
- Differential current sink for the suppression of supply voltage disturbances due to heavy load fluctuations.

The alphanumeric indication for output of the measured data and entry and output of setting data consists of 13 5x7 dot-matrix displays which are driven in columns in multiplex operation. For this purpose, the single-chip microprocessor B67 is used which is connected to the main processor via the FIFO store interface B54-B55. The data transfer is interrupt controlled and is accomplished by asynchronously entering and outputting ASCII character strings into and from the first-in-first-out stack store.

The slave processor decodes the ASCII characters against a reference table into the five information columns for the LED dot-matrix displays which are successively loaded into the 13 8-bit latches (B25 to B37) by multiplex clock control of the internal timer of the processor and displayed by triggering the respective transistors T1 to T5. A separate clock cycle drives the decimal points via T6.

In addition to the alphanumeric indication, the microprocessor controls the LEDs for the indication of the selected device functions GL1 to GL37 via the I/O expander ICs B57 to B59. The internal processor software also comprises blinking routines for individual LEDs and for the complete alphanumeric display to identify operator errors and overload of the test receiver.

The 6-digit display of the current receiver frequency (in MHz with fixed decimal point) is obtained by means of the LED ICs B18 to B23. They include latches and decoders as well as integrated current sources for the LEDs. The frequency information is transferred from the output ports of the Computer board via ST1 to the Display Unit.

With the exception of S46 (Local), all the keys are connected to the keyboard and display IC B61 via the demultiplexer B62. The keyboard IC is directly connected via the data and system bus and ST2 to the main processor on the computer board. For certain keys (S8, S16, S19 to S21) automatic key

repetition is provided by the ICs B41 to B45 permitting pulses for the keyboard IC to be obtained at time intervals of first 600 ms, then 300 ms and finally every 150 ms if the key is held down.

The 3-digit 7-segment displays for readout of the selected RF attenuation and indication of the beginning, centre and end of the demodulator operating range (B1, B2 to B4) are also driven and multiplexed by the keyboard and display IC via the demultiplexer B63 and the driver transistors T7 to T13.

The analog frequency offset display consists of 16 LEDs which are driven from the IC B66. The analog level indication consists of 31 LEDs which are driven from B64 and B65. The analog voltage for both displays is taken from the Analog board to the Display Unit via the Computer board (ST1 and ST2). Going outside either end of the operating range and centre tuning are indicated separately via the individual LEDs GL38, GL39 and GL88.

The differential current sink B71-B72 controls the shunt transistor T16 which via R87 levels out load fluctuations caused by multiplexing and the changing indications, thus suppressing interference on the 5-V supply line of the test receiver.

4.1.2 Computer Board (Y2)

(See circuit diagram 335.8800 S)

The microprocessor B2 on the Computer board is the heart of the digital control circuit of the Test Receiver ESH 3. The data bus, the address bus and the control lines of the processor are buffered via the driver ICs B1, B3 and B6. The Reset input is directly connected to the +5-V voltage monitor of the analog power supply to ensure a defined start of the program run when switching on the receiver.

Since the lower addresses are multiplexed with the data bus in the 8085 processor, the octal latch B5 is used as an intermediate address memory. The program memory consists of four 4-kbyte EPROMs and additional memory chips on the Memory board which is connected to the Computer board via BU4 and ST3. The entire lower 32-kbyte address area is reserved for the resident program range. Address decoding takes place via B4 in 4-kbyte steps.

The upper 32-kbyte address space serves for controlling the peripherals, the I/O ports and the RAM. Address decoding takes place via B7. For the I/O ports the decoders B23 to B25 are also used, in conjunction with the I-O/M control line of the processor.

The RAM capacity is provided by a 512-byte CMOS memory (B9-B10-B12-B13) which is powered from the NiCd battery BA1 while the receiver is switched off to safeguard the data. Moreover, a 256-byte volatile working memory is provided on the peripheral chip B30 which can be used for the stack area and for intermediate and auxiliary variables.

The complex peripheral chip B17 connects the microprocessor data bus to the IEC-625 interface located on the rear panel of the test receiver. Data transfer in both directions is interrupt controlled and takes place via the 16 internal write and read registers of the IEC-bus IC. The eight data lines, five control lines and three handshake lines are terminated in accordance with the standard by the special drivers B18 to B21 which are connected via BU8 to the chart recorder control circuit and via the rear panel socket to the IEC bus.

The IEC-bus address plus the code for the chart recorder, if used, is read in via BU7 and input port B46 when switching on the receiver and acknowledges through output port B45. A change in the input data is recognized by the 8-bit comparator B49 and converted into an interrupt request which is sent to the processor. The processor, in turn, reads in the new information, processes it and returns it via the output port. The same principle is used to process the test antenna/probe code and applicable conversion factor at the antenna supply socket 47 via ST12 and recognize a change, if any (B47, B48 and B50).

The priority encoder B82 and the 8-bit register B31 handle the interrupt requests and the hardware side of generating the required start addresses RST1 to RST7. Some interrupt lines are gated with the output port B80 via a logic AND function so that these interrupts can be disabled during certain software routines by using a suitable bit pattern.

On account of their high priority, overload indication from the mixers, the monitoring circuits of the oscillator and synthesizer loops and the quasi-continuous tuning control signal are applied to the separate interrupt inputs RST5.5 to RST7.5 of the microprocessor. The signals from the monitoring circuits can be read in at the input port B54 and the signals from the comparators for the power supply voltages in the analog power supply ST9 can be read in at the input port B53.

The line from the STOP key 28 is brought out separately as is that from the LOCAL key 24 which is not connected to the keyboard unit of the front panel; they are debounced and taken via the flip-flop B55 to the input port B81.

Quasi-continuous tuning of the Test Receiver ESH 3 is effected via the tuning sequencer 568.7811 whose output signals are routed via ST 11. The pulses of the Hall sensors of the tuning sequencer are conditioned by B64, B66 providing the CLOCK and UP/DOWN signals for the binary counters 357 and 358.

The current count can be polled by the microprocessor via the input port B56. Every first count pulse arriving after a readout operation of the processor triggers the monostable B71, which produces an interrupt request via the flip-flop B65 with a delay of about 50 ms. This prevents continual, unnecessary interrupting of the main program during fast tuning.

The output ports B33 to B35 are used for outputting the current receiver frequency to the front panel display and to the two synthesizers. The remaining logic signals for setting the RF circuitry are produced at the output ports B36 to B38 and B51 and B52.

In addition, two D/A converters, which furnish the analog output values for driving a YT, XY or radiomonitoring receiver, are provided on the computer board. The receive frequency is taken via output ports B43 and B44 to the 10-bit D/A converter B40, whose analog output is buffered by the operational amplifier B41. The Y analog voltage for level indication is produced by the 8-bit D/A converter B39, which obtains its input information from output port B42. It is also buffered via an operational amplifier. The logic signals for recorder control (pen lift, format advance) from port B44, and the two analog voltages, are taken via BU7 to the recorder control output on the rear panel of the receiver. The ground of the D/A converters and the ground of the A/D converter circuit are run separately from the general digital ground to avoid interference on these lines.

The A/D converter circuit consists of the sample/hold amplifier B77, the A/D converter proper B26 and the peripheral chip B30, whose port lines are used for reading in the converted analog voltage and driving the converter ICs. The +5-V reference voltage is obtained from the high-accuracy +10-V supply

via the op-amp B22 and T1. The divider chain B27 and B28 produces the 250-kHz clock frequency necessary for the 10-bit A/D converter. The flip-flops B29 ensure synchronization of the start/stop signals with the clock frequency.

The data bus of the microprocessor and the control lines are taken to the front panel via BU2, where they are connected to the slave processor for controlling the alphanumeric readout and to the keyboard and display IC for scanning the keys.

4.1.3 Analog Circuit (Y3)

(See circuit diagram 336.0710 S)

4.1.3.1 General

The Analog circuit is used to select the various demodulated voltages to match the output levels and the level to the A/D converter as well as for evaluation of the various signals (e.g. logarithmization, frequency deviation and modulation depth measurement, control of analog level and offset indication).

All circuit paths are controlled via CMOS switches. Except for a few gate circuits (which can be readily seen in the circuit diagram), the µP system of the ESH 3 handles the control of the circuit via output ports; i.e. gating required for the various measurement routines is accomplished via software.

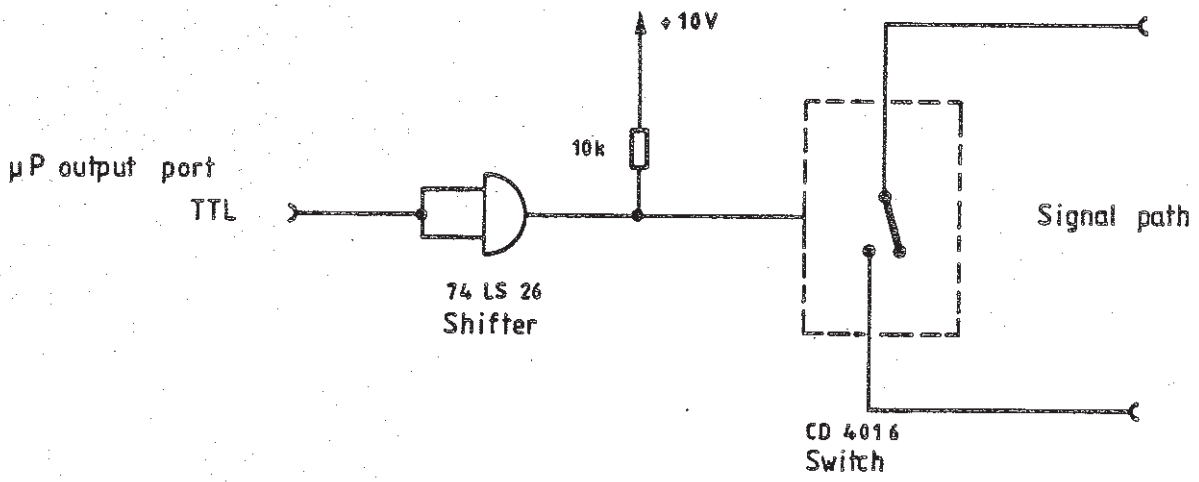


Fig. 4-1 CMOS switch control

4.1.3.2 Signal Path for Level Measurement

The demodulated signal is applied to the input via ST1/17a. Window comparator B1/I, B1/II delivers logic H to pin 21b when the input voltage has reached 2 V ±2 mV at the end of the Cal. command. The analog memory B1 in the 3rd mixer is used for this purpose with the control amplifier B1/III. In the CISPR 1 and CISPR 3 modes the comparator B1/IV supplies a negative output voltage to the gate of T10 which is thus cut off increasing the charging time constant for the analog memory.

With $\overline{\text{CISPR}}$ (= $\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$) the input signal is applied via the switch B6/I or with CISPR via pin 17b, B6/II to the non-inverting amplifier B2/I, which in conjunction with B2/II, B6/III, B6/IV and B7/I forms a programmable amplifier whose switchable gain +1 and +2 can be measured at test pin 18a (for switch control see Fig. 4-1).

B17, T2, B18, B3/I form a logarithmic converter with an input or output voltage range from 0.4 to 4 V. The linear signal is applied via B7/III, and the logarithmized signal via B7/II to the amplifier B3/II which is used as a low-pass filter. Output 7a is used for driving the LED array used for the analog level indication. If $V < 0.355$ V, the comparator B3/III causes via T3 the min.-level LED to light and if $V > 3.55$ V, B3/IV causes via T4 the max.-level LED to light. From the output of B2/I, the signal is applied via B8/III to the sample & hold amplifier for measuring the minimum and maximum levels for AM measurement or via B20/I and B14/III directly to the sample & hold amplifier for level measurement.

4.1.3.3 Signal Path for Frequency Offset Measurement

The offset voltage from -5 V to +5 V is applied via ST1/14b to the differential amplifier which supplies an output voltage from 1 to 4 V. This output voltage is available at 11a via the amplifier B4/IV which is provided with a low-pass filter. B4/II is a calibration amplifier for B19 (analog memory). It is activated through B13/I and T5 during frequency offset calibration process, charging the storage capacitor in B19, the voltage on which controls B4/I.

The calibrated frequency offset voltage of +5 V is output via 8b.

The window comparator B5/I to B5/II supplies a logic L signal to output 5b when the ESH 3 is tuned to centre frequency, or controls the center-tuning indicator via T9. The frequency offset voltage is applied via B8/I and the buffer amplifier B14/III to pin 3a (to sample & hold amplifier).

When measuring frequency deviation, B21 and B14/I are activated for positive peak deviation and B22 and B14/II for negative peak deviation.

B9/I and B9/II serve for discharging the peak-value rectifier.

4.1.3.4 AF Amplifier

The AF is applied to the DC-voltage-controlled volume control B25 via 18b. B23 is the integrated AF amplifier which is switched in via T7 and T8.

In Table 4-1, the logic functions are listed that are required for switching on the desired CMOS switch (+10 V at the control input).

Table 4-1

B6/I	:	$\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$
B6/II	:	CISPR moving-coil meter simulator = CISPR 1 V CISPR 3
B6/III	:	CISPR 1 V CISPR 3 V PEAK (3 s) V Log 40 V LOG 60
B6/IV	:	AV $\wedge$ 20 dB = CISPR 1 $\wedge$ CISPR 3 $\wedge$ PEAK (3 s) $\wedge$ Log 40 $\wedge$ Log 60
B7/I	:	PEAK (3 s) V Log 40 V Log 60 V CISPR 1 V CISPR 3
B7/II	:	$\overline{\text{Log 40}} \wedge \overline{\text{Log 60}}$
B7/III	:	Log 40 V Log 60
B8/I	:	$\overline{\text{Deviation}}$
B8/II	:	$\overline{\text{m}}$
B8/III	:	m
B9/I	:	Discharge
B9/II	:	Discharge
B20/I	:	$\overline{\text{Level}}$
B20/II	:	$\overline{\text{m, f(+)}}$
B20/III		$\overline{\text{m, f(-)}}$

4.1.4 Synthesizer 2 (Y4)

(See circuit diagram 303.7850 S)

This subassembly consists of

- the 60-MHz reference oscillator,
- the interpolation oscillator for the synthesizer 1 and
- the second mixer oscillator (66 MHz).

4.1.4.1 60-MHz Reference Oscillator

The 60-MHz reference oscillator is a high-precision crystal oscillator using transistor T10, the temperature of the crystal being internally controlled by means of a PTC resistor. This oscillator crystal reaches its final accuracy within 30 seconds thanks to its low thermal capacity.

The buffer T11

- converts the interpolation oscillator 5.0 to 5.0999 MHz up to 65.0 to 65.0999 MHz and
- drives the ECL divider B31 (functions as a 1/10 divider).

B33 (1/10) is driven via B32 (1/6). It supplies a reference frequency of 100 kHz which is taken to the Synthesizer 1 (Y5) via the motherboard. The other reference frequencies, 1 kHz for the interpolation oscillator and 500 Hz for the 2nd oscillator, are produced via the divider chain B34, B42 and B41. A further 500-Hz reference output on the motherboard supplies the filter control board, the calibration generator, the 3rd oscillator and the A1 demodulator.

The frequency of the crystal oscillator can be varied in the internal operating mode by applying a DC voltage to the crystal fine-tuning circuit GL30, GL31 and L70. For crystal oscillator adjustment procedures see section 5.3.1.4. The typical temperature stability of the oscillator is about $\pm 4 \times 10^{-6}$ over the temperature range from -10 to +45°C. The maximum tuning error at the highest receive frequency (29.9999 MHz) is thus about ±120 Hz. To fulfill still more stringent frequency accuracy requirements, it is possible to synchronize the ESH 3 via the BNC socket EXT. REF. 55 with an external standard frequency of either 5 or 10 MHz. Depending on the external reference frequency, the division ratio of the switchable divider B39-B38-B40 is set to either 50 or 100 by means of the switch 55 on the rear panel of the receiver. The phase is compared in the phase discriminator B36. Integrator B35 produces the control voltage for the crystal fine-tuning circuit, which is applied via B37 (B37 acts as changeover switch between the variable voltage from the Display Unit and the synchronization voltage).

4.1.4.2 Interpolation Oscillator

The low-microphony interpolation oscillator T3 delivers an adjustable frequency of 50.000 to 50.999 MHz. Via the buffer stages T4-T7-T8 an ECL 1/10 divider (B21) is driven so that at the output of T9 a signal of 5.0000 to 5.0999 MHz is available, with microphony and sideband noise improved by a factor of 10, for conversion in BM1. Another ECL divider (B19) is driven in parallel with B21. Together with B20 and the necessary logic control it forms a 1/100 or 1/101 divider, which is driven via the 2-decade down counter B24 and B25. The divider is preset by the frequency-setting of the receiver and the 1-kHz and 0.1-kHz values for frequency tuning. In addition, the up/down counter controls the division ratio of B18 - adjustable between 500 and 509 -, the first two decades of this division ratio being hardwired. The output frequency from B18 is compared with the reference frequency of 1 kHz in B16. The current pulses from the phase comparator B16 are integrated in the control amplifier B15 and control the varicaps in the oscillator T3 via an appropriate filter network. B17 produces a signal which gives an indication of synchronization of the overall control loop. The functioning of this circuit is explained in some detail in section 4.1.10. The functioning of the various synthesizer loops is explained by a tuning example given in section 4.1.5.

4.1.4.3 Mixer Oscillator

The signal of 66 MHz required for conversion from 75 MHz to 9 MHz is derived from a crystal oscillator whose frequency of which can be varied by ±1.5 kHz for SSB reception.

The buffer T2, which is driven by the crystal oscillator T1, supplies 7 ±2 dBm to the 2nd mixer on the board Y9 and at the same time controls the ECL divider of the synchronization circuit B1. This control circuit operates analogously to that of the interpolation oscillator, but the reference frequency is only 500 Hz and the division ratio 132000 ±3 (driven via B9).

4.1.5 Synthesizer 1 (Y5)

(See circuit diagram 303.7715 S)

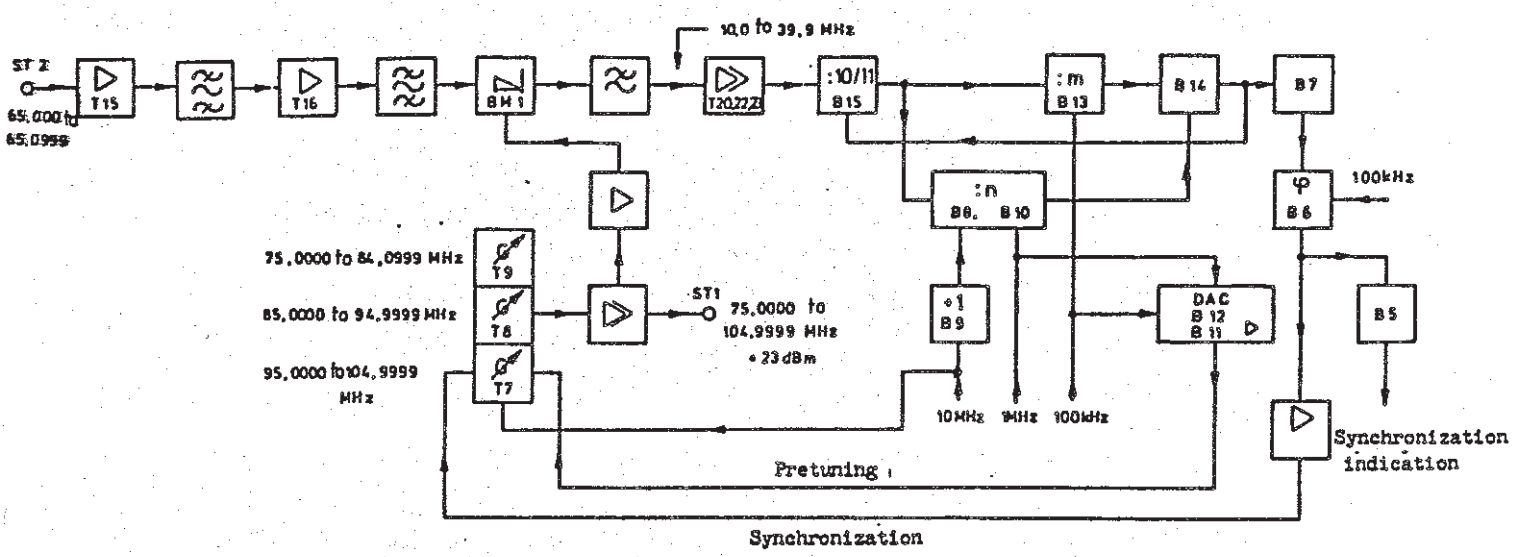


Fig. 4-2 Block diagram of the Synthesizer

The interpolation signal, of frequency 65.0 to 65.0999 MHz, supplied by the synthesizer 2 (Y4) is applied via ST2 to a selective amplifier with a bandwidth of about 1 MHz. When the signal has passed through the amplifier T15-T16, it is largely free from mixer products (60 MHz) and the 2nd sideband (55.0 to 54.9001 MHz), and it is mixed with the signal of the 1st BFO of the ESH 3 (75 to 104.9999 MHz) in the mixer BM1. The resulting sum product is terminated via a high-pass filter and the difference product passes via a low-pass filter to the amplifier T20 to T23 where it is boosted and converted to ECL level. This signal (10.0 to 39.9 MHz) is divided down to about 1 to 4 MHz in the IC dividers (SP 8695B) (1/10 or 1/11), and divided down to 100 kHz in the programmable low-power Schottky dividers with a division ratio adjustable from 100 to 399. B7 acts as a pulse stretcher. B9 adds "1" to the most significant digit of the applied receive frequency to equalize the receive frequency and the division ratio. The phase of the divided-down signal is

compared in B6 with the phase of the 100-kHz reference frequency from synthesizer 2. B5 produces a signal which indicates synchronization of the control loop (LOW = not synchronized, HIGH = synchronized). The output stage of the phase discriminator B6 drives the control amplifier B3, which acts as an integrator, with current pulses depending on the phase relationship of the two signals.

The 1st oscillator of the ESH 3 comprises three oscillators each of which covers about 10 MHz. The oscillator required is selected by appropriate gating circuits fed from the most significant digit of the programmable divider. The practically noisefree oscillators are coarsely pretuned (B12, B11) with the aid of a D/A-converted voltage derived from the 100-kHz and 1-MHz decades. This same voltage is also applied to the Filter control board Y6 and is 0 V for 0 x 1 MHz and 0 x 100 kHz and +7.5 V for 9.9 MHz. Largely freed from residual AC voltage by an appropriate filter, the D/A voltage controls the series-connected quad diodes of the individual oscillators. Synchronization is carried out by the voltage arriving from B3, which has been largely freed from residual AC voltage caused by the 100-kHz reference frequency and its harmonics. The control bandwidth is approximately 500 Hz which cuts out the greater part of the microphony of the oscillators brought about by mechanical vibrations. Sideband noise is about 138 dB/1 Hz 10 kHz away. The low-noise amplifier T10-T11-T12 boosts the oscillator signal to about +23 dBm in the frequency range 75 to 105 MHz, which is then fed to the 1st mixer (in Y9) of the receiver.

Numerical example:

The receiver is tuned to the frequency 12.3456 MHz. The 123 digits arrive at the synthesizer 1 (Y5). A further "1" is added to the "1" by means of B9 which makes a "2". This "2" switches on the oscillator by means of T8 (85 to 95 MHz) via B1, B2, T2, T5 and sets the presettable down counter B8. The figure "2" of the frequency setting is taken to B10 and sets it as the figure "3" sets the counter B13. (B12 converts the digital information "23" to a proportional DC current which in turn is converted to a DC voltage by B11, which among other things coarsely tunes the 1st oscillator.) B15 functions as a 1/10 or 1/11 divider which is kept in the 1/11 mode by B13 until B13 has counted down to "0". It is changed over to the 1/10 mode via B14 III. The preset counter chain B10, B8 is driven in parallel with B13. When it has counted down to "0", it sets B15 again to the 1/11 mode via B14 IV and the process starts again.

The effective division ratio for the above example:

$$\text{division ratio } 1 = 3 \times 11 + (22 - 3) \times 10 = 33 + 190 = 223.$$

The figure combination "456" is delivered to the synthesizer 2 (Y4). The divider B19/B20 functions as a 1/100 or 1/101 divider. The "6" sets the down counter B24, the "5" sets B25, the "4" sets B18, the next to most significant digits of which are fixed at 50... . Hence, the effective division ratio is:

$$\text{division ratio } 2 = 56 \times 101 + (504 - 56) \times 100 = 5656 + 44800 = 50456.$$

The oscillator T3 is synchronized to the frequency 50.456 MHz. This frequency is divided by 10 (B21) and after mixing it with 60 MHz 65.0456 MHz is obtained.

The lock-in frequency of the 1st oscillator is given by

$$223\ f_{\text{ref 1}} + 65.0456 \text{ MHz} = 87.3456 \text{ MHz}.$$

Since the 1st oscillator operates at a frequency that is higher than the receive frequency f_{receive} by the 1st IF:

$$f_{\text{receive}} = f_{\text{1st osc.}} - f_{\text{1st IF}} = 87.3456 - 75.000 = 12.3456 \text{ MHz}.$$

Typical pulse shapes and durations at points of major interest for the above setting of synthesizer 1 are shown in Fig. 4-3.

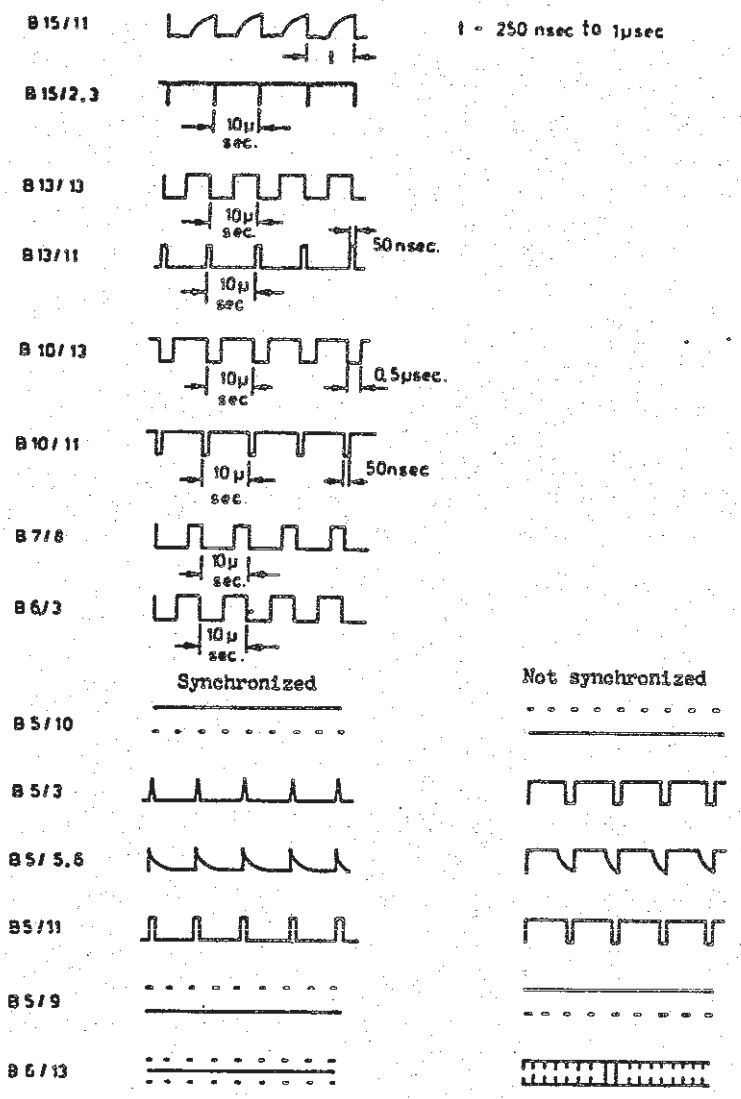


Fig. 4-3 Typical pulse shapes and durations

4.1.6 RF Preselection

The RF preselection in the ESH 3 consists of three related boards:

Filter Control (Y6)
Filter 1 (Y7)
Filter 2 (Y8)

4.1.6.1 Filter Control (Y6)

(See circuit diagram 303.7915 S)

The Filter Control performs the following three main tasks:

- Determination and selection of input filter required for the current tuning frequency.

- Generation of a tuning voltage for the tracking filters in the frequency range 10 to 29.99 MHz from the D/A-converted pretuning voltage fed to the 1st oscillator.
- De-energizing filter relays during setting procedure.

The total frequency range of the ESH 3 is subdivided into 16 filter ranges, the ranges 1 to 14 being fixed tuned while ranges 15 and 16 are tracking.

Table 4-2

Range	f_1 (MHz)	f_2 (MHz)
1	0.01	0.1499
2	0.15	0.1999
3	0.2	0.2799
4	0.28	0.3899
5	0.39	0.5399
6	0.54	0.7499
7	0.75	1.0499
8	1.05	1.4499
9	1.45	1.9999
10	2.0	2.6999
11	2.7	3.6999
12	3.7	5.1999
13	5.2	7.1999
14	7.2	9.9999
15	10.0	19.9999
16	20.0	29.9999

where f_1 is the lower cutoff frequency of a range and
f_2 is the upper cutoff frequency of a range.

The Filter Control board receives the tuning frequency read out on the front panel via the Motherboard (Y18) in the form of 14 bits for the upper four decades:

10-MHz decade (2 bits)
1-MHz decade (4 bits)
100-kHz decade (4 bits)
10-kHz decade (4 bits).

Two diode matrices on the Filter Control board store the 16 lower and the 16 upper cutoff frequencies. The ESH 3 determines which range must be selected as follows:

By comparing the magnitude of the tuning frequency f_M with that of the lower cutoff frequency f_1 (in B1 to B4) and that of the upper cutoff frequency f_2 (in B5 to B8) of the particular range selected, the procedure is controlled by the following simple mathematical functions:

a) $f_M > f_2$:
The selected range is too low.

b) $f_M < f_1$:
The selected range is too high.

c) $f_M > f_1$, but $< f_2$:
The selected range is correct.

The ranges are switched by applying a 500-Hz clock pulse to a decade up/down counter (B9) which controls a 1-out-of-16 decoder (B10). The decoder B10 drives the diode matrices and the switching transistor for the selected range. The direction of the B9, as well as its inhibition after the range determination has been accomplished, is controlled by B11. The transistors T1 and T2 prevent the range relays from being successively cut in after the receiver has been switched on for first-time adjustment.

For generation of the tuning voltage for the ranges 15 and 16, a DC voltage between 0 and +7.5 V, produced in the Synthesizer 1 (Y5) from the 1-MHz and 0.1-MHz decades by D/A conversion, is applied to the Filter Control board (Y6) via the Motherboard (Y18). It is converted to a voltage between +3 and +25 V by a network made up of resistors and operational amplifiers B12 to B14, the input/output relationship of this network being chosen so as to linearize the voltage/frequency characteristic of the tracking filters.

4.1.6.2 Filter 1 (Y7)

(See circuit diagram 303.7015 S)

Filter 1 (Y7) contains the filter ranges 1 to 8 (corresponding to the frequency range 10 kHz to 1.45 MHz). The tasks of the filters 2 to 8 are identical with those of the filters 9 to 16. Except for filter range 1 (10 kHz to 150 kHz), which covers more than one decade, special circuitry has been added to improve the harmonic distortion of the input mixer.

4.1.6.3 Filter 2 (Y8)

(See circuit diagram 303.7415 S)

The subassembly Filter 2 (Y8) contains the filter ranges 9 to 16 (corresponding to the frequency range 1.45 to 29.9999 MHz).

The tasks of the filters are as follows:

- Improve the harmonic distortion of the 1st mixer.
  This means the filter has to provide attenuation at frequency $f_K = \frac{f_2}{2}$, approximately 20 dB with the filters selected.
- Limit the pulse bandwidth (6-dB bandwidth) at the receiver input, above all in the frequency range 10 to 30 MHz to relieve the 1st mixer.

If a range > 8 is selected, the individual filter ranges are switched on via the reed relays RS17 to 34 and the filter 1 is cut off.

4.1.7 1st and 2nd Mixers (Y9)

See circuit diagram 303.6019 S (model 52)
839.9035 S (sheet 1 and 2) (model 56)

Note: The figures given in brackets refer to model 56 (e.g. T2 (V111) denotes transistor T2 in model 52 and V111 in model 56).

This board largely determines the dynamic characteristics of the ESH 3 (harmonic distortion, intermodulation, 1-dB compression, crossmodulation) as well as its performance with respect to image-frequency rejection, oscillator reradiation and IF rejection. The input signal passes through a 9-section Chebishew low-pass filter with a cutoff frequency of about 35 MHz which ensures a rejection of the oscillator frequency from 75 to 104.9999 MHz and of the image frequency from 150 to 179.999 MHz of better than 70 dB. From there, the signal passes via a link to the first mixer which, for model 52, is a high-power mixer (B1) receiving via ST3 an oscillator power (+23 dBm) from the synthesizer 1 (Y5). The 1st mixer of the ESH 3 (model 56) is made up of an 8-diode IC V101 and the balance-to-unbalance transformers T4 and T5. The oscillator power is provided (+23 dBm) via T4. The V101 amplifier generates a 50 Ω termination for the LO gate for all oscillator frequencies. The RF signal is routed to the 8 diodes and the IF signal is taken off via T5. An optimum symmetric design and a specially selected group of 8 diodes ensure an LO suppression of the mixer of > 66 dB. The reduced oscillator power for the reconversion in the tracking generator is available at ST4 (X4) via R94, R95 (R208, R209).

The signals generated in the IF gate of the 1st mixer (above all $f_{1st\ osc}$/ $f_{sum} = f_{1st\ osc} + f_{receive}$, $f_{difference} = f_{1st\ osc} - f_{receive} = f_{IF} = 75$ MHz) are routed to the first IF amplifier T1 (V111) and the overload detection circuit T2 (V200) via ST9 (X9). This circuit simultaneously amplifies f_{sum} and $f_{difference}$ and - after rectification - takes them to a fast comparator B4/I (N4/A) whose rise time is low as against the maximum RF bandwidth of the receiver. The output pulse from the comparator is taken via a pulse stretcher (B8/I) to the Control Board (Y3) for further processing.

T14 (V140) and T15 (V150) amplify the 1st IF with a bandwidth of approx. 2 MHz. The IF signal, e.g. for an IF panoramic monitor, is available at the output ST13 (X14). The IF signal amplified by T1 (V111) passes through a diode limiter (for protection of the crystal filter B2), an attenuator and the following lowpass filter (for suppression of self-generated spurious) to the two-stage low noise amplifier T3 (V300) and T4 (V500). The following lowpass filter suppresses additional self-generated spurious.

The 75-MHz IF signal is converted to the 2nd IF of 9 MHz in the 2nd mixer with the aid of the 2nd oscillator whose frequency is 66.000 MHz, 66.0015 MHz or 65.9985 MHz depending on the type of demodulation. The oscillator power of +7 dBm = 5 mW is applied via St5 (X5). A reduced oscillator power is available at ST6 (X6) for reconversion in the calibration generator (Y10). The sum product $f\Sigma$ = 75 MHz + 66 MHz = 141 MHz obtained at the output of the mixer is amplified in T6 (V60) and after rectification, comparison and pulse stretching taken to the Control Board (Y3). The difference product 75 MHz - 66 MHz = 9 MHz separated by means of the series-resonant circuit C31, C32 and L17 is taken to the amplifier T11 to T13 (V110, V120, V130) via the low-noise and high-level amplifier T7 to T10 (V700, V800, V90, V100) by means of the diode switch for the IF bandwidths and subsequently via a lowpass filter to the output St7 (X7). The maximum IF bandwidth is determined by B2 (6-dB bandwidth about 9.5 kHz) and the two next smaller bandwidths by B7 and B6.

4.1.8 Calibration Generator (Y10)

(See circuit diagram 303.6319 S)

The calibration generator performs the following tasks:

a) Produces temperature-independent input signal of constant level at the tuning frequency of the receiver for calibration of receiver gain (output ST1: -67 dBm).

b) Supplies a second signal of the same frequency and at a level that permits two-port measurements over as wide as possible a level range (output ST2: -27 dBm).

c) Supplies a filtered amplitude-limited output signal at the exact frequency of the input signal (but displaced in phase due to internal time delays) for remote frequency measurements (output ST2: -27 dBm).

4.1.8.1 Sinewave Calibration with AV., PEAK Indication

The signal (4th oscillator with sinewave calibration or the limited last IF with remote frequency measurement) applied to ST4 is mixed with the 3rd oscillator:

$$f_{3rd\ IF} + f_{3rd\ osc.} \longrightarrow f_{2nd\ IF}.$$

The signal obtained at the 2nd IF is so heavily attenuated at ST5 by the well-balanced design of the mixer B1, the return loss of T2 and the attenuator R2-R3-R4 that it does not disturb the ESH 3's indicating circuitry.

$f_{2nd\ IF}$ is boosted in T1. Its spectrum can be improved to meet stringent requirements with respect to suppression of non-harmonic spurious frequencies for special applications, by retrofitting a filter. After further amplification in T5, the 9.0-MHz signal is taken to B3 where it is mixed with the 2nd oscillator which obtains its required level from the two-stage amplifier T3, T4 with a high return loss.

The signals at f = 66 MHz $\pm$9 MHz are amplified in T7 and taken to the filter B4 which passes them on to T12 almost unattenuated on account of its selectivity about the 75-MHz component (= $f_{1st\ IF}$). The boosted 75-MHz signal is applied to T14 whose gain is adjustable by means of GL6. In B5 the 75-MHz signal is mixed with the 1st oscillator signal, which is coupled out via the non-interactive amplifier T13, T15.

As a result, a signal is obtained at the tuning frequency of the receiver:

$f_{receive} = f_{1st\ osc.} - f_{1st\ IF}$ = 10 kHz to 30 MHz. It passes through a 7-section Chebishev low-pass filter which heavily attenuates $f_{1st\ osc.}$ and $f_{1st\ osc.} + f_{1st\ IF}$, and is then taken to the broadband amplifier T16-T17-T19-T20. The boosted signal is rectified in GL10 and after temperature compensation by means of GL9 and B7 its voltage is compared with the variable voltage at the input of B6/I. The resulting difference voltage is amplified in B6/I making for frequency-independent level control. Addition of a temperature-dependent adjustable current to the currents into the + or - input of B6/I provides temperature compensation.

The output signal from T19-T20 (-1 dBm) is split into two paths:

- Path 1 (ST2) is used for two-port and remote frequency measurements
- Path 2 (ST1) is used for internal calibration of the receiver.

R110 (CAL.CORR.) permits the readout to be set to 80 dB(μV) when making two-port measurements.

4.1.8.2 Pulse Calibration (CISPR 3: f < 150 kHz; CISPR 1: f ≥ 150 kHz)

The 500-Hz TTL signal supplied by synthesizer 2 (Y4) is divided by 20 (CISPR 3) or 5 (CISPR 1) in a programmable 1/5 or 1/4 divider. Needle pulses with a pulse repetition rate of 25 or 100 Hz are produced, whose pulse width is adjustable with R89 (CISPR 3) or R91 (CISPR 1). R124 is used for temperature compensation. The output pulse from B12 passes to the voltage follower T21 and via RS1 to the calibration output ST1.

According to CISPR 3, a pulse of 13.5 µVs is required for calibration which should give an indication of +60 dB(µV) = -47 dBm at an IF bandwidth of 200 Hz.

According to CISPR 1, a pulse of 0.316 µVs is required for calibration which should likewise give an indication of +60 dB(µV) = -47 dBm at an IF bandwidth of 9 kHz.

Since the Receiver ESH 3 is internally calibrated with a sinewave level of -67 dBm, the internal pulse generator must supply pulses that are smaller than the specified CISPR pulses by 20 dB.

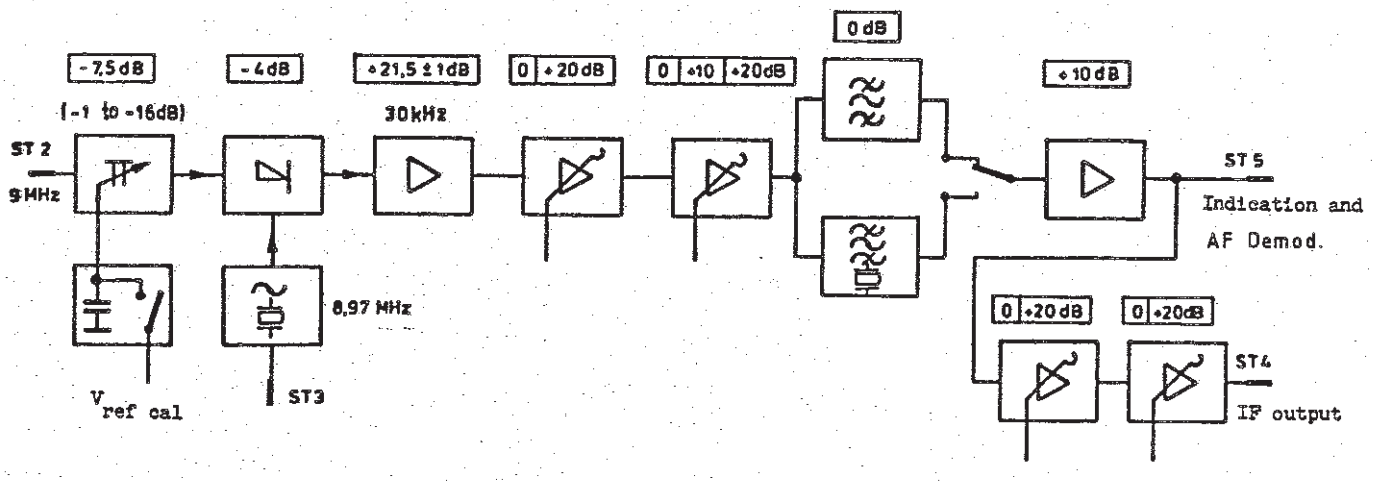
The frequency response of the pulse generator at the upper frequency range limit can be varied by means of C90 for a flatter indication.

4.1.9 3rd Mixer (Y11)

(See circuit diagram 303.6219 S)

The 3rd mixer performs the following tasks:

- Corrects the gain over entire signal path between the RF input and the display during level calibration (PIN-diode attenuator with store IC B1).
- Converts 9.0 MHz to 30 kHz using a built-in 8.97-MHz oscillator (phase-locked loop with 500-Hz reference).
- Adjusts the IF attenuation in steps, 0 to +40 dB, by means of B10, B15.
- Filters out the noise before the indication and AF demodulation to preserve the overall noise figure at 500-Hz and 2.4-kHz IF bandwidth.
- Switches over to 200 Hz IF bandwidth by means of the mechanical filter B18. Indicates any overload of the stages preceding the 200-Hz filter.
- Switches the IF gain over before the IF output.



IF attenuation

"0db":	+20dB	+20dB
"+10dB":	+20dB	+10dB
"+20dB":	+20dB	0dB
"+30dB":	0dB	+10dB
"+40dB":	0dB	0dB

Log 60:	0dB	0dB
Log 40:	20dB	0dB
Lin :	20dB	20dB
CISPR1:	20dB	0dB
CISPR3:	20dB	0dB

Fig. 4-4 Block diagram of the 3rd mixer

The 8.97-MHz oscillator consists of a crystal oscillator which is trimmed by means of a phase-locked loop. The IF attenuation is selected by switching the feedback which sets the gain of two operational amplifiers.
Two stagger-tuned active resonant circuits (B16-B21) filter out the noise.

4.1.10 Indication and AF Demodulation (Y12)

(See circuit diagram 303.6919 S)

The Indication and AF Demodulation board obtains the 30-kHz IF signal from the 3rd mixer, from which it produces signals for the level indication) as well as AF voltages (e.g. for the AF amplifier) by means of various demodulators.

In Fig. 4-5, a simplified block diagram is shown. The signal path for the indication demodulation is completely separate from the signal path for the AF demodulation.

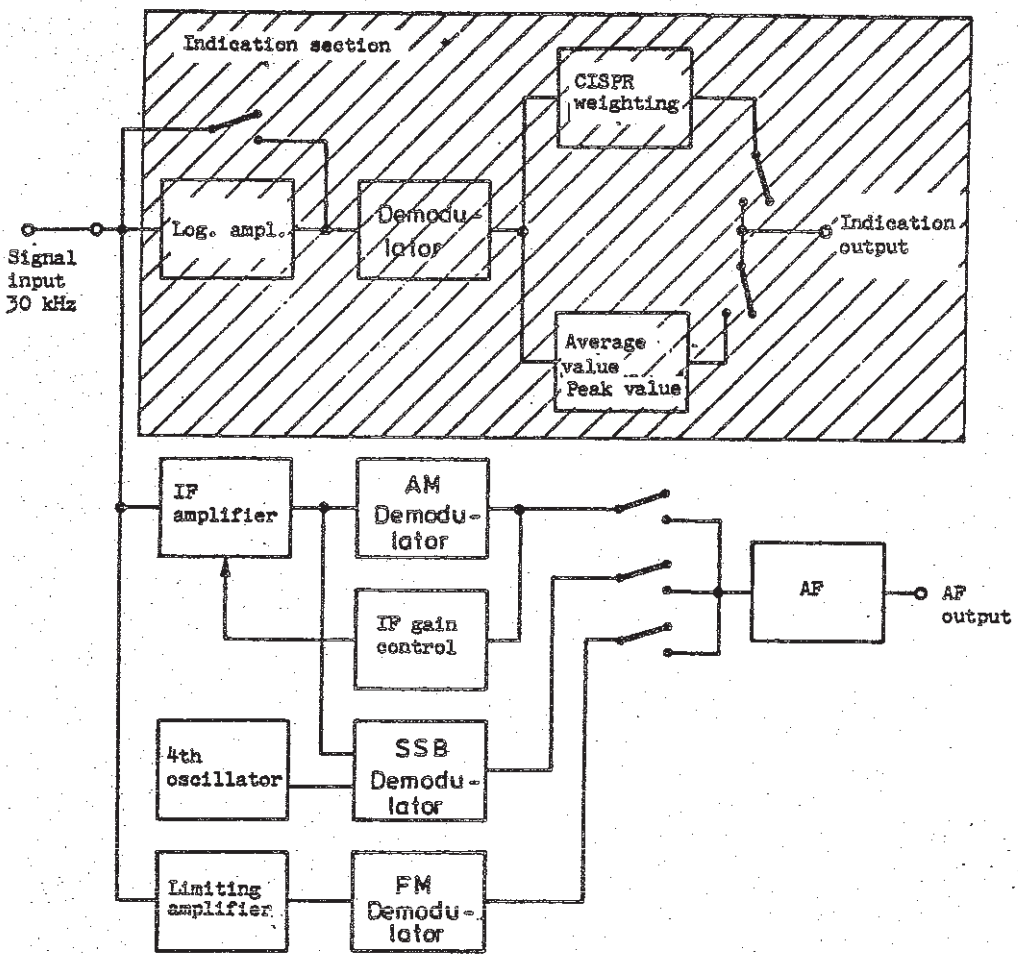


Fig. 4-5 Block diagram of indication and AF demodulation

The indication section demodulates the input signal and produces a DC voltage for level measurement. Moreover, signal weighting according to CISPR or peak value indication is possible.

To achieve a wider indicating range than 20 dB with linear demodulation, a logarithmic converter for the instantaneous value can be connected before the demodulator. In this way, the 40-dB and the 60-dB ranges are obtained.

The AF demodulation section permits reception of AM and FM as well as SSB and telegraphy signals.

The FM demodulator consists of a limiting amplifier which is followed by a PLL demodulator. It is separate from the circuit for the other demodulation modes.

The latter contains an automatic gain controlled IF amplifier. This control circuit keeps the AF voltage nearly constant even in the case of large level differences and permits easy aural monitoring of the input signal. In AM operation, the AF voltage is derived from the IF signal by means of an active rectifier which supplies at the same time the input voltage for the control amplifier.

With telegraphy and SSB demodulation, the amplified IF signal is taken to a product detector. The mixer signal is supplied by the 4th oscillator which is also included on the board. The control circuit is switched over with telegraphy and SSB demodulation and the rise and fall times are adapted to the demodulation mode selected.

Because of limiting in the FM mode and level control in the other demodulation modes, the input level cannot be determined from the volume of the AF signal. This is only possible by separate indication demodulation. The detailed block diagram of this subassembly is shown in Fig. 4-6.

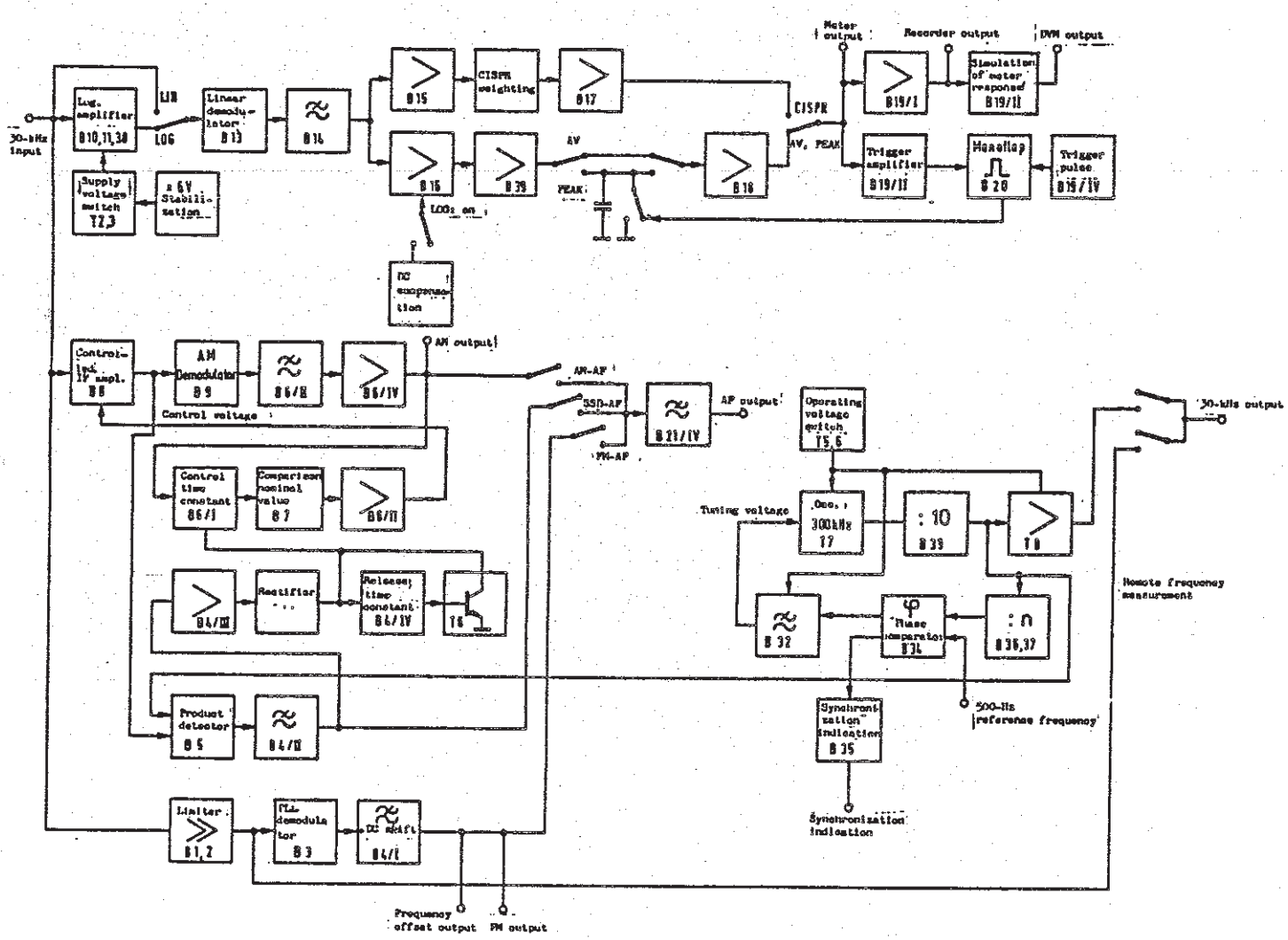


Fig. 4-6 Block diagram of indication and AF demodulation

4.1.10.1 IC Switches

For the numerous switching functions, IC analog switches are used. They are entered in the circuit diagram as normal switches with the designations S1, S2, etc. For the sake of clarity, the control circuit is drawn separately from the switches.

Depending on the requirements, two different types of IC switches are used: CD 4016 and IH 5027. An essential difference between the two types is that the CD 4016 switches on with a positive (+10 V) and the IH 5027 with a negative (-6 V) control voltage. Unlike the CD 4016, the IH 5027 does not require a supply voltage.

Table 4-3 contains a summary of the control inputs to the board. They are driven with TTL signals. The particular function is switched on if the level is at high.

The comparators B22-23-24-25 convert the TTL signals to the above mentioned levels of +10 V and -6 V required for driving the IC switches. The comparison voltage is produced by means of R239, GL67 and GL68 and amounts to 1.4 V.

OR gates formed by diodes gate the control signals. For example, S9 is to switch on with PEAK1 or PEAK3 (SP1 v SP3). The signals are gated by means of GL63-GL64-R264. The output of the OR gate is connected to the inverting input of the comparator B24/II. Since it is an IH 5027 type switch, S9 requires a negative output voltage from the comparator to switch on.

Table 4-3: Control inputs

For the indication demodulation:		
CISPR 1	Signal weighting in the indication path according to CISPR Publ. 1	
CISPR 3	Signal weighting in the indication path according to CISPR Publ. 3	
PEAK1	Peak-value measurement with 1 s hold time	With the ESH 3, only control input PEAK3 is used for switching on peak-value indication.
PEAK3	Peak-value measurement with 3 s hold time	
LOG 40	Logarithmic indication, 40-dB range, corresponding to 40-dB operating range	
LOG 60	Logarithmic indication, 60-dB range, corresponding to 60-dB operating range	

For the AF demodulation	
AM	AM demodulation
FM	FM demodulation
A0	Demodulation of telegraphy, for adjustment to zero beat
A1	Demodulation of telegraphy
USB	Demodulation of AM SSB signals, upper sideband
LSB	Demodulation of AM SSB signals, lower sideband
Other:	
RFM	Remote frequency measurement
30 kHz ON 4th oscillator at 30.0 kHz	

Table 4-4 contains a summary of all the IC switches and their respective control inputs.

Table 4-4 IC switches and switch control

Switch	No.	Type	Triggered in mode	Triggered by
S1	B31/I	IH 5027	$\overline{\text{LOG 40 v LOG 60}}$ (= LIN)	B25/II
S2	B31/II	IH 5027	LOG 40	B25/I
S3	B31/III	IH 5027	LOG 60	B25/III
S4	B27/I	CD 4016	LOG 40 v LOG 60	B25/II
S5	B29/IV	IH 5027	LOG 40	B25/I
S6	B31/IV	IH 5027	$\overline{\text{LOG 60}}$	B25/III
S7	B29/III	IH 5027	$\overline{\text{PEAK1 v PEAK3}}$ (= AV)	B24/III
S8	B29/II	IH 5027	Triggered in mode PEAK by B20	
S9	B29/I	IH 5027	PEAK1 v PEAK3	B24/II
S10	B28/I	IH 5027	CISPR 1	B23/IV
S11	B28/II	IH 5027	CISPR 1	B23/IV
S12	B28/III	IH 5027	CISPR 1 v CISPR 3	B23/II
S13	B28/IV	IH 5027	$\overline{\text{CISPR 1 v CISPR 3}}$	B23/III
S14	B30/II	CD 4016	PEAK3	B24/I
S15	B30/III	CD 4016	$\overline{\text{A1 v USB v LSB}}$ = (AM v FM v A0)	B23/I
S16	B30/I	CD 4016	$\overline{\text{CISPR 1 v CISPR 3}}$	B23/II
S17	B27/III	CD 4016	$\overline{\text{A1 v USB v LSB}}$ = (AM v FM v A0)	B23/II
S18	B28/IV	CD 4016	A1 v USB v LSB	B25/IV
S19	B26/III	CD 4016	A1	B22/II
S20	B26/II	CD 4016	FM	B22/III
S21	B26/I	CD 4016	A0 v A1 v USB v LSB	B22/I
S22	B27/II	CD 4016	AM	B22/IV
S23	B26/IV	CD 4016	A1 v USB v LSB	B25/IV

4.1.10.2 Indication Section

In the indication section, the 30-kHz IF signal applied to ST2 is processed. The following levels are permissible at ST2 for the various measurement ranges:

LIN	2 to 20 mV (rms)	corresponding to 20-dB operating range with the ESH 3
LOG 40 dB	2 to 200 mV	corresponding to 40-dB operating range
LOG 60 dB	2 to 2000 mV	corresponding to 60-dB operating range

4.1.10.2.1 Logarithmic Amplifier

A logarithmic amplifier consisting of B38 is connected before the indication demodulation. It is triggered only in the LOG 40 or LOG 60 mode. In the LIN mode, it is bypassed by S1.

The supply voltages +6 V and -6 V are produced and stabilized by T1 and T4. S4 makes contact only in the LOG 40 or LOG 60 mode causing T2 and T3 to conduct which in turn connect the supply voltages through to the logarithmic converter. In the LIN mode, T2 and T3 are cut off to save current.

The signal present at ST2 is either applied directly to the inputs A1, A2, B1, B2 or after attenuation by 30 dB or amplification by 30 or 60 dB (see Fig. 4-7). The 30-dB amplifier stages consist of the operational amplifiers B10 and B11.

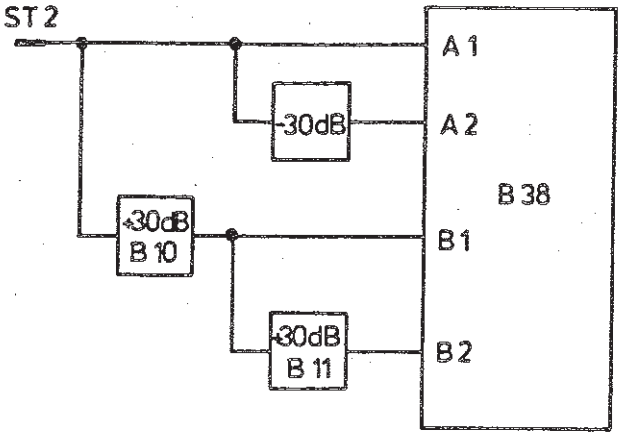


Fig. 4-7 Driving circuit of B38

R128, R123, R126 permit exact setting of the attenuation and gain, respectively of the 30-dB attenuators or amplifiers. In this manner, the logarithmic characteristic can be adjusted.

The diodes GL23 to 28 reduce the supply voltage of B10 and B11 to +4 V thus limiting the voltage at the inputs B1 and B2 of B38.

The differential amplifier B12 combines the currents at the outputs of B38. The NTC resistors R145 and R146 serve for temperature compensation of the complete logarithmic amplifier. The attenuators are connected to the output of B12 according to the measurement range selected: R138-R139-R140 in the LOG 40 mode and R137-R141-R142 in the LOG 60 mode.

4.1.10.2.2 Indication Demodulation

The signal path is the same in the operating modes LOG 40, LOG 60 and LIN (corresponding to 40-dB, 60-dB and 20-dB operating ranges) after the switches S1, S2, S3. B13 functions as an active demodulator consisting of the diodes GL85 I and II. Then the signal is taken to the balanced active filter B14 whose cutoff frequency is 10 kHz.

With an input signal of 2 mV_{rms} present at ST2 in switch position LIN, the output voltage at B14 is approximately 20 mV.

Offset compensation control R164 is used for adjusting maximum gain linearity of B14 so that the output voltage at 20 mV input voltage is exactly 10 times that at 2 mV.

After B14, the signal paths split up depending on whether CISPR or average-value (AV) or peak-value (PEAK and MIL) indication has been selected.

4.1.10.2.2.1 CISPR Meter Amplifier

B15 and B17 are the active components of the meter amplifier section which is used only with CISPR weighting. B15 is a peak rectifier. Offset compensation control R174 permits it too to be adjusted for maximum gain linearity.

It drives the RC network R190-R192-C82 whose charging time constant of 45 ms and discharging time constant of 500 ms comply with the provisions of the CISPR Publication 3. GL86 prevents the capacitor from discharging via B15.

The CISPR Publication 1 specifies a charging time constant of 1 ms and a discharging time constant of 160 ms. For this reason, the resistors R192 and R193 are added for CISPR 1.

B17 amplifies the input voltage by a factor of 10. R195 permits exact zero setting. R198 enables exact setting of the gain.

4.1.10.2.2.2 Meter Amplifier for Average- and Peak-value Indication

B16 amplifies the input signal by a factor of 10. Zero setting is accomplished with R177. R182 serves for gain adjustment. The voltages produced by means of the adjustable dividers R179, R185, R186 and R172, R187, R188 are taken via R181 to the inverting input of B16 in the operating modes LOG 40 and LOG 60. As a result, the output voltage of B16 is reduced in the LOG 40 and LOG 60 modes to ensure the same voltage range at the meter output in the LIN, LOG 40 and LOG 60 modes.

The gain of the following operational amplifier B39 is unity. GL81 prevents C97 from discharging via B39 in peak-value measurements. When measuring the peak value, S9 is closed. C97 is the storage capacitor for the peak value. In the PEAK 1s mode, C97 is discharged every second and in the PEAK 3 mode, every three seconds by means of S8.

When measuring the average value S9 disconnects C97 and in its place R189 is switched on by means of S7, which prevents charging of the non-inverting input of B18. The average value is calculated in the microcomputer.

Switch S8 discharges the peak-value storage capacitor C97. This switch is controlled via input SP50 directly by the allocated port on the Computer Board, depending on the selected measuring time. A discharge takes place whenever the measuring time ends. As a result, B20 has no function in the ESH 3.

4.1.10.2.3 Indication Outputs

4.1.10.2.3.1 Meter Output (ST1/a2)

S12 or S13 connects either the CISPR meter amplifier or the meter amplifier for average- and peak-value indication to the output ST1/a2. When making average-value and peak-value measurements, the voltage range is 0.2 to 2 V with an input signal of

2 mV to 20 mV in the LIN mode	(20-dB operating range)
2 mV to 200 mV in the LOG 40 mode	(40-dB operating range)
2 mV to 2 V in the LOG 60 mode	(60-dB operating range)

at ST2.

No logarithmic measurement is possible with CISPR weighting.

4.1.10.2.3.2 Recorder Output (ST1/a6)

B19/I produces the recorder output level

0.5 V to 5 V in the AV or PEAK indicating mode
0.2 V to 2 V with CISPR weighting

from the signal at the output ST1/a2.
The output impedance is 10 kΩ.

4.1.10.3 AF Demodulation

The AF demodulation section supplies the signals for the AF amplifier and the various demodulator outputs. It contains an AM and an FM demodulator as well as a demodulator for SSB and telegraphy signals.

4.1.10.3.1 FM Demodulation

B1 and B2 boost a weak input signal by about 80 dB. Stronger signals are limited by means of GL3, GL4 as well as by GL1, GL2. The input 14 of B3 is thus driven with squarewave pulses.

A PLL circuit based on B3 demodulates the FM signals. The voltage-controlled oscillator (VCO) contained in B3 is synchronized in phase with the input signal by means of the phase comparator that is also in B3. The demodulated AF signal is the control voltage of the oscillator if a frequency-modulated signal is fed in. Fig. 4-8 shows the block diagram.

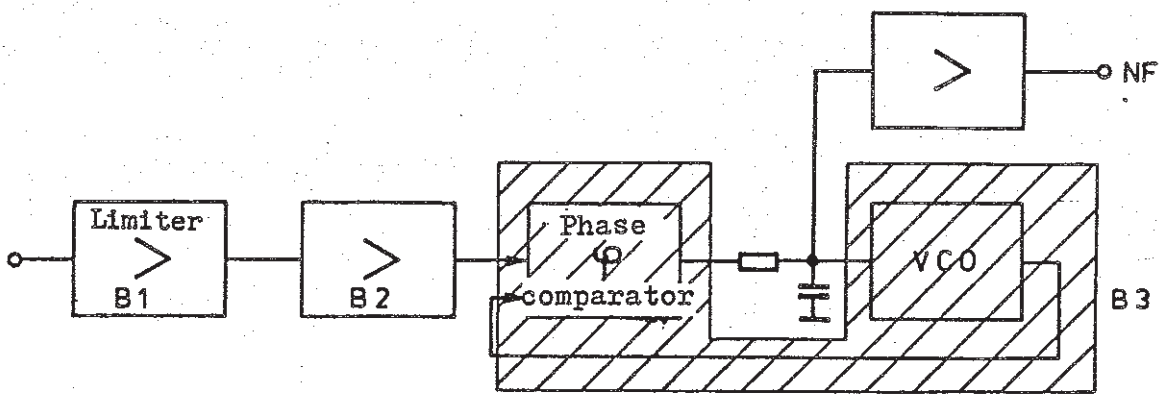


Fig. 4-8 Block diagram of the FM demodulation

C7 and the resistors at pins 11 and 12 of B3 determine the oscillator frequency. The oscillator is adjusted to the centre frequency of 30 kHz by means of R19. R17 serves for temperature compensation.

After amplification and limiting in B1 and B2, the input signal is available at input 14 of the phase comparator. The signal from pin 4 of the internal oscillator is available at input 3. The output voltage of the phase comparator at pin 2 passes through a low-pass filter to the tuning input of the oscillator.

This is also where the AF voltage is derived which is boosted by B4/II so that the voltage at its output corresponds exactly to 1 V per kHz offset from 30 kHz. It is available at the frequency offset output.

The demodulated signal is also available at the FM output ST3. On account of the voltage divider R30, R49, the voltage is here 0.1 V per kHz offset, and the source impedance 10 kΩ.

The AF voltage passes then via the voltage divider R28, R29 and the switch S20 to the AF filter comprising B21/IV. The cutoff frequency of the filter is 8 kHz. Its gain is unity. It supplies about 200 mV_{rms} to the AF output (ST1/a3) at 5 kHz deviation.

4.1.10.3.2 AM, SSB and Telegraphy Demodulation

The same AGC-controlled IF amplifier B8 (TCA 440) is used for AM, A0, A1, USB and LSB. A simplified block diagram of B8 is shown in Fig. 4-9.

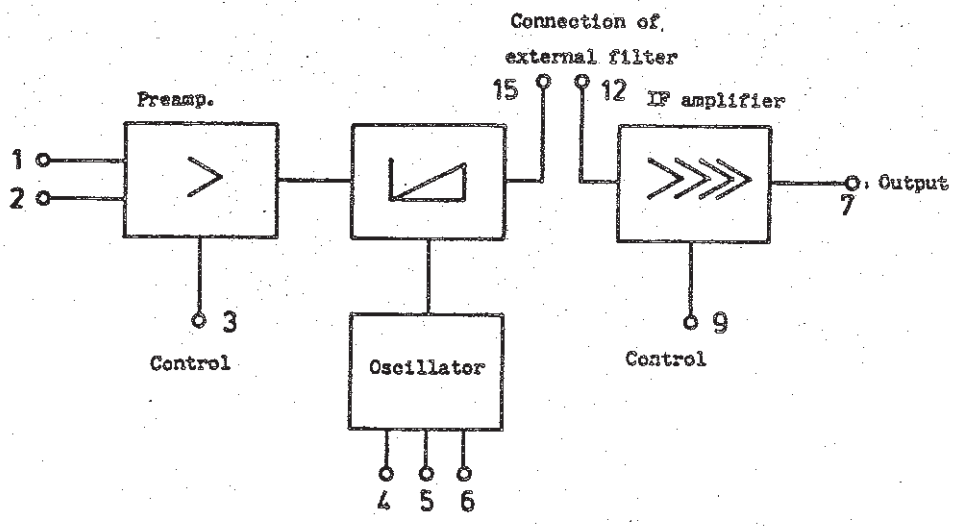


Fig. 4-9 Simplified block diagram of the B8 (TCA 440)

The internal oscillator is disabled by the connections to pins 4, 5, 6. The preamp and the IF stages operate at 30 kHz. The gain is controlled by the voltage at pins 3 and 9. A positive control voltage decreases the gain. The automatic gain control keeps the output signal at pin 7 at about 20 mV_{pp} (see sections 4.1.10.3.2.1 and 4.1.10.3.2.2).

4.1.10.3.2.1 AM Demodulation

B8 is followed by an active demodulator using B9 for AM demodulation. Then the signal is taken to the differential amplifier B6/II with a gain of 27 and an upper cutoff frequency of 10 kHz. The voltage follower B6/IV drives the AM output ST4. 1 V_{pp} at the AM output corresponds to a modulation depth of 100%. The source impedance is 10 kΩ. Fig. 4-10 shows the voltage at the AM output at various modulation depths.

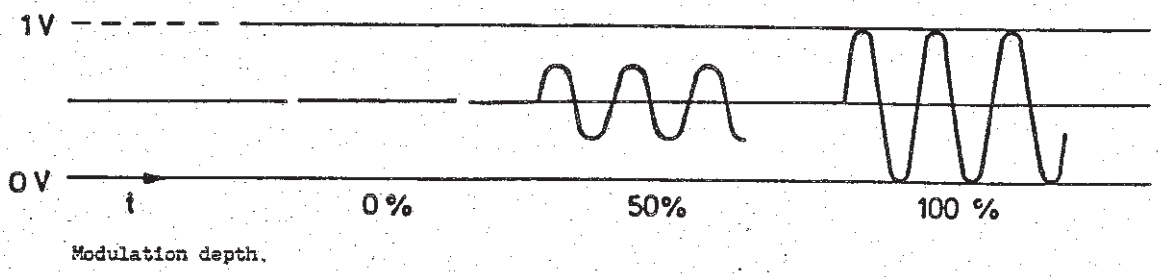


Fig. 4-10 AM output

Control with AM

The demodulated signal is further processed to obtain the control voltage. The switches S17 and S15 after the voltage follower B6/I are closed in AM demodulation. The low-pass filter R61-R64-C22 filters out the AF superimposed on the DC voltage and sets the AM control time constant of 0.5 s.

The voltage divider comprising GL20 and R67 produces the nominal control value at the inverting input of B7. B7 compares the nominal value with the actual value at the non-inverting input. B6/II boosts its output voltage for the control of B8. The voltage dividers match the levels to the two control inputs B8/3 and B8/9.

Control with AM

To generate the AM control voltage the demodulated signal is buffered by B6/IV and then transferred to the RC lowpass R61-R64-C22 via S17. This lowpass suppresses the alternating voltage component of the AF signal (time constant 0.5 s). To render interfering pulses more audible GL94 and R78 are connected in parallel to the charging resistor R61 via the switch B40. The quasi-peak value of the AF signal is used for control, so that the volume of noise is reduced. Furthermore, instead of the AF lowpass B21 the diode GL98 is cut into the AF path via the switch B41. Thus weak pulses are accentuated to such an extent that they can easily be distinguished from the noise. However, sinewave signals are distorted. If necessary, the position of link ST7 can be changed in such a way (connect 2 and 3) that the quasi-peak value is no longer the basis of control.

The control voltage is generated at the subsequent amplifier B7 by comparison of the AF centre frequency to the nominal value (voltage at GL 20). B6/III amplifies the control voltage, and the subsequent voltage dividers match it to the control inputs of the AM component B8.

4.1.10.3.2.2 Demodulation of A0, A1, USB, LSB

For the demodulation of telegraphy and SSB transmissions, a carrier produced by the 4th oscillator must be added to the IF signal (see 4.1.10.4). The output signal of the IF amplifier B8 is applied to the ring modulator B5 (pin 1) where it is mixed with the signal of the 4th oscillator which is available at pin 10.

The balanced output signal available at pins 6 and 12 is applied to the active low-pass filter B4/I (f_{cutoff} = 3 kHz). The filtered AF voltage is taken to B21/IV via S21 (see 4.1.10.3.1).

Control with A1, USB, LSB

Another difference between the demodulation of A1, USB and LSB signals and the AM demodulation is in the control of B8. With telegraphy and SSB transmissions, the signal level fluctuates heavily since the carrier is not constantly present. Hence, it is desirable that the control of the IF amplifier reacts very fast in the case of a signal increase. The fall time of the control should be longer to prevent the noise during voice transmission and keying intervals from being amplified.

The control circuitry for A1, USB and LSB has been designed with this in mind. With A0, the IF amplifier is controlled as with AM.

S18 and S23 close when A1, USB or LSB is switched on. The RC section R62-C23 determines the rise time of the control and the fall time is determined by the network B4/III-B4/IV-T6. B4/III boosts the AF signal and adds a positive DC voltage. GL8 clips the negative half-waves. In the case of slow signal changes, C23 discharges via GL6 and R54 during the negative half-wave.

The rectified AF signal is smoothed by C21. B4/IV boosts the DC voltage obtained and cuts off T6. If the signal changes suddenly by more than 20 dB, for example, during a keying interval with A1, the AF is no longer present at B4/III and C23 cannot discharge via GL6. The control voltage remains unchanged.

Only after R56 has discharged the storage capacitor C21 to below the threshold fixed by R58 and R73 does T6 conduct discharging C23. With A1, S19 switches R57 into circuit shortening the release time constant.

To avoid short pulses affecting the control voltage, a second RC section R63-R66-C23 with a short rise and fall time has been provided.

Fig. 4-11 shows the IF control with a morse code character ("n"). When the carrier is keyed, the control voltage rapidly reaches the required value. During the keying interval between dash and dot, the control voltage remains unchanged. After the dot, it "waits" for further signals to follow and will then again drop very fast.

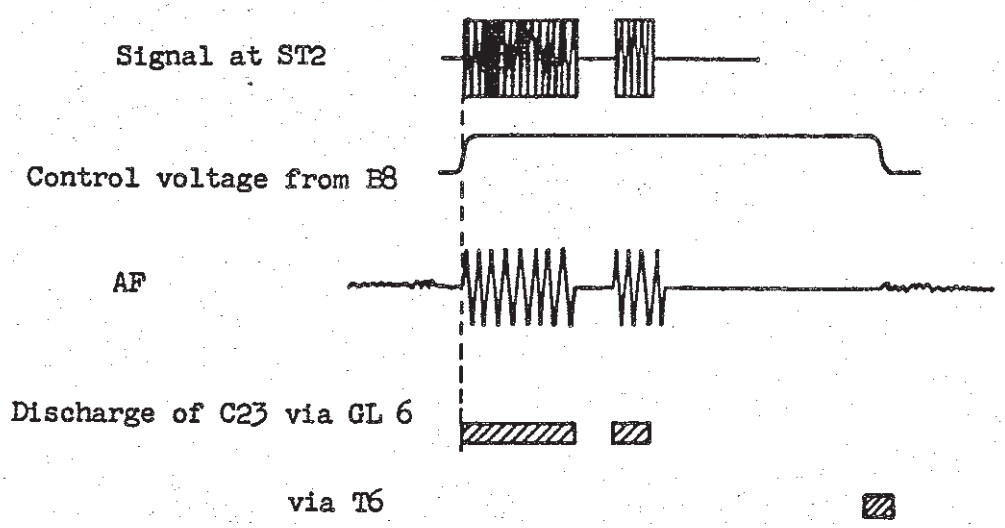


Fig. 4-11 Time function of the control voltage with a morse code character

4.1.10.4 4th Oscillator

The 4th oscillator produces the heterodyne frequency for the product detector with A0, A1, USB and LSB (see 4.1.10.3.2.2) and with 30 kHz ON, it supplies a signal to the 30-kHz output (see 4.1.10.4.5).

The frequencies of the 4th oscillator are as follows:

With	30 kHz ON	30.0 kHz
	A0	30.0 kHz
	A1	31.0 kHz
	USB	31.5 kHz
	LSB	28.5 kHz.

These frequencies are produced by a PLL referenced to a crystal.

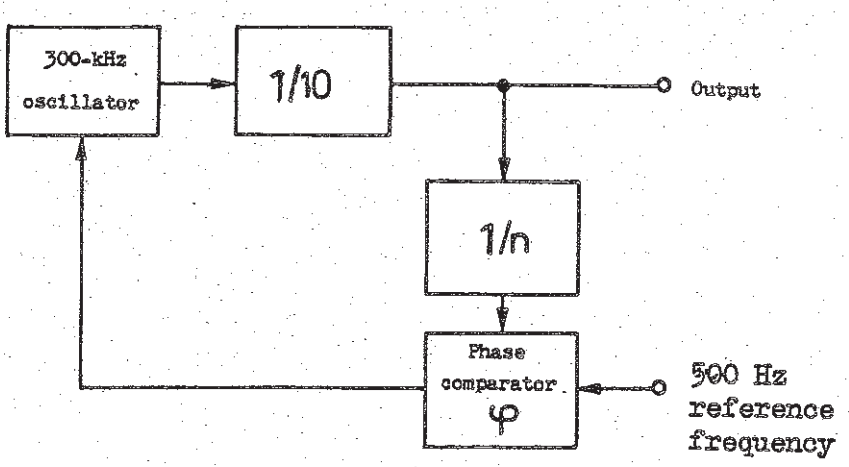


Fig. 4-12 Block diagram of the 4th oscillator

The voltage-controlled oscillator oscillates at approximately 300 kHz. The oscillator output signal is first divided by 10 and then by n, which depends on the desired output frequency. A phase comparator compares the divided signal with the 500-Hz reference frequency and tunes the oscillator to the frequency 10·n·500 Hz.

4.1.10.4.1 Oscillator

T7 is connected up as a 300-kHz Clapp oscillator. It is automatically tuned with GL90. B33 divides by 10 and its output 2 feeds the product detector. Output 14 is taken to the 30-kHz amplifier using T8 (see 4.1.10.4.5) and to the input of the divider B36.

4.1.10.4.2 Adjustable Divider

B36 and B37 form a programmable divide-by-n circuit. n is programmed via the inputs A, B, C, D. According to the formula given above, the division ratios required are 57, 60, 62 and 63. The diodes GL41 to 48 decode the control signals A0, A1, USB, LSB, 30 kHz ON. The logic levels (TTL) at the programming inputs are given in the following table:

Inputs to programmable divider:

	Frequency n kHz		B36 A B C D					B37 A B C D				
A0, 30 kHz ON	30.0	60	L	L	L	L	(=0)	L	H	H	L	(=6)
A1	31.0	62	L	H	L	L	(=2)	L	H	H	L	(=6)
USB	31.5	63	H	H	L	L	(=3)	L	H	H	L	(=6)
LSB	28.5	37	H	H	H	L	(=7)	H	L	H	L	(=5)

Fig. 4-13 shows an example of the timing diagram for an adjustable divider, assuming n = 62.

B36 is BCD-encoded for 2 and B37 is preset to 6. Fig. 4-13 shows the signals at the BCD outputs of the counters. At first they have the preset values. With each positive-going edge of the clock pulse at pin 6 B36 counts down 1. On reaching 0, the "0" output of B36 (pin 12) remains LOW since it is cut off via the CF input (pin 13) which is connected to the "0" output of B37. B36 continues to count down from 0. The positive-going edge at Q4 of B36 switches B37 down by 1.

When B37 finally reaches 0, the "0" output of B37 goes HIGH and the "0" output of B36 is no longer cut off. After B36 has also counted to 0, the "0" output goes HIGH and resets the counter to 62 as it is connected to the Preset Enable inputs (pin 3). The process repeats itself.

To produce a pulse edge at the Preset Enable inputs exactly 62 edges are required at the clock pulse input of B36; i.e. the divider divides by 62 as desired.

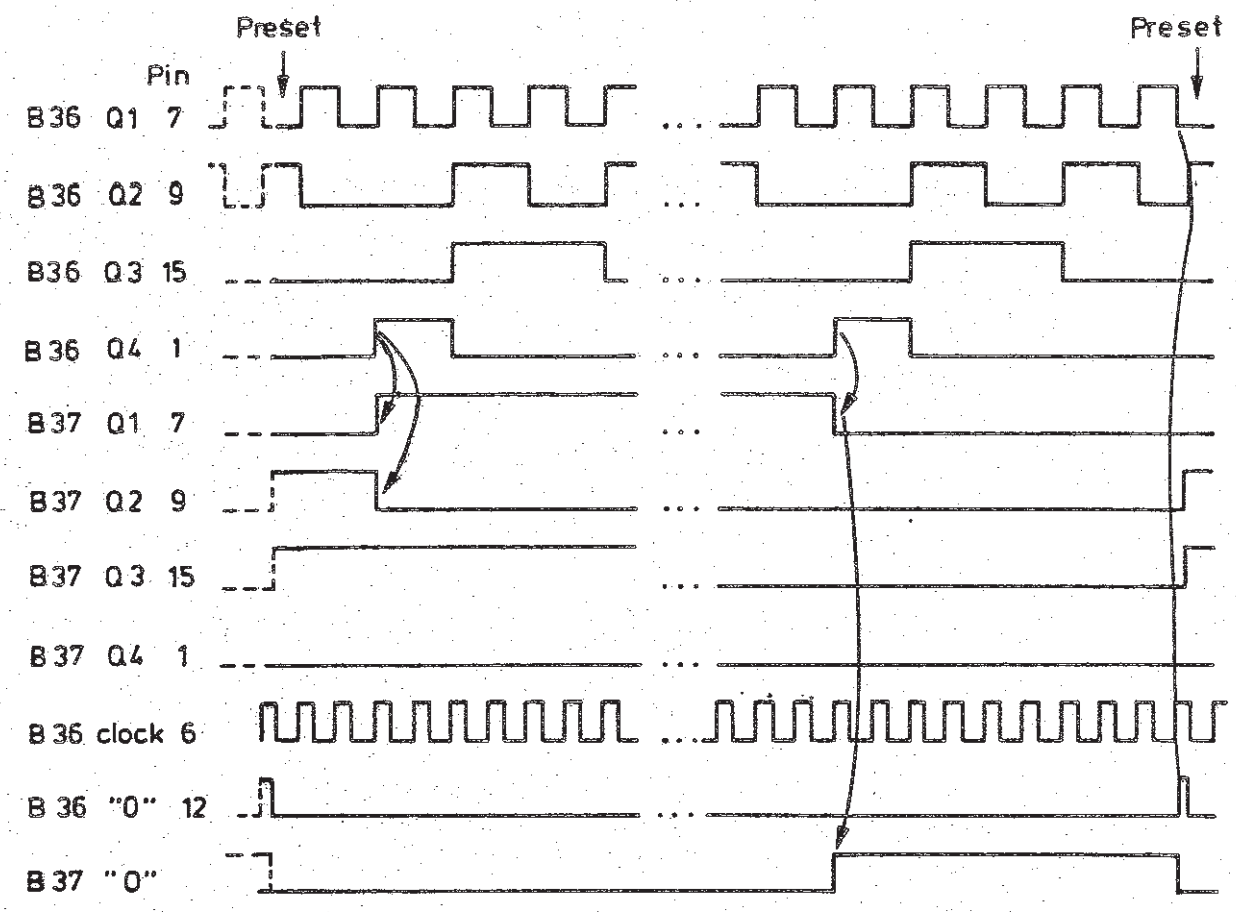
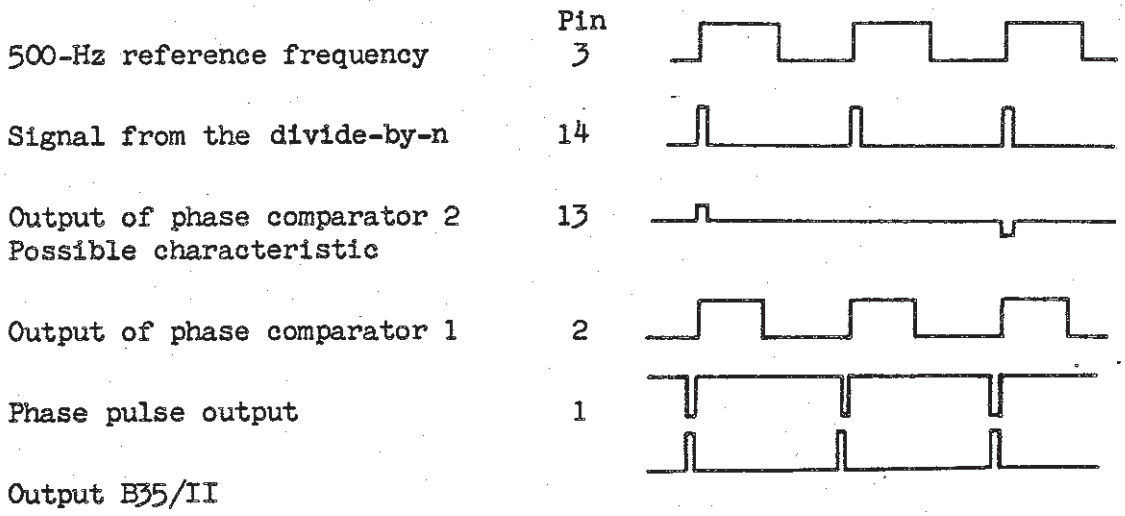


Fig. 4-13 Pulse characteristic with adjustable divider

4.1.10.4.3 Phase Comparator and Synchronization Indication

The phase comparator B34 (MC 14046) compares the divided signal with the 500-Hz reference frequency. The phase comparator 2 used in B34 responds only to pulse edges. Its function is independent of the duty cycle. It synchronizes the oscillator via the active PI (proportional-integral) controller B21.

The phase comparator used produces a phase difference of 0° at the inputs 3 and 14. From the output of the phase comparator 1 (pin 2) and the phase pulse output (pin 1), a signal for synchronization indication is obtained by means of B35/II.



The short peaks at the output of B35/II are smoothed by C121. B35/I functions as an inverter so that, when synchronized, the output of B35/I and, as a result, the Synchronization indication output go HIGH.

4.1.10.4.4 Supply Voltage Switch of the 4th Oscillator

The diodes GL35 to 40 decode the operating modes A0, A1, USB, LSB and 30 kHz ON. If one of them is selected, T6 and T4 connect a supply voltage of +10 V to the 4th oscillator which at all other times is switched off to save power.

4.1.10.4.5 30-kHz Output (ST5)

The 30-kHz output is activated by the controls signals RFM (remote frequency measurement) and 30 kHz ON. The two control signals can never occur at the same time.

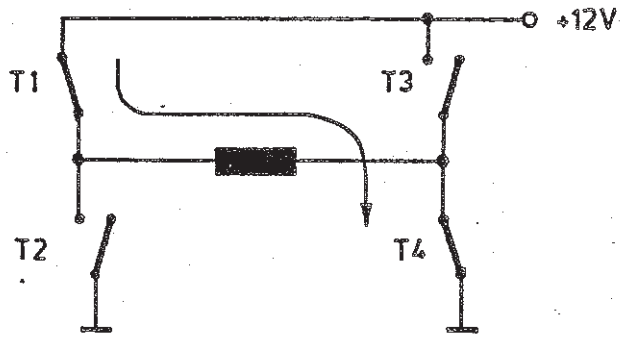
If the RFM input is HIGH, the comparator B21/II causes GL89 to conduct and cuts off GL88. The oscillator signal of the FM demodulator, which is in phase synchronization with the input signal at ST2, is then available at the 30-kHz output (See 4.1.10.3.1).

If RFM is switched to LOW and 30 kHz ON to HIGH, GL88 conducts and GL89 is cut off. The amplifier comprising T8 takes then the 30.0-kHz signal of the 4th oscillator to ST5 (see 4.1.10.4). The level at ST5 is 80 mV_{rms}.

4.1.11 Attenuator Control (Y13)

(See circuit diagram 303.6460 S)

The Attenuator Control design combines high switching speed with minimum power consumption.



Each one of the nine bridge circuits (made up of 4 transistors each) drives one of the solenoids of the RF level switch.

Nine level shifters B14 to B22 match the logic level of the preceding 5-V logic circuit to the 12-V bridge supply.
The logic using the modules B1 to B4 links the attenuation information applied to ST1 in binary code generating the necessary control signals for the level shifters B14 to B21. The monoflops B5 and B6 generate an 18-ms enable signal for the level shifter rendering a switchover of the relays.

The logic levels at the test pins B, C, D, E, F, H, I, K represent the respective nominal switching state of the attenuators. The 4-dB attenuator B22 is normally switched off. Table 5-13 in section 5.3.1.14 shows the relationship between the input levels at ST1.a2, ST1.a2 to 16 and the levels at the test pins. The monostable B5 I (150 ms) which is triggered via differential networks at the control inputs triggers in turn the switching pulse (B6 I = test point G) for switching over the attenuators. Only upon completion of this switching pulse is the new switching state stored in the latches with the clock pulse (B6 II, A).

In automatic operation, the delay is reduced to approximately 1 ms. Monostable B5/II is operative and B5/I is cut off; control line ST1.a3 = HIGH.

Monoflop B7/I ensures that the correct attenuation is connected into circuit at switch-on.

NOTE: When testing the ESH3 with it switched on, the contacts of the Control board must not touch any other potentials since this would immediately overload the unprotected bridge-connected transistors of the Attenuator Control.

4.1.12 Power Supply

(See Circuit Diagram 354.9215 S and Fig. 4-14)

4.1.12.1 Functional Description

The power supply contains the three subassemblies rectifier board, switching power supply and analog power supply, as indicated on the block diagram Fig. 5-1.

The power supply can be operated either with AC line power or with battery power of +24 V with respect to ground. In operation with AC input, a +24-V raw voltage is generated from which the switching and, in part, the analog units produce the required supply voltages for the instrument. An additional supply voltage and two reference voltages are produced for use within the power supply.

4.1.12.2 Rectifier Board

(See Circuit Diagram 355.0011 S)

The power transformer and associated rectifier are mounted directly on the rear panel of the instrument. The 24-V DC output is applied over a short line to charging capacitor C5 on the rectifier board. If the voltage on C5 rises above 40 V, thyristor V10 fires and the AC line is opened. Short noise pulses are limited by V7. The battery voltage is applied via X3, overvoltage being limited by V8 and V9.

The DC output of the power rectifier is passed on for further processing through relay contact k1 when the relay is not energized. The switchover to battery operation occurs only if the AC line voltage is insufficient, a battery voltage of the correct polarity is present, and the instrument is switched on (X4 open).

In case of overvoltage on the +12-V and +5-V supplies, thyristors V3 and V4 shortcircuit these outputs.

The lines into the switching power supply are provided with filters. Furthermore, the analog power supply is connected through 26-pole connector X18 and the loads through two 20-pole connectors X8 and X15. The circuit diagram shows the pin assignment for these connectors from the component side. The board also contains the common neutral X5 of the analog ground lines.

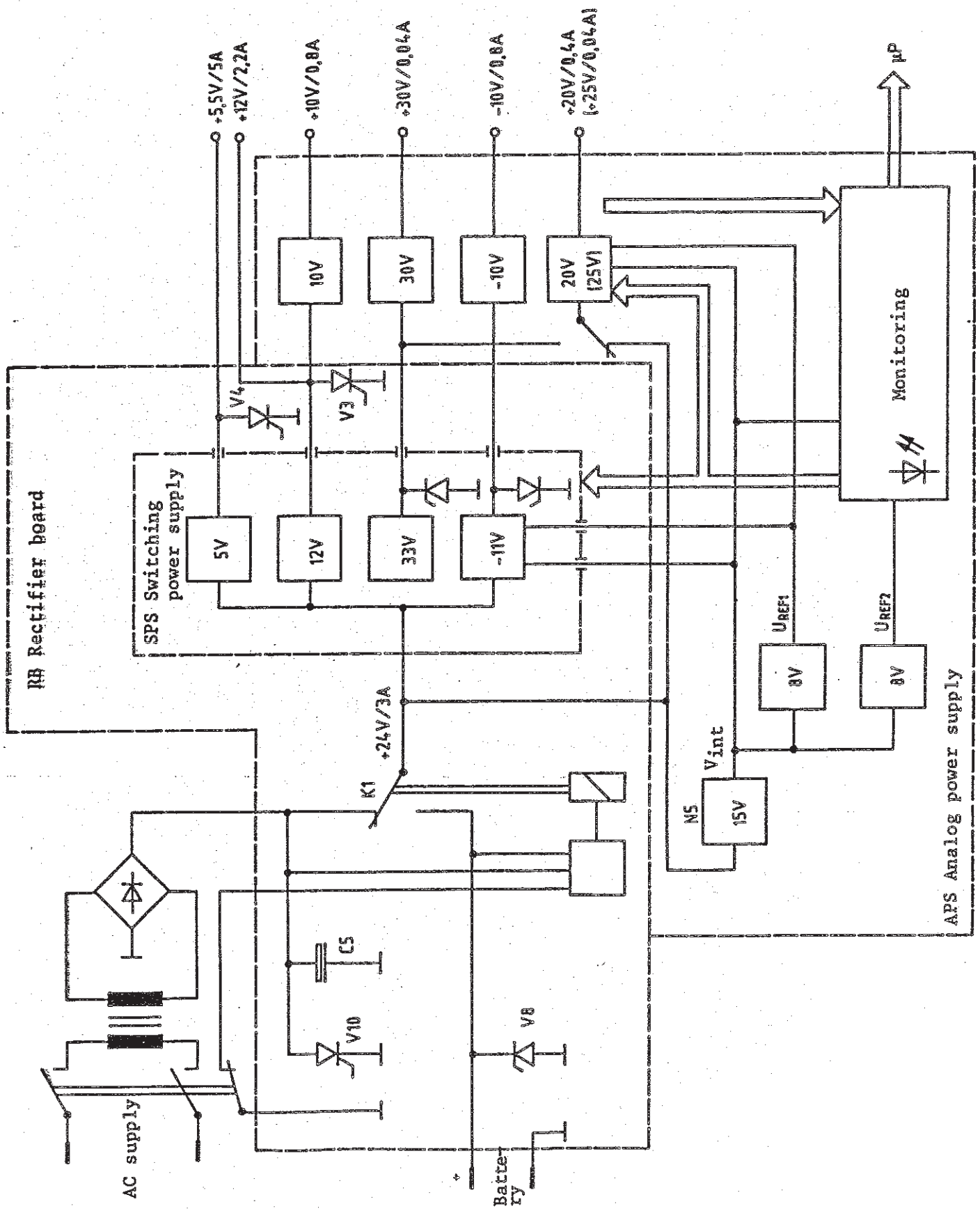


Fig. 4-14 Block diagram of power supply

4.1.12.3 Switching Power Supply

(See Circuit Diagram 354.9515 S)

The switching power supply board is contained in a closed housing to provide RFI shielding. The board generates in three separate switching regulators the output voltages +5 V, +12 and -11 V and +33 V. The regulators operate at a frequency of 200 kHz and are synchronized with each other to prevent beat frequencies.

4.1.12.3.1 Regulators +5 V and +12 V

The +5-V and +12-V circuits are practically the same, so that only the +5-V circuit will be briefly described. It is basically a regulator without transformer.

Transistor V112 is periodically cut in for a fixed time. During this time the current in choke L101 increases slowly from a given initial value. When the transistor is switched off, a slowly decreasing choke current is furnished by the free-running diode V113, so that the voltage across V113 is approximately a rectangular voltage with the amplitude of the input voltage. The duty factor corresponds approximately to the ratio of the output voltage to the input voltage, ignoring losses. A DC current with superimposed ripple flows through L101. Its mean value corresponds to the output current and its AC component is taken up by C118. The output voltage on C118 thus contains only a small ripple. Because of the on-off switching operation, the power loss in the transistor is small. For small duty factors, the loss in the Schottky diode V113 is decisive.

The VMOS transistor V112 requires a positive gate voltage of about 6 V. (A VMOS is used in this position because of the high switching frequency.) The gate voltage is generated by bootstrap circuit C110. When the parallel-connected output transistors of N101 block, V104 conducts and V102 and V112 block. The V112 source voltage is thus slightly negative because of the current voltage of V113, and capacitor C110 is charged via V100 and V101. The maximum voltage is limited by means of V115. In the switch-in phase, transistor V104 is blocked via N101, so that V102 receives base current via R104 and very quickly loads up the V112 gate. When V112 opens, the source potential rises and with it, via C110, the V102 collector voltage.

The pulse width is so regulated by the error amplifier in N101, that the output voltage remains constant. This voltage is furthermore smoothed with an additional LC filter (L102, C120). To assure the stability of the regulation, the varying component of the output voltage is picked off ahead of L102 by C121, whereas the DC component is regulated at the output via R122. The output (pin 9) of the error amplifier is terminated with R109 and C107 for phase compensation. If the potential on this connection drops, the power supply is switched off. This characteristic is used for the switch-on to obtain a soft start-up-capacitor C114 connected via V110 charges up slowly through R112, so that the duty factor increases slowly.

The voltage drop across L102 is used for current limiting. If the drop exceeds the difference input voltage of comparator N100 (set by R114 and R117), C113 discharges and functions similarly to C114 in the start-up circuit.

4.1.12.3.2 Reverse Converter

The third switching regulator functions as a reverse converter in triangle operation and generates the output voltages -11 V and +33 V when power transistor V172 is activated via the push-pull driver V175, V176. The current in the primary winding rises linearly, since no secondary current is flowing. When V172 is switched off, the secondary voltages of transformer V170 are reversed in polarity, so that diodes V173 and V174 become conducting and the output capacitors are charged. During this phase the primary voltage on the V172 drain rises to a value about twice that of the operating voltage. The overshoots, which then occur more frequently, are attenuated by the RCD network on the drain.

Voltage regulation is obtained similarly as for the +5 V and +12 V regulators by means of C185 and R185. The +33-V output is stabilized by the magnetic coupling.

The secondary current limiting is taken from L171 and functions as in the case of the regulators. A current-limiting action is also produced in the primary circuit by means of sensor resistor R177.

4.1.12.4 Analog Power Supply

(See Circuit Diagram 354.9815 S)

The analog power supply furnishes the stabilized +10-V, -10-V, +20/25-V and +30-V supplies as well as the internally used 15-V supply and two 8-V reference voltages. A monitoring circuit generates error signals and the RESET signal for the microprocessor.

4.1.12.4.1 +15-V Supply

This unit containing the integrated regulator N5 generates from the raw 24-V input the 15 V for the circuits of the power supply. The 15-V supply is confined to the power supply and thus is not subject to any external influences.

4.1.12.4.2 +8-V Reference Voltage Sources

Two independent 8-V reference voltages are generated from the +15-V supply with N8 and N9 and temperature-stabilized 6.2-V diodes V30 and V31.
The voltage levels can be adjusted with potentiometers R89 and R95.
Regulator reference V_{REF1} determines the output levels of all analog and switching power supply lines, V_{REF2} is used in monitoring these voltages.
Z-diode V45 prevents any rise in the output voltages in case of a disturbance.

4.1.12.4.3 +10-V/0.8-A Supply

The +10-V supply is obtained from the +12-V output of the switching power supply. Series regulation with collector output permits a slight difference between the input and output voltages. Voltage control is provided by N1III via driver transistor V2. This permits the generation of output voltages higher than the internal supply voltage to the amplifier.

Current limiting with current cutback is provided with sensing resistors R8 and R9 and N1IV, which blocks driver V2 in case of overcurrent. The power supply can also be switched off by an external LOW signal.

To permit use of the +10-V supply as an external voltage reference, the positive sensing lead is separately taken out via X18.16 and is connected to the output lead at the load itself. Resistor R12 prevents an overvoltage in the output in case of a broken sensing line.

4.1.12.4.4 -10-V/0.8-A Supply

This circuit is similar to that of the +10-V supply except for the polarity reversals. The -11-V output of the switching power supply is used as input voltage and for the comparison amplifier. The output of the +10-V supply serves as reference voltage, so that the two voltages are symmetrical. In this case also the sensing lead is taken out separately, via X18.10, to the load. This supply is switched off indirectly via the +10-V supply.

4.1.12.4.5 +20-V/0.4-A (25-V/0.04-A) Supply

This supply is of the same design as the +10-V supply, but, because of the higher output voltage, requires voltage dividers at the input of the current-limiting amplifier N1I. To make this supply usable in other devices, the output voltage and current limiting have been made switch-selectable. In the +20-V setting the supply is driven directly by the raw 24-V voltage, whereas for the +25-V output the +33-V supply of the switching power supply is also used.

4.1.12.4.6 +30-V/0.06-A Supply

In this circuit transistors V16 and V17 form a difference amplifier, V14 is a series transistor and V13 serves for current-limiting. This circuit is supplied from the +33-V output of the switching power supply.

4.1.12.5 Voltage Monitoring

The voltage-monitoring circuit is located on the analog power-supply board. All important supply voltages are constantly monitored in order to inform the user and the microprocessor of any disturbances in operation. Nine LEDs and eight message lines to the microprocessor are provided for this purpose. A green LED is lit to indicate normal status. It is visible from above through the instrument panelling. In case of a failure, the green LED goes out and one or more red LEDs light. If the microprocessor is still functioning, it outputs an error message to the display. Table 5-1 lists the functions of the LEDs (from left to right) and the error codes.

Table 4-4 LED Functions

LED	Designation	Condition signalized	Error code displayed
H2	+24 V	Input undervoltage	-
H1	+15 V	Internal undervoltage	-
H3	+30 V	Voltage outside tolerance limits	ERROR 14
H4	+20/25 V	"	ERROR 13
H5	+12 V	"	ERROR 12
H6	+10 V	"	ERROR 10
H7	-10 V	"	ERROR 11
H8	+5 V	"	-
H9	O.K.		-

4.1.12.5.1 Input Undervoltage

When the raw 24-V supply drops below +21 V, N6II generates a LOW signal, so that red LED H2 lights. A TRAP signal is sent to the microprocessor, via monostable D4I, and initiates a rescue routine. In order to have the +5-V and +12-V supplies available for this routine as long as possible, the -11-V/+33-V switching supply is switched off via output S3 (X18.25) and all analog supplies are switched off via transistor N7III.

Input overvoltages are prevented by circuits on the rectifier board.

4.1.12.5.2 Internal Undervoltage

The internal supply voltage is adequate so long as the input voltage is over 15 V. If the input sinks below this value red LED H1 lights, and the switching power supplies are switched off via S1, S2, S3 and the analog supplies via N7III before their regulators become inoperative.

No message appears on the display, since the required +5-V supply is already switched off.

4.1.12.5.3 Window Comparators

The regulated output voltages, +30 V, +20/25 V, +12 V, +10 V, -10 V, and +5 V, are monitored for over- and undervoltage by means of window comparators (N10, N11, N12). In case of a failure, the green LED H9 goes out and the appropriate red LED H3-H8 lights. The microprocessor receives an ERR INT signal and comparator signal, and generates the corresponding ERROR message for the display. If the 5-V comparator is involved - and only in this case - a RESET is initiated. All supply voltages except the +5-V are shut off in this case.

4.1.12.5.4 Startup and RESET

After the instrument is switched on, RESET is held at LOW via R36 as soon as a very small input voltage is exceeded. All comparators and reference voltages function with the same promptness. With an input voltage over +15 V, the internal supply level is over +13 V, so that S1 goes LOW and the +5-V supply is started up.

As the voltage rises toward its full value, the RESET flip-flop D3 is set via R137 so that RESET remains LOW even when the 5-V comparator switches to HIGH. In this case however N7IV conducts, so that red LED H8 goes out, S2 goes LOW, and the +12-V switching supply makes a soft startup.

When the input voltage has risen to over +22 V, the output of N6II goes high, releasing the third switching supply via S3 and the analog supplies via N7III.

As soon as all voltages lie within their tolerance limits, the D3 output goes LOW and the green LED H9 lights. Monostable D4II is triggered via D3I, and after it resets, the RESET flip-flop is extinguished via C24. The microprocessor is thus activated after a certain delay period during which the voltage for all instrument circuits reach the correct value. Lowpass filter R127, C23 and Schmitt trigger D3II prevent incorrect switching in the transition range of the comparators.

When the 5-V comparator responds, the RESET flip-flop is set via R137 and X14.20 goes low. The power supply thus is restored to its initial state.

4.1.13 Recorder Control

(See circuit diagram 335.9913 S)

This board is used as an interface between the Computer board and the external I/O peripherals.

4.1.13.1 IEC-625 Bus

The IEC-bus socket 1 is connected to the Computer board via ST8. Pin wiring is shown in Fig. 4-14.

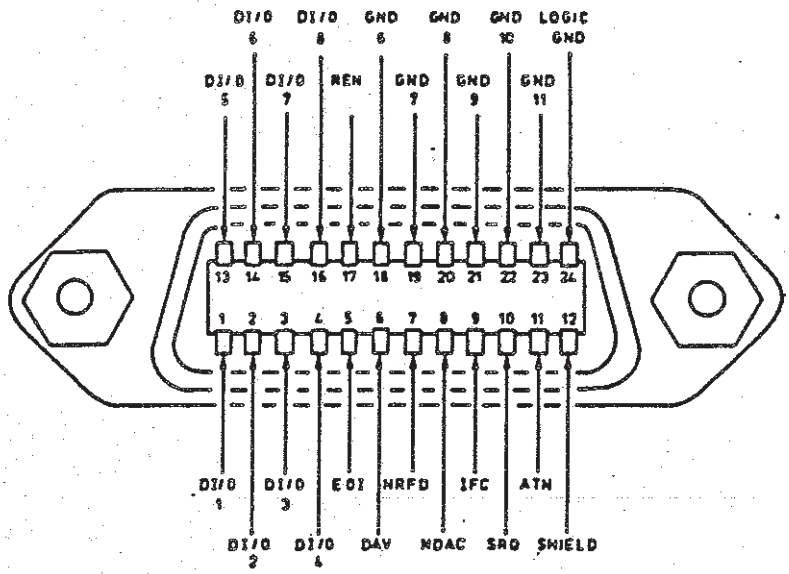
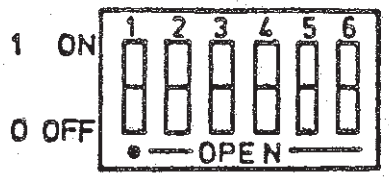


Fig. 4-15 Pin wiring diagram

The IEC-625-bus address can be selected by means of S1 on the rear panel as follows (1-32):

Switch	Value
a1	2^0 = 1
a2	2^1 = 2
a3	2^2 = 4
a4	2^3 = 8
a5	2^4 = 16



The ESH 3 is factory-adjusted to address 17.

4.1.13.2 Recorder Outputs

The recorder outputs can be derived via the 24-way female connector BU2 on the rear panel.

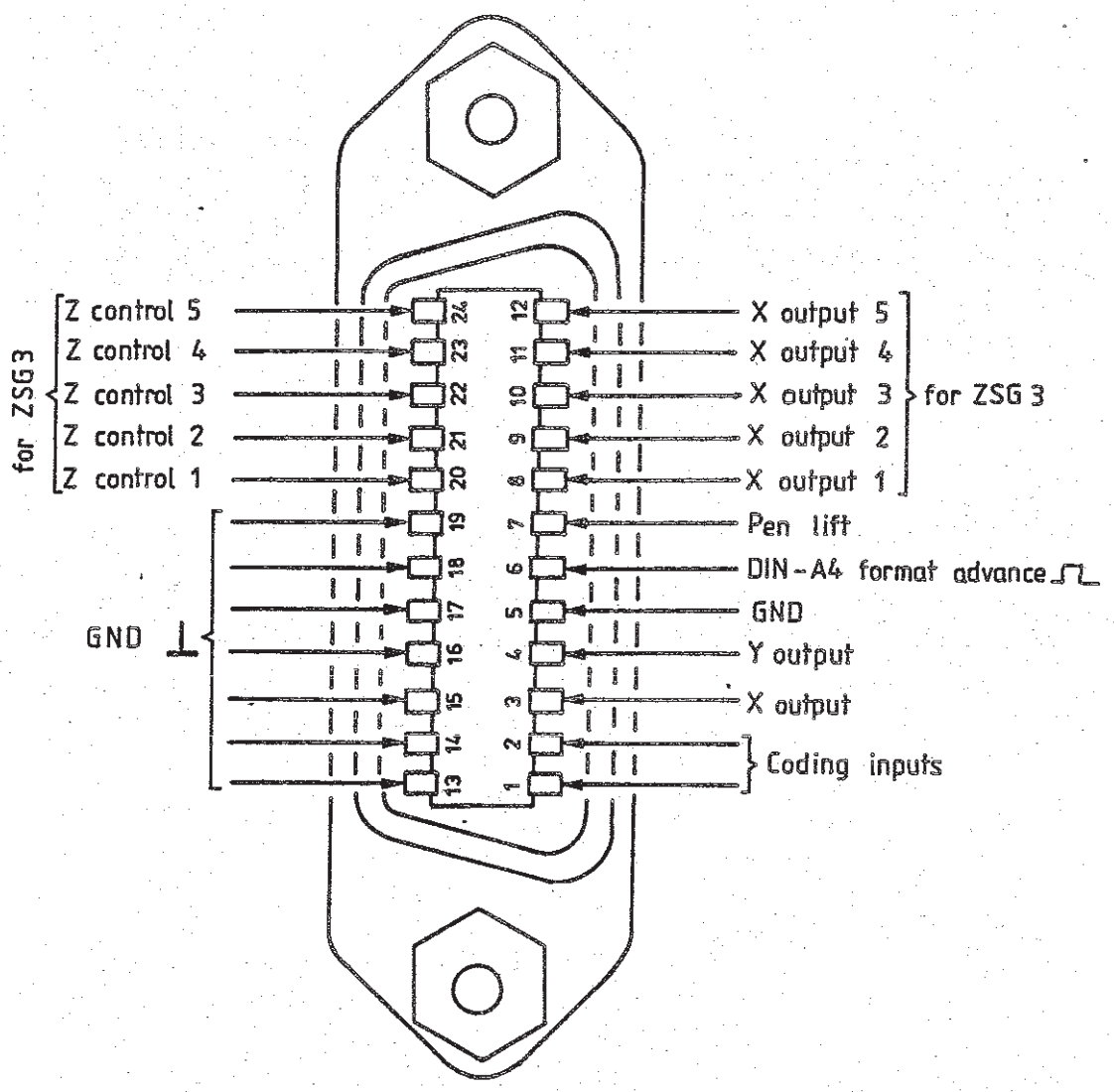


Fig. 4-16 Pin allocation of BU2

The coding lines BU2/pins 1 and 2 supply the information to the µP in the ESH 3 as to whether a recorder and if so, which type of recorder is connected.

Table 4-5 BU2

Pin 1	Pin 2	
N/C	N/C	No recorder connected
To ground	N/C	YT recorder (ZKT)
N/C	To ground	XY recorder (ZSK 2, ZSKT)
To ground	To ground	Radiomonitoring Recorder ZSG 3

The analog X signal is demultiplexed for the Radiomonitoring Recorder ZSG 3 by B1 (which converts from BCD to 1-out-of-5), which controls via level shifter B2, the CMOS switches B3/B4 (+12 V = on). The outputs are converted to low impedance via B5/B6 (I_{max} < 1 mA). B7 controls the pen lift for each channel (HIGH = Pen up).

S2 permits switching over between internal and external reference (5 MHz or 10 MHz).

The recorder control circuit is powered via ST3.

4.1.14 Attenuator (Y16)

(See circuit diagram 302.2813 S)

The Attenuator consists of a base plate on which the attenuator pads are mounted, the drive system comprising the switching contacts and a control board. Ten transmission line sections, eight attenuator pads and an input for the calibration voltage of the ESH 3 are soldered onto the base plate which is made of copper for improved heat dissipation. The transmission lines and attenuator pads are of thin-film design, using a ceramic substrate. The 1- and 4-dB steps are arranged in a T; a π-arrangement is used for the 10- and 20-dB steps and a dual π-arrangement for the 40-dB steps. The contacts of the attenuator pads and transmission lines are gold-plated for enhanced switching reliability and life expectancy. The drive system for switching over the contacts contains 9 rocker switches which are switched over by means of solenoids and kept in the final position by means of permanent magnets. Each of these rocker switches controls three switching contacts, of which one alternately interconnects the transmission lines and the other two switch the associated attenuator pad into circuit. High contact force (0.2 N) ensures reliable contacts.

4.1.15 Motherboard

The Motherboard is used for electrically connecting all the boards plugged in directly or indirectly. The circuit diagram of this board is on 335.8017 S, sheet 1.

4.2 Mechanical Construction

The ESH 3 comes as a 19" unit, 4 dimensional units in height.

To open the receiver, loosen the four Phillips type screws on the two side panels. Remove the top and bottom panels thus gaining access to screening panels which can be unscrewed.

After these panels have been removed, all the boards are freely accessible. The overall AF wiring of the plug-in boards is accomplished via the Motherboard. On account of the stringent RF shielding requirements, RF wiring is accomplished via coaxial Subminax screw-in connectors.

The front panel and the Display Unit (Y1) + Computer board (Y2) form a mechanical unit which can be removed by undoing 4 screws. After unplugging the cables, the front panel unit can be completely dismantled. The RF-shielded boards can be removed in two simple steps:

- Undo the coaxial connections on the underside of the board.
- Press board from below to unplug.

The Attenuator (Y16) is screwed down on the frame and can be removed only after undoing these screws.

Use of plug-in boards throughout and avoidance of solder connections between the individual boards makes for optimum serviceability as all the boards can be dismantled and repaired quickly with a minimum of tools.

4.3 Arrangement of the Boards

(See Fig. 4-16 (top view of receiver) and maintenance instructions on the inside of the shielding of the ESH 3)

Legend for Fig. 4-16

Board	Designation	Ident. No.
Y1	Display Unit	335.8400 S
Y2	Computer Board	335.8800 S
Y3	Analog Circuit	336.0710 S
Y4	Synthesizer 2	303.7850 S
Y5	Synthesizer 1	303.7715 S
Y6	Filter Control	303.7915 S
Y7	Filter 1	303.7015 S
Y8	Filter 2	303.7415 S
Y9	Mixers 1 and 2	303.6019 S
Y10	Calibration Generator	303.6319 S
Y11	Mixer 3	303.6219 S
Y12	Indication and AF Demodulation	303.6919 S
Y13	Attenuator Control	303.6460 S
Y16	Attenuator	303.2813 S
Y20	Power Supply	303.3210 S
Y21	Memory Board	336.0778 S

4.4 Location of Trimming Components

Board	Reference No.	Function
Y1	R1	Zero adjustment of analog frequency offset indication
	R47	Intensity of upper LED array, analog level indication
	R51	Zero adjustment of analog level indication
Y2	R5	A/D converter adjustment: full-scale deflection
	R6	A/D converter: reference voltage
	R12	Sample/hold amplifier offset
Y3	R33	Frequency offset (gain)
	R37	Offset } Logarithmic converter for
	R40	Gain } 20-dB analog indication
	R98	Offset mod. depth and Δf (-)
	R99	Offset mod. depth and Δf (+)
	R111	Frequency correction
Y4	L4	Frequency of 2nd oscillator
	L21, C42	Characteristic of 100-Hz loop
	L68	Frequency of reference oscillator
Y5	L12, C3	Characteristic of 75-to-85-MHz osc.
	L13, C13	Characteristic of 85-to-95-MHz osc.
	L14, C23	Characteristic of 95-to-105-MHz osc.
Y6	R58, R70, R79, R92, R106	Tuning voltage of RF filters 15 and 16
Y7	-	
Y8	L79, L78 C162, C164	Adjustment of tracking of RF filter 16
Y9	R63, C53, C56	Gain and ripple, 500 Hz
	R69, C64, C67	Gain and ripple, 2.4 kHz
	R76	Gain and ripple, 10 kHz

Board	Reference No.	Function
Y10	R84	Level of sinewave generator
	R110	Calibration correction
	C90	Frequency response
	R91	Adjustment of pulse width for f > 150 kHz (CISPR 1)
	R89	Adjustment of pulse width for f < 150 kHz (CISPR 3)
	R77	TC correction for sinewave generator (do not change setting)
Y11	C4	Frequency 3rd oscillator
	R20	Gain 30 kHz
	R102	Gain 200-Hz bandwidth
Y12	R139	Gain of log amplifier with LOG 40 dB
	R142	Gain of log amplifier with LOG 60 dB
	R164	Adjustment of linearity of B14
	R174	Adjustment of linearity of B15
	R177	Zeroing of B16
	R182	Adjustment of gain of B16
	R186	Compensation DC voltage with LOG 40 dB
	R188	Compensation DC voltage with LOG 60 dB
	R195	Zeroing of B17
	R198	Adjustment of gain of B17
	R19	Adjustment of centre frequency of PLL demodulator
Y20	R26	Adjustment of 10.00-V reference voltage