SERVICE INSTRUCTIONS

Synthesizer 2

342.5003.12

Table of Contents

5. Service Instructions for Synthesizer 2

5.1 Circuit Description

(See Fig. 4 and circuit diagram 342.5003 S)

The synthesizer 2 consists of three functional groups:

5.1.1 Reference Frequency Generation

The crystal B1 the temperature of which is internally controlled by a PTC resistor is connected in series with the two FETs V51 and V52 in a Butler circuit. The crystal oscillator can be tuned to its nominal frequency through varicap V50. In normal operation, this is accomplished with the aid of an adjustable DC voltage which is applied externally via X141.a8. In operation with an external reference frequency tuning is accomplished by means of a PLL via switch D27.

The RF oscillation boosted in V53 is applied via the decoupling power divider T4 to the two outputs X145 and X146. A buffer amplifier comprising V54 and V55 supplies a 100-MHz TTL level to D20 and prevents at the same time that the 100-MHz signal is amplitude-modulated with 50 MHz by the 2:1 divider D20. The second J-K flip-flop D20 provides division to 25 MHz. A further low-power Schottky divider produces 2.5 MHz for the 110.7-to-210.699-MHz PLL. D22 divides by 5, so does D23. As a result, a 100-kHz TTL level is present at the phase comparator D26. D24 divides once more by 10 to 10 kHz which is available at the motherboard connector via a filter section.

The external reference frequency can be fed to the synthesizer board 2 via the coaxial socket X144. If an external reference frequency of 5 MHz is applied, pin a7 is enabled causing the external frequency after division in the 10:1 divider D28 to be divided by 5 in D29. The resulting 100 kHz (5 MHz:50) control the integrator N3 via the phase comparator D26. The tuning voltage is applied via the filter section R123 and C130 to the varicap V50 to be controlled.

If an external reference frequency of 10 MHz is applied, pin b7 is enabled. As a result the divider D29 is switched over to 10:1 division ratio by V58. Thus another frequency of 100 kHz (10 MHz:100) is obtained which is required for phase synchronization.

5.1.2 110.7-to-210.699-MHz Oscillator

The 110.7-to-210.699-MHz oscillator functions as an interpolation oscillator over a 100-MHz range in steps of 1 kHz. It determines above all the synchronization time and the noise performance in the vicinity of the carrier for the complete frequency synthesis of the receiver. Essential features of the low-noise oscillator are a high-Q resonant circuit and a mechanically stable construction preventing microphony. The Hartley type oscillator transistor V14 is tuned simultaneously by two tuning voltages. For coarse tuning of the oscillator 2 x 3 tuning diodes are connected in anti-parallel. Fine tuning for synchronization is accomplished via V1. To obtain a satisfactory tuning characteristic of the frequency range of almost one octave, coupling of fine tuning is varied with coarse tuning, i.e. the gain of coarse tuning is increased at high frequencies, hence about the upper range end. The RF is applied via the output coupling coils L30 and L29 to the two buffer amplifiers. V13 the operating point of which is kept constant by means of a control loop comprising V12 supplies an RF power of > +2 dBm to X142. Finally, the RF is applied to the PLL via a further buffer amplifier consisting of V11 and V10.

5.1.3 Phase-lock Loop

The phase-lock loop consists of a 5-decade (n x 10 MHz to n x 1 kHz) parallel-serial converter with conversion from 5-V to 10-V logic. The 20 control lines (= five decades in BCD) are present at the input of the two data multiplexers D1 and D2. The control inputs 10, 11 and 14 are enabled via a diode matrix consisting of V32 to V40 so that the information of the individual frequency decades is available at the four inputs (4, 5, 11, 12) of the inverting level shifter D3 at time intervals of 1.25 kHz (10 kHz:8) in 5-V logic. After conversion to 10-V logic, this information controls D6 (see Fig. 1).

This universal divider module in LSI technique controls the series-connected 10/11:1 dividers D4 and D5 and moreover further divides the divided frequency as programmed to produce the frequency control information and the desired synchronization frequency. The control of the prescalers via the lines SY, FB1 and FB2 with the aid of the auxiliary circuits D7, D8 and D9 is shown in Fig. 2.

The offset between the frequency entered and the frequency of synthesizer 2 is given by the equation:

$$f_{synth2} = f + 110.7 \text{ MHz}.$$

This offset is taken into consideration in the diode matrix V22 to V27 by provision of a subtracter.

Example:

Setting of the five decades: 12.345 MHz
(data A for subtracter)

Offset: 110.700 MHz

Desired frequency: 123.045

Data B = 1 000 000 - 110 700 = 889300

Data B is called up via the inputs D0 to D5. Since the last two digits of B are 0, only D2 to D5 are connected to the B outputs via appropriate diodes.

The fixed programmed internal divider stages of the LSI circuit are controlled by D6 (in active low format via V18 to V21). A noteworthy feature of this control is the production of 1-kHz increments from a reference frequency of 10 kHz (pin 13) (fractional division).

The second LSI circuit D10 supplies the clock frequency of 10 kHz to D6. It divides the incoming reference frequency of 2.5 MHz (TTL) which is converted to +10-V logic level by 250 (N_S divider: 10, N_T divider: 25). Furthermore, D10 contains two phase discriminators:

PC1

The special circuitry of this sample + hold phase discriminator provides the high gain of 3000 V/2π and low crosstalk of the reference frequency.

PC2

This conventional digital phase discriminator supplies positive or negative output pulses depending on the phase relation of its two input signals with a pulse duration corresponding to the phase difference. The integrator N1 converts the output pulses into the control voltage for coarse tuning. The phase discriminator becomes inactive in a sub-range about the centre of its characteristic in which only the PC1 synchronizes the loop.

In addition, D10 contains an auxiliary circuit which sends an out-of-lock signal via pin 4 as soon as the complete control loop is unlocked. After it has been inverted in V28 this signal controls further auxiliary circuits the operating principle of which is as follows:

Operating principle of PLL (see Fig. 3)

The PLL is assumed to be out of lock after frequency switching by changing the BCD code at the control decades:

1. Synchronization indication (pin a10) goes low.
   This considerably increases the limit frequency of the low-pass filter via the timer D14, D11, V41 and V42 by by-passing R25 with V42.

2. The inactive phase discriminator PC2 in the locked state causes a low-impedance current to be applied to the integrator N1 for acceleration of synchronization. The active low-pass filter N2 with a cut-off frequency of approximately 1 kHz changes the direction of coarse tuning of the VCO as required.

3. The locked state is restored. PC2 is disabled and PC1 is exclusively responsible for the control. D14 resets with a delay the low-pass filter to the slow time constant.

4. At frequencies at which the leading decade reaches the value 8 or 9 the gain is switched over by D12 according to the change in the division ratio and the oscillator gain.

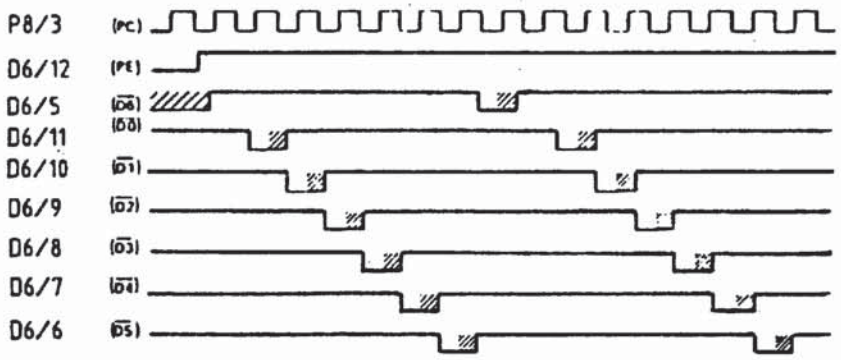


Fig. 1 Control of the data multiplexers D1, D2 by D6

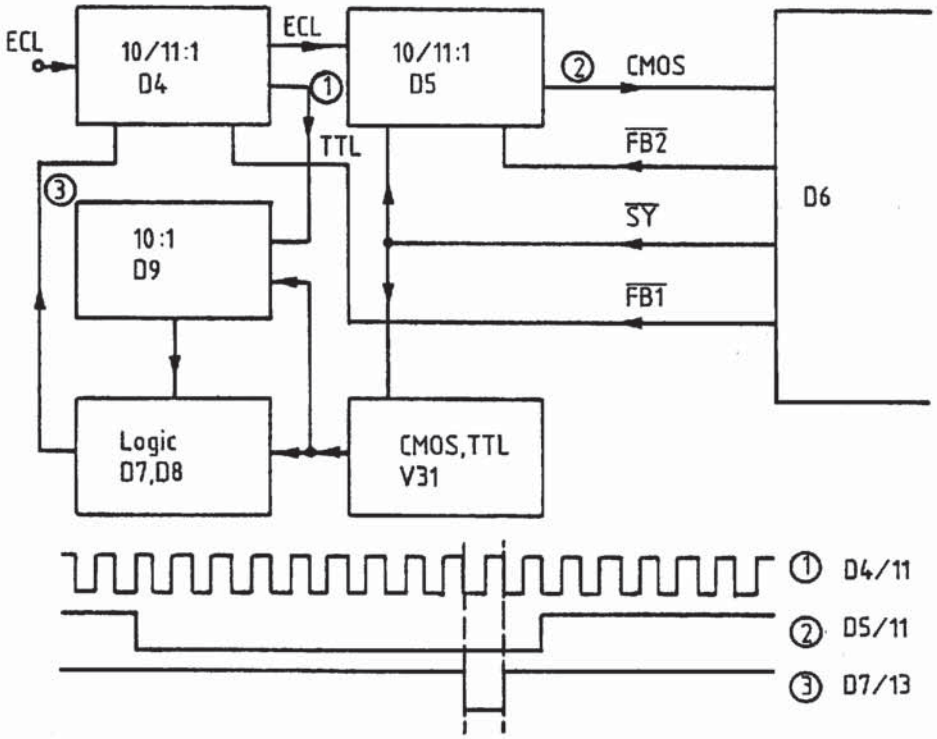


Fig. 2 Control of the prescalers D4, D5

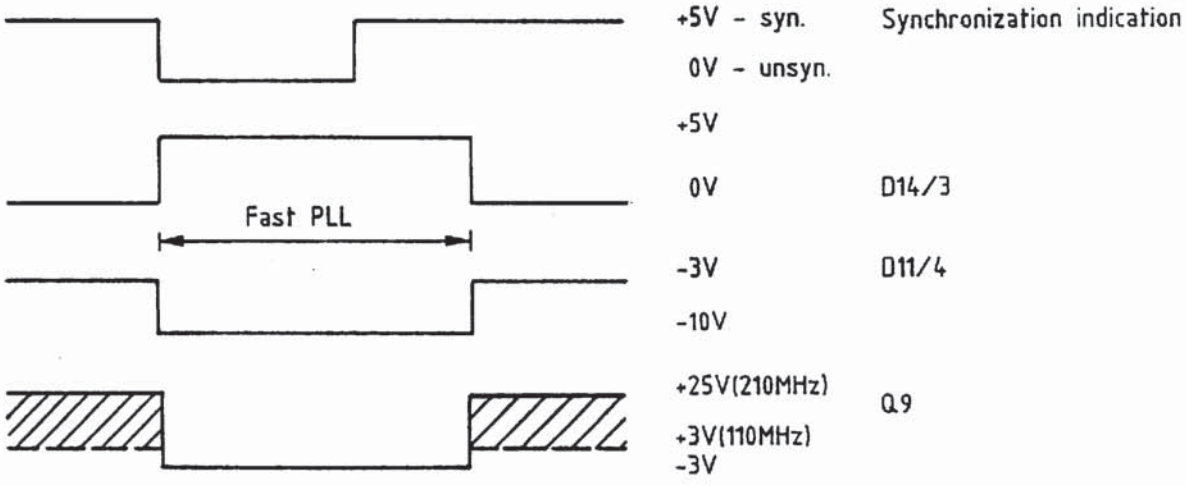


Fig. 3 Synchronization process

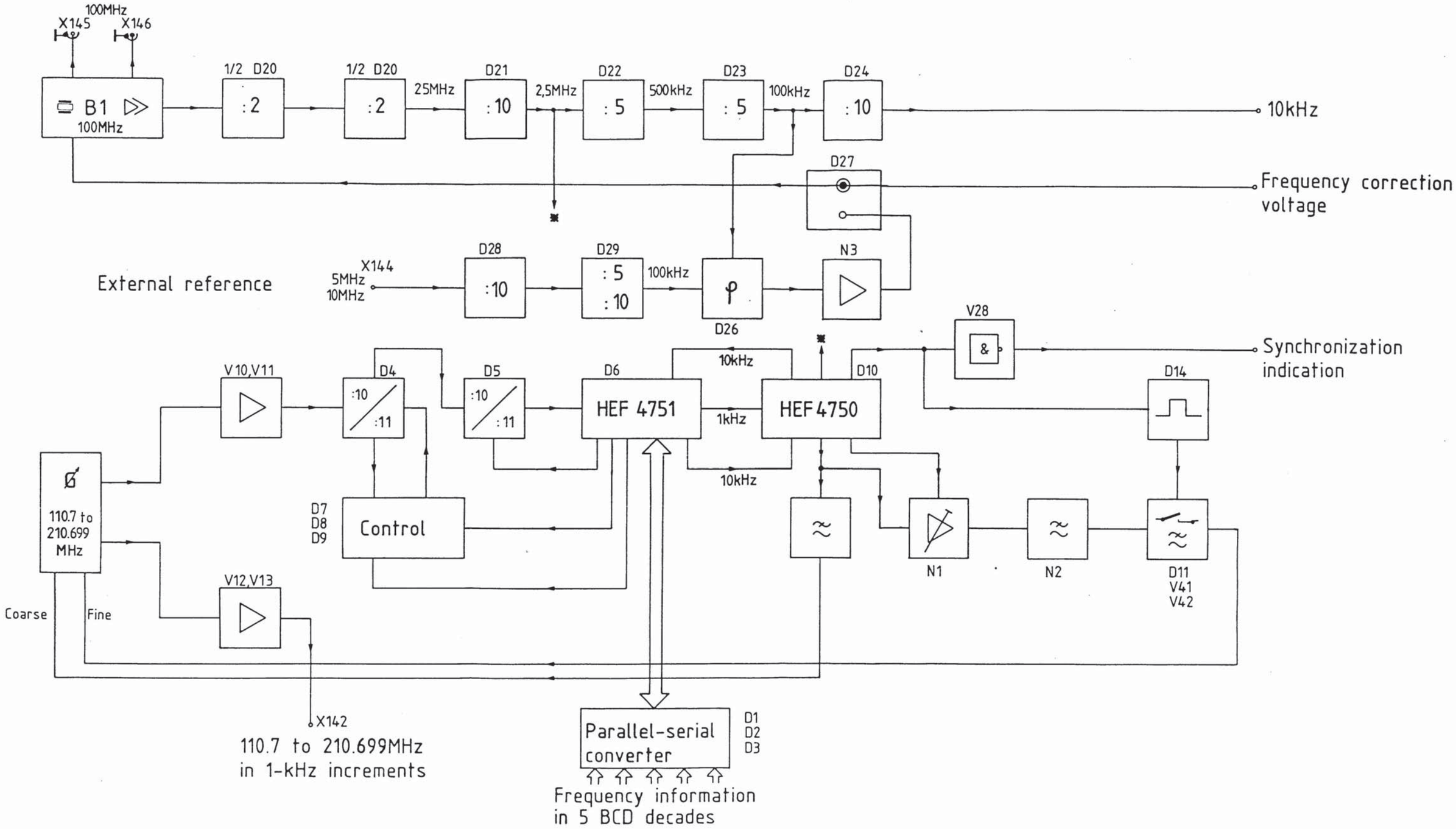


Fig. 4 Block diagram of synthesizer 2

5.2 Checking and Adjustment Procedures

Checking the current drain:

Voltage	Tolerance	Current	Tolerance	Pin
+5.40 V	±0.05 V	160 mA	±40 mA	a2, b2
+10 V	±10 mV	6 mA	± 2 mA	a4
+12 V	±0.1 V	70 mA	±10 mA	a3, b3
+30 V	±0.1 V	9 mA	± 2 mA	a5
-10 V	±0.1 V	5 mA	± 1 mA	b4
0 V	-	-	-	a1, b1, a31, b31

Adjustment of the reference circuit
(See circuit diagram 342.5003 S, sheet 2)

-Connect a spectrum analyzer to X145 and a frequency counter to X146.

-Apply +5.5 V to X141.a8.

-Use L901 to adjust the oscillator to 100.000 MHz.

-By varying the tuning voltageat X141.a8 from +3 V to +9 V, the oscillator can be pulled by ± 1 kHz to ± 1.5 kHz.

-If the pulling range is too small towards higher frequencies, reduce the voltage at X141.a8 to +5 V and readjust the oscillator.

-If the pulling range is too small towards lower frequencies, increase the voltage at X141.a8 to +6 V and readjust the oscillator.

-By varying C99 (4.7 pF to 8.2 pF, N750), the pulling range can be decreased or increased.

-By reducing C104 (56 pF to 27 pF, N750), the pulling range can be shifted towards higher frequencies.

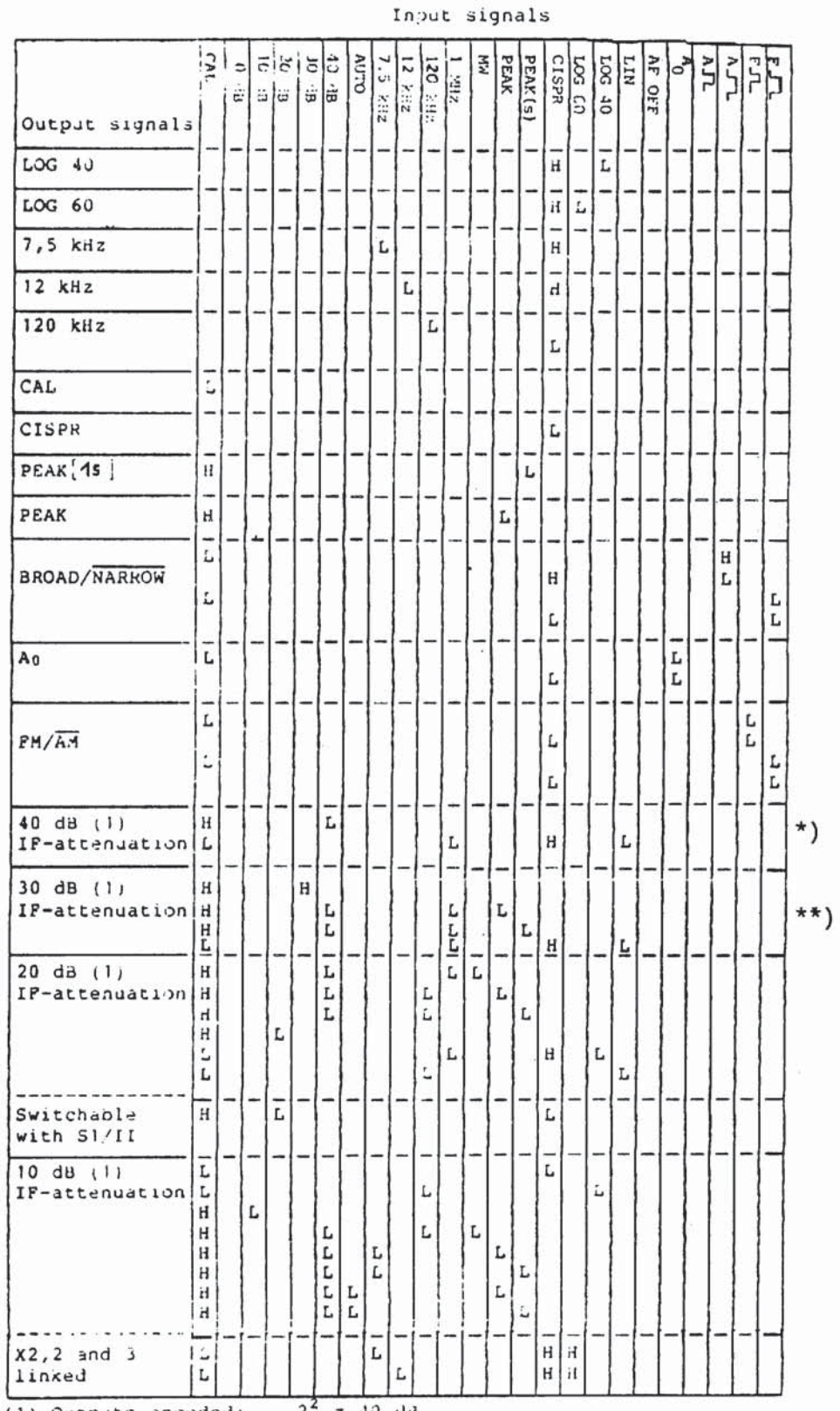
-Increasing the tuning voltage at X141.a8 to +10 V-► the oscillator must not stop oscillating.

-Switch the oscillator on and off repeatedly in order to check for proper oscillation build-up.

Check for spectral purity:

Non-harmonic spurious signals between 0 and 1 GHz...down 90>dB (harmonic excepted).

Table 1 Logic functions



(1) Outputs encoded: 2^2 = 40 dB
2^1 = 30 dB V 20 dB
2^0 = 30 dB V 20 dB

*) only for model 02

**) only for model 55

Adjustment of 110.7-to-210.699-MHz oscillator

Remove links X2 and X4.

Apply DC voltage of +5 ±0.2 V to X1, pin 1.

Apply DC voltage adjustable between +3 and +25 V to X3, pin 1.

Connect frequency counter to X142. Bend T2 so that

f = 110 MHz is obtained with a DC voltage of > +3 V;

f = 211 MHz is obtained with a DC voltage of < +25 V.

The typical coarse tuning voltage/frequency characteristic is shown in Fig. 5

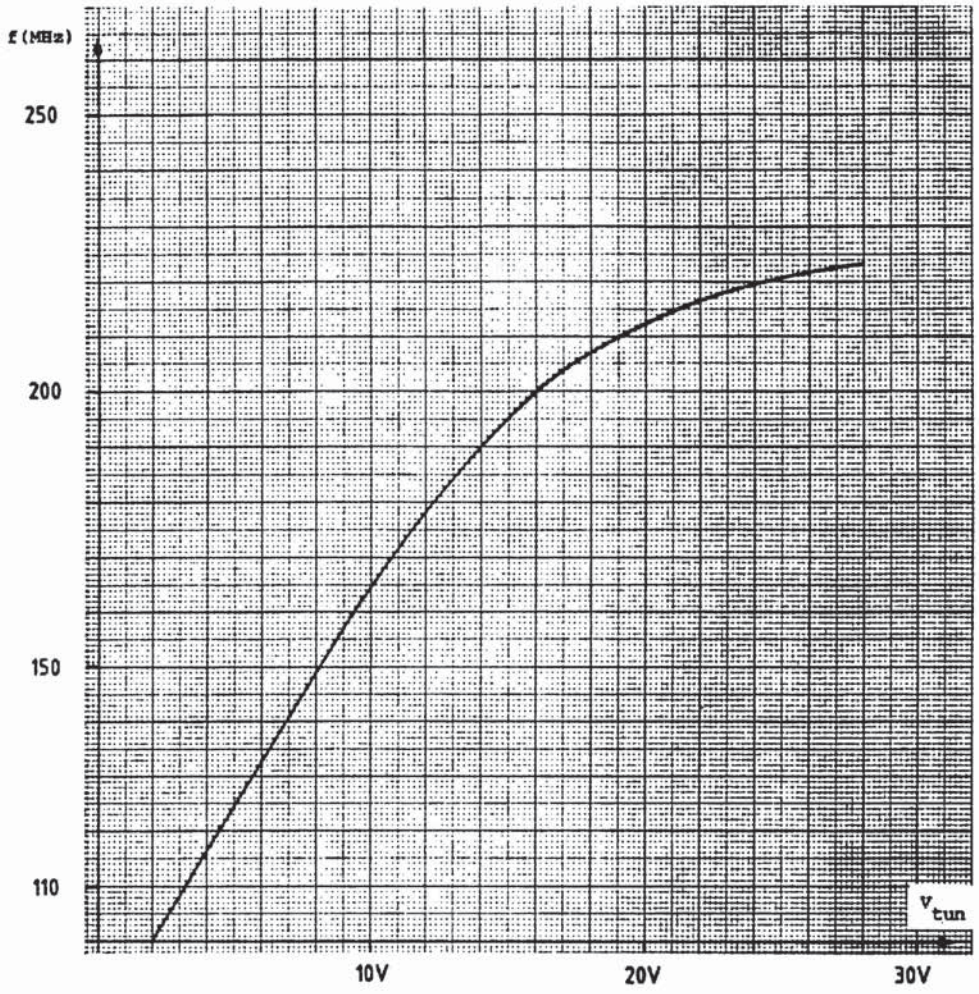


Fig. 5 Typical coarse tuning characteristic of the 110-to-210-MHz oscillator

Checking the fine tuning

Adjust frequency of 110.7 MHz by varying the coarse tuning voltage (X3, pin 1). Vary the fine tuning voltage between +4 and +6 V in 0.5-V steps.

Tuning characteristic: min. 80 kHz/V; max. 180 kHz/V.

Check at 210.7 MHz:

Tuning characteristic: min. 160 kHz/V; max. 240 kHz/V.

The typical fine tuning voltage/frequency characteristic is shown in Fig. 6.

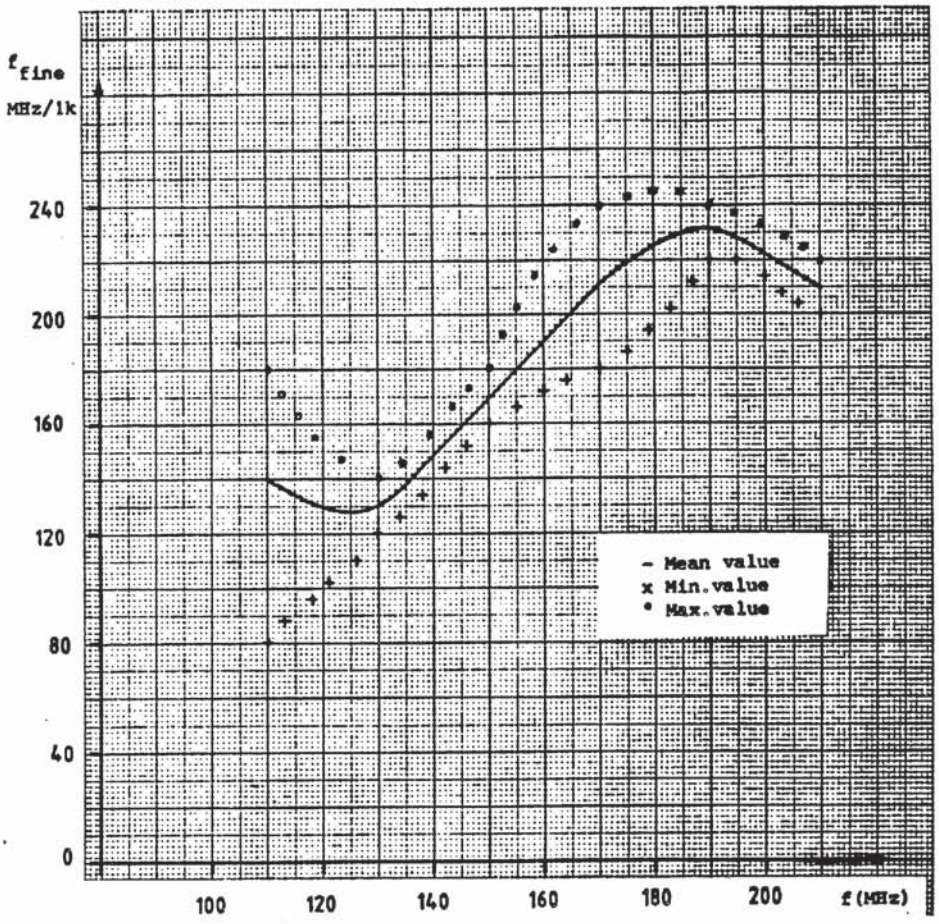


Fig. 6 Typical fine tuning characteristic of the 110-to-210-MHz oscillator

Check the operating points of V11 and V13:

Measure the DC voltage at P1 and P2: +7.3 V ±0.2 V.

Check the RF level at X142 with selective measuring instrument (test receiver, analyzer)

f (110.7 to 210.7 MHz) +4 dBm ±2 dB

Check the ECL dividers (using low-capacitance probe and oscilloscope):

D4: pins 1, 16

D4: pin 9

D4: pin 11

D5: pin 11

Caution: D4 is a selected IC and must not be interchanged witch D5!

Check the complete divider chain:

The frequency from the oscillator V14 is applied to the RF input X142 of the ratio counter.

A frequency corresponding to the five-decade frequency setting (ab11 to a29) plus 11070 (P8/1) or 110700 (P8/2) is applied to the ratio input of the counter via test point P8/1 or P8/2. Check accuracy to within at least ten frequencies between 110.7 and 210.699 MHz.

Check the reference voltage at D10, pin 22:
f = 2.5 MHz, level 10 V CMOS

Check the reference voltage at C10, pin 25, 26 or D6, pin 13:
f = 10 kHz, level 10 V CMOS

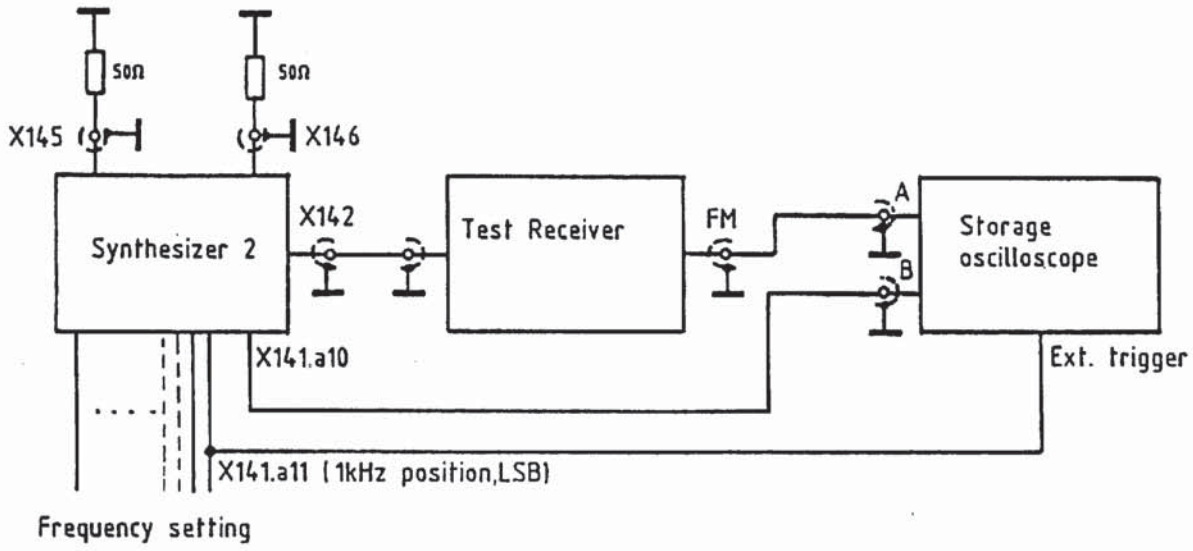
Insert links X2 and X4.

Check synchronization indication at a10:
Synchronized: high = +5 V
Not synchronized: low < 0.5 V.

With synchronization the frequency counter should read out the frequency setting of the five decades plus 110.700.

Adjustment of synchronization and transient response time:

Test setup:



Test receiver setting:

IF bandwidth: (1 V/kHz at FM output)		7.5 kHz
IF attenuation:		40 dB
RF attenuation:		30 dB

The following setting times should be obtained (max. deviation from the final frequency < 3 kHz):

Frequency jump (at X142)	Synchronization active (X141.a10 low)	Transient response time of slow PLL
111.001 → 111.02 MHz	-	≤ 20 ms
189.981 → 190.000 MHz	-	≤ 20 ms
210.680 → 210.699 MHz	-	≤ 20 ms
110.999 → 116.300 MHz	typ. 10 ms	≤ 35 ms
210.699 → 110.700 MHz	max. 70 ms	≤ 35 ms

The transient response time of the slow PLL is the time required for the synthesizer to reach the final frequency when the synchronization is no longer active (high).

The transient response time is adjusted by means of R901.

If necessary, C48 (6 pF) can be fine adjusted over the range of 3.9 to 8.2 pF (N150).

Check sideband characteristics of signal at X142. Use selective measuring instrument (with low inherent sideband noise, e.g. analyzer).
Phase noise:

f = 110.7 MHz down > 105 dB/Hz 2.5 kHz from carrier
f = 210.699 MHz down > 100 dB/Hz 2.5 kHz from carrier

Discrete signals:
The following discrete signals may occur:
n x 1 kHz --> phase modulation by the reference
n x 1.25 kHz --> crosstalk of the clock frequency from D6, D1, D2, D3

Level: down > 60 dB at f = 1 kHz
down > 70 dB at f = 2 kHz
down > 90 dB at f > 10 kHz

Check the synchronization time:

The maximum permissible time for frequency switching from the input of the new frequency until synchronization indication is high:
70 ms.

5.3 Troubleshooting

Reference circuit:

a) No level present at X145, X146:
Check operating pulses of
V51, V52, V53: V_{source} to ground +3 V $^{+50\%}_{-30\%}$
Adjust L901.
Check crystal.

b) No 10-kHz reference frequency:
Check divider chain D23, D22, D21,
D20II, D20I, V55, V54.

c) No synchronization with external reference frequency:
Check 100-kHz TTL level at P5 and P6.
Check switchover of control voltage by means of D27.
In the case of inappropriate control of D20 the control frequency may be exactly 100 MHz but due to phase jitter of D20 spurious modulation may be such that slow synchronization is not possible.

110.7-to-210.699-MHz loop

a) Loop does not lock at any frequency entered.
Check reference frequency at P3.
Check divided-down oscillator frequency at P6 and P8/3.
Check divider chain D6, D5, D4.
Check frequency input D6, D3, D2, D1.
Check oscillator, oscillator amplifier stages and the two tuning voltages.

b) Wrong synchronization of the loop in the low-order digits of the frequency:
Check performance of D7, D8, D9.
Check the two ECL dividers D4, D5.

c) Loop unsteady with input frequency > 80 000:
Wrong setting of R901 or R71 too low.
Excessive gain of fine tuning (C48, V1).

d) Wrong division at f = 140 MHz ±10 MHz:
Inappropriate operating point of D4.

e) High spurious deviation despite synchronization:
Check time constant switchover (D14, D11, V41, V42).

f) Spurious:

n x 1 kHz: Check the low-pass filters of the control lines

n x 1.25 kHz: Leakage, crosstalk from the centre card frame.