5. Repair

5.1 Measuring Instruments and Auxiliary Equipment Required

The measuring instruments and auxiliary equipment required are listed in Table 5-17.

5.2 Failure Location

In the following test, instructions are given for locating typical possible trouble sources. See also section 2.3.20 which describes the error messages that can be produced by the software of the Test Receiver ESH 3 when it identifies certain trouble sources.

Section 5.3 contains adjustment procedures and instructions for checking the various boards. For checking the performance specifications of the receiver refer to section 3.

5.2.1 No Response at Switch-on or Readout Makes no Sense

a) Failure symptoms:

At switch-on, the 13-digit display, frequency indication, RF attenuation and demodulator operating range indication, the analog indication and the individual LEDs associated with the device functions do not light up, the readouts obtained make no sense or there are combinations that make no sense, or there is no response to the push of a key.

b) Locating the fault:

- Check the LEDs which monitor the supply voltages of the Analog Power Supply.
- Check the following plug-and-socket connections:
  ST9 (Computer board/Analog Power Supply),
  BU3 (Computer board/Display Unit) and
  ST15 (Motherboard/Analog Power Supply)
  BU4/ST3 (Computer board/Memory board).
- Check the voltage on the Computer board:

ST9 3a,b/4a,b/5b	5 V ±5%
ST9 6a,b	+12.0 V
ST9 7a	+10.0 V
ST9 7b	-10.0 V

- Check the voltage on the Display Unit:

ST3 9 to 13	+5 V
ST3 14	-10 V
ST3 15 to 16	+12 V

- Check the links B1 to B5 on the Computer board and the shorting link ST1 on the Display Unit.

- Check the microprocessor on the Computer board:

RESET input	ST16/3 and B2/36	HIGH potential
CLOCK output	B2/37	3-MHz TTL level
RD and WR outputs	B2/32 and B2/31	Pulses, depending on program

and carry out signature analysis testing as described in 5.3.1.2.

- Check the microprocessor on the Display Unit:

RESET input	ST2/7 and B67/4	HIGH potential
PROG. input	B67/25	Pulses depending on program

and carry out signature analysis testing as described in 5.3.1.1.

5.2.2 Receiver Fails to Self-calibrate

a) Failure symptom:
After the CAL. button 15 has been pressed, the calibration process is interrupted by an error message (time exceeded).

b) Locating the fault:

Settings on the ESH 3: Indicating mode 35 : AV.
Operating range 33 : 20 dB

The supply voltages and 500-Hz and 100-kHz reference frequencies must be checked.

- Check the level and the frequency in the TWOPORT mode 38.
  Level into 50 Ω .... -27 dBm ±1 dB

- Check the level and the frequencies at the four inputs of the calibration generator Y10 as follows:

  Inputs:

ST4:	31.5 kHz 31.0 kHz (depending on demod. mode) ... 30.0 kHz 28.5 kHz	-15 dBm (±1 dB)
ST5:	8.97 MHz	-13 dBm (±1 dB)
ST6:	66.0015 MHz 66.0000 MHz .... 65.9985 MHz	-15 dBm (±1 dB)
ST3:	Receiver frequency +75 MHz	-15 dBm (±1 dB)

  Outputs:

ST2:	Receiver frequency	-27 dBm (±0.3 dB)
ST1:	Receiver frequency	-67 dBm (±0.3 dB)

- Connect RF socket 45 to GEN. socket 44 with a BNC cable. Set RF attenuation 40, 41 to 10 dB:

Attenuator (Y16)	BU2	-37 dBm (±1 dB)
Filter 2 (Y8)	ST8	-38 dBm (±1 dB)
Mixers 1/2 (Y9)	ST7	-2 dBm (±3 dB)

- Set RF attenuation and IF attenuation 40, 41 to 50 dB and 40 dB, respectively.

  RF level at ST5 of Mixer 3 (Y11) .... -22 dBm (±3 dB)

- Voltage on pin ST1/a2 of the Indication and AF Demodulation board (Y12) .... +1 to +2 V

The analog level indication 14 must give about full-scale deflection (right-hand scale end).

If not, the fault is in the AGC amplifier of the Analog Circuit (Y3) or in the Mixer 3 (Y11).

5.2.3 Receiver Self-calibrates but Indication Incorrect in AV. Mode

Settings on the ESH 3: Operating mode 38 : TWOPORT.
All other settings same as under 5.2.2.

Level at BU2 of the Attenuator Y16 .... -67 dB $\pm$0.3 dB

The fault is in the feedback amplifier on the Analog Circuit board (Y3) (reference).

5.2.4 Receiver Self-calibrates but Indication Incorrect in CISPR Mode

Apply 2 mV EMF at receive frequency.

Level indication 13 .... 60 dBµV

If the indication is incorrect, check the following functions:

- Demodulation and weighting of the indicated signal on the Indication and AF Demod. board (Y12).
- IF bandwidths of Mixer 3 (Y11) and Mixers 1 and 2 (Y9).
- Calibration pulses produced by the Calibration Generator (Y10).

If the indication is correct, check the IF bandwidths of Mixer 3 (Y11) and Mixers 1 and 2 (Y9).

5.2.5 Error Messages of ESH3 and Possible Causes

ERROR 01

The frequency entered is too high (> 30 MHz).
→ Operating error

ERROR 02

The frequency entered is too low (< 0.009 MHz).
→ Operating error

ERROR 03

The error 03 may occur during the brief calibration if the overall gain of the receiver deviates by more than 0.5 dB from the value determined in the course of the last total calibration. By this error message the user is requested to carry out a total calibration. The message does not implicate a device error.

ERROR 05

Level calibration at 1 MHz during the brief or total calibration cannot be terminated within the internally fixed time (deviation from nominal value: >6 dB).

Possible causes:

→ Error of calibration generator. Check as described in sections 5.3.1.10 and 5.2.2.
→ Error in signal path. Check as described in 5.2.2.

ERROR 07

This error may occur during total calibration. The error message informs the user of a correction value exceeding the specified tolerance. If level calibration at 1 MHz is not possible, the ERROR 05 message appears.

During calibration in the Talk-only mode, all correction values can be output to a printer via the IEC bus (printer address: Listen Only). All correction factors up to the last valid value are printed out before the calibration is aborted, thus enabling the user to find the cause of error.

Separated by a blank line, the correction values are printed out in the following sequence:

- Correction values for gain at the different bandwidths and correction values for CISPR 1 (f > 150 kHz) and CISPR 3 (f < 150 kHz; altogether 4 values):
  2.4 kHz,
  500 Hz (1 kHz for model 56),
  200 Hz,
  CISPR 1
  CISPR 3

- Linearity correction values for 20-dB operating range
  (3 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- Linearity correction values for 40-dB operating range
  (5 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- Linearity correction values for 60-dB operating range
  (7 values; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 3 dB).

- MIL correction value for 10-kHz IF bandwidth
  (1 value; abort of calibration if deviation > 6 dB, flashing of level indication if deviation > 4 dB).

- Frequency-response correction values (for frequency and level)
  With a deviation of > 6 dB from the nominal value (= 0 dB), the calibration is aborted; if the deviation is > 4 dB, the indication flashes.

In case of aborted calibration, proceed as follows to find the cause:

If an appropriate printer is not available, the source of error can be found by observing the calibration process.

If ERROR 07 occurs at the beginning of the calibration (receiver at 1 MHz), carry out the following tests:

▶ **Check the calibration generator:**

Settings on the ESH 3: Frequency 1: MHz
Generator: ON

Connect a power meter to the generator output.
→ Level at generator output: -27 dBm ±0.3 dB

If an error has been found, check the calibration generator as described in section 5.3.1.10.2.

▶ **Check the gain at all IF bandwidths:**

Settings on the ESH 3: Frequency: 1 MHz
Generator: ON

Connect the generator output to the RF input using a short BNC cable.
→ Select the IF bandwidths successively. The level indication is 0 ±6 dB at every IF bandwidth (abort criterion; ideal value < ±2 dB).

In case of an error, check the 1st + 2nd mixer PCB (5.3.1.9.5 to 5.3.1.9.8) and the 3rd mixer PCB (5.3.1.11.8).

- **Check the CISPR indication:**

Settings on the ESH 3: Frequency: 1 MHz
Generator: OFF
Indication mode: CISPR
RF attenuation: 40 dB
IF attenuation: 30 dB

Apply a sinewave signal (1 MHz, 60 dBµV) to the RF input.

→ The receiver indicates 60 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).
Apply the CISPR-1 standard pulse (100-Hz pulse frequency) to the RF input (see 3.2.1.4).
→ The receiver indicates 60 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

Set the frequency to 100 kHz and the RF attenuation to 20 dB.
Apply a sinewave signal (100 kHz, 40 dBµV) to the RF input.
→ The receiver indicates 40 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

Apply the CISPR-3 standard pulse (25-Hz pulse frequency) to the RF input (see 3.2.1.3).
→ The receiver indicates 40 dBµV ± 6 dB (abort criterion; ideal value < ± 2 dB).

- **Check the indication linearity:**

Settings on the ESH 3: Frequency: 1 MHz
IF attenuation: 40 dB
RF attenuation: 50 dB
IF bandwidth: 200 Hz
Indication range: 20 dB

Increase RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max. (abort criterion; ideal value < 1 dB).

Select 30-dB RF attenuation and 40-dB indication range.
Increase RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max. (abort criterion; ideal value < 3 dB).

Select 10-dB RF attenuation and 60-dB indication range.
Inrease RF attenuation in steps up to 70 dB.
→ The indication deviates from the starting value by 6 dB max. (abort criterion; ideal value < 3 dB).

In case of an error, check the indication section on the indication and AF demodulation PCB as described in 5.3.1.12.2.

When the calibration is aborted while the frequency response is measured, check the preselection filter on the filter 1 or filter 2 PCB, depending on which filter is in circuit when the abort occurs. The cut-off frequencies of the filters are specified in Tables 5-2 (section 5.3.1.7) and 5-3 (section 5.3.1.8). Check according to 5.3.1.7 and 5.3.1.8.

If no error is found in the input filters, check the oscillator level at input ST3 (X3) of the 1st + 2nd mixer PCB (nominal value: +23 dBm ±2 dB).

ERROR 08:

The memory register called up with RCL is not occupied.
→ Operating error

Voltage supply errors:

ERROR 10:

Error in +10-V supply. The voltage is either not available or not within tolerance. The +10-V LED on the power supply lights.
→ Remove power connector from motherboard. If the +10-V LED goes out, one of the PCBs is faulty, if it remains lit, trace the error in the power supply.
→ In case of a PCB error, remove the PCBs one after the other until the error has disappeared.

ERROR 11:

Error in -10-V supply. The voltage is either not available or not within tolerance. The -10-V LED on the power supply lights.
→ Trouble-shooting analogous to that of ERROR 10.

ERROR 12:

Error in +12-V supply. The voltage is either not available or not within tolerance. The +12-V LED on the power supply lights.
→ Trouble-shooting analogous to that of ERROR 10.

ERROR 13:

Error in +25-V supply. The voltage is either not available or not within tolerance.
→ Power consumption too high or short circuit on one of the PCBs
synthesizer 1,
synthesizer 2,
mixers 1 + 2 or
analog circuit.
→ Error in power supply.
Remove the PCBs one after the other until the error has disappeared.

ERROR 14:

Error in +30-V supply. The voltage is either not available or not within tolerance.
→ Power consumption too high or short circuit of filter control PCB.
→ Error in power supply.

ERROR 20 to ERROR 41:

These errors are operating errors. They are defined in Table 2-6 of the ESH 3 Operating Manual.

Synthesizer errors:

ERROR 51:

The 1st oscillator (75 to 105 MHz) on the synthesizer 1 PCB does not lock.

Trouble-shooting:

- Check 65-to-65.1-MHz, -16 ±2-dBm signal at ST2.
- Check 100-kHz reference at ST1.b18 (TTL level).
- Check 65-MHz amplifier on synthesizer 1 PCB according to section 5.3.1.5.4.
- Check 10-to-40-MHz amplifier on synthesizer 1 PCB according to section 5.3.1.5.5.
- Check the oscillators according to section 5.3.1.5.

ERROR 52:

The 50-to-51-MHz interpolation oscillator on the synthesizer 2 PCB does not lock.

Trouble-shooting:

- Check setting of int./ext. reference switch on rear panel of receiver.
- Check reference oscillator of synthesizer 2 according to section 5.3.1.4.2.
- Check 50-to-51-MHz oscillator according to section 5.3.1.4.3.

ERROR 53:

The 2nd oscillator (66 MHz) on the synthesizer 2 PCB does not lock.

Trouble-shooting:

- Check int./ext. reference switch on rear panel.
- Check reference oscillator of synthesizer 2 according to section 5.3.1.4.2.
- Check 66-MHz oscillator of synthesizer 2 according to section 5.3.1.4.4.

ERROR 54:

The 3rd oscillator (8.97 MHz) on the mixer 3 PCB does not lock.

Trouble-shooting:

- Check 500-Hz reference at ST1.b1 of 3rd mixer. In case of error, check synthesizer 2.
- Check 8.97-MHz oscillator of 3rd mixer according to section 5.3.1.11.2.

ERROR 55:

The 30-kHz oscillator on indication and AF demodulation PCB does not lock.

Trouble-shooting:

- Check 500-Hz reference at ST1.ab1 of indication and AF demodulation PCB. In case of error, check synthesizer 2.
- Check 30-kHz oscillator on indication and AF demodulation PCB according to section 5.3.1.12.2 h.

Several errors at a time:

If several error messages appear at the same time, they generally have a common source. The following table lists the secondary errors occurring as a result of synthesizer errors.

Source	Secondary error
Reference oscillator not available	ERROR 51, 52, 53, 54, 55
ERROR 51	-
ERROR 52	ERROR 51, 53
ERROR 53	-
ERROR 54	-
ERROR 55	-

Table 2-6 Error code list

01	Frequency entered above limit
02	Frequency entered below limit
03	CAL:CHECK Comparison frequency response correction/ current value ≥ 0.5 dB, occurs after an aborted total calibration, for example.
04	No listener on IEC bus (fault in IEC-bus controller)
05	Level or offset calibration is not accomplished within fixed time (hardware error)
07	Correction value at CAL. TOTAL > 6 dB; total calibration aborted.
08	Memory register not occupied on RCL
10 11 12 13 13	+10 V -10 V +12 V +25 V +30 V Failure of a supply voltage (the failure of the +5-V supply voltage is not indicated)
20 21 22 23 24 25	Current register Register 1 Register 2 Register 3 Register 4 Register 5 At start of automatic frequency scan, one or more values are not defined.
30 31	START frequency > STOP frequency START frequency = STOP frequency and XY recorder or ZSG 3 connected
32	MAX. PEGEL ≤ MIN. PEGEL
33	SPEC.FUNC. 61 X axis logarithmic and fstop : fstart < 1.4
40	ZSG 3 error: Error message if SPEC.FUNC. 61 is selected for SCAN RUN with ZSG 3
51	Synthesizer 1: 1st oscillator has not locked
52	Synthesizer 2: 50-to-51-MHz oscillator has not locked
53	Synthesizer 2: 2nd oscillator has not locked
54	Mixer 3: 3rd oscillator has not locked
55	Indication and AF demodulation: 30-kHz oscillator has not locked

5.3 Adjustment and Performance Check of the ESH 3

5.3.1 Adjustment of the Various Boards

To facilitate measurements on and adjustment of the boards normally plugged directly into the motherboard of the ESH 3, Rohde & Schwarz supply the Service Unit ESH2-Z7 (IN 338.4112) which permits operation of these boards outside of the receiver.

5.3.1.1 Display Unit

5.3.1.1.1 Supply Voltages

Pin	Voltage	Current
ST3.1 to .7	Ground	-
ST3.9 to .13	+5 V	max. 2 A
ST3.15 to .16	+12 V	approx. 50 mA
ST3.14	-10 V	approx. -10 mA

5.3.1.1.2 Frequency Indication

- Enter BCD-coded frequency information at ST1.1 to ST1.23.
- Check the resulting frequency indication (B18-B23).

5.3.1.1.3 Analog Level Indication

- Apply analog voltage GND to ST3.8 and 0.355 V to 3.55 V to ST2.12.
- Adjust R51
  for the first (left-hand) LED (GL40) to light up at 0.355 V and
  the last (right-hand) LED (GL43) to light up at 3.55 V.
- Adjust R47
  until the intensity of the right-hand LED array (GL42, GL43) is the same as that of the left-hand LED array (GL40, GL41).
- Apply a logic L to ST1.4 and ST2.8 and check the MIN. LED (GL38) and the MAX. LED (GL39) respectively.

5.3.1.1.4 Analog Offset Indication

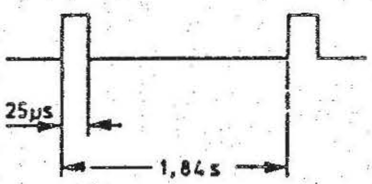
- Apply analog voltage GND to ST3.8 and 1.0 V to 4.0 V to ST1.24.
- Adjust R1
  for the two centre LEDs (GL44, GL45) to light up at 2.5 V.
- Apply a logic L to ST1.16 and check the FREQUENCY OFFSET LED (GL88).

5.3.1.1.5 Signature Analysis

The microcomputer B67 contains a signature analysis program which can be activated by changing the connection of the link ST4, and which permits checking the digital driving circuit for the 5 x 7 dot matrices and all the LEDs which indicate the device settings. First check visually that all the LEDs and dot matrices light up.

To do so:

- Change the connection of link ST4.
- Reset the processor B67 by momentarily connecting ST7.1 to ground.
- Check the clock pulses at ST7.3:



- Connect the signature analyzer to ST5 and set as follows:

  START: " "

  STOP: " "

  CLOCK: " "

  Subsequently check the board against the above diagram and signature analysis table.

5.3.1.1.6 Keyboard and Display Interface

The keyboard and display chip B61, which is a self-contained unit, is driven directly from the main processor on the Computer board and is covered by the test and signature analysis of the latter. The test is therefore carried out in conjunction with the Computer board and the relevant signature analysis table (section 5.3.1.2.2.1).

5.3.1.1.7 Difference Current Sink

- Switch on signature analysis in accordance with 5.3.1.1.5 (all the LEDs and dot matrices light up).
- Connect oscilloscope to ST3.1 to 7 (GND) and ST3.9 to 13 (+5 V) and watch screen display.

5.3.1.2 Computer Board

5.3.1.2.1 Supply Voltages

Pin		Voltage	Current
ST9	1a/1b/2a/2b	Ground	-
ST9	3a/3b/4a/4b/5a	+5 V	approx. 2 A
ST9	6a/6b	+12 V	approx. 50 mA
ST9	7a	+10 V	approx. 100 mA
ST9	7b	-10 V	approx. 100 mA

5.3.1.2.2 Signature Analysis

Free-running and software-driven signature analysis is used in fault location when testing the Computer board, which constitutes a complex digital system. With free-running signature analysis, the processor must cyclically scan its entire address range, and the start/stop signal for the signature analyzer originates directly from the address bus.

With software-driven signature analysis, a cyclic control program for all the peripheral chips is stored in the EPROMs, making for more thorough individual testing.

5.3.1.2.2.1 Free-running Signature Analysis

An initial but effective test of the Computer board can be carried out using free-running signature analysis. In this signature analysis mode, the feedback between the processor and the EPROMs memory is interrupted (bus driver B6), and driver B83 is activated, which produces a NOP instruction in every read cycle of the processor. The signatures are used for checking the processor and the EPROMs as well as the driver chips and the address decoder chips.

Settings and checks:

- To select the free-running mode, change over the connection of the links BR2 and BR5 to the position shown: BR2  ; BR5  .
- Reset the processor by: momentarily applying a logic L to ST16.2 (normally at H level); or switching the unit off.
- Check the CLOCK output B2.37 of the processor: 3-MHz clock signal at TTL level.

- Check the signatures of the address bus.

- Connect the signature analyzer to ST14.

  Settings on the 5004A:

  START , STOP , CLOCK

  Signatures B2.21 to B2.28 (≙ A8 to A15) and B5.4,
  B5.6 to B5.21 (≙ A0 to A7):

A0	UUUU	A8	HC89
A1	5555	A9	2H70
A2	CCCC	A10	HPP0
A3	7F7F	A11	1293
A4	5H21	A12	HAP7
A5	0AFA	A13	3C96
A6	UPFH	A14	3827
A7	52F8	A15	755U

  Check these signatures on the chips B1, B4, B7 as well as on the EPROMs B8, B11, B14, B15 and the socket BU4 on the Memory board.

- Check the signatures of the data bus.
  Connect signature analyzer to ST13 (contents of EPROMs).

  Settings on the 5004A:

  START , STOP , CLOCK

All the signatures are listed in the table given in the Appendix.
After the test has been accomplished, reconnect the links BR2 and BR5 in the original positions.

5.3.1.2.2.2 Software-driven Signature Analysis

The next step in testing the Computer board is a special test program provided in the EPROMs:

- Change the connection of link BR1.

- Reset the processor by momentarily applying a logic L to ST16.3.

- Check the signatures of the peripheral chips against the table given in section 5.3.1.2.2.1.

- Check the staircase signals (0 V to +10 V) at the two D/A converter outputs via B41, on the oscilloscope.

After the test has been accomplished, reconnect the link BR1 in the original position.

5.3.1.2.3 A/D Converter

All the voltages to be measured or applied are with respect to ST9.10b.

A special test routine of the processor software can be used for adjustment of the A/D converter B26, B27. For this purpose, EPROMs B8, B11, B14, B15 must be fitted, and the Memory board must be connected to BU4, just as for the signature analysis.

By changing the connection of the link BR6 and resetting the processor (logic L at ST16.3), the A/D converter continually receives start-of-conversion pulses, and its output is continuously read out.

- Adjust the reference voltage at MP3 to +5.000 V (±1 mV) by means of R6.
- Adjust the sample/hold amplifier B77:
  Connect the sample/hold input ST5.22 to ST9.10b. Adjust the voltage at MP6 to 0 V (±1 mV) by means of R12.
- Adjust the A/D converter B26:
  Apply a voltage of +5.000 V (±1 mV) to input ST5.22. Adjust the gain of the A/D converter by means of R5 such that the logic level at B30.1 is just at the switching point between H and L (= A/D converter value 1023).

  The value of the A/D converter is output directly to the 13-digit display of the Display Unit. After the adjustment has been accomplished, reconnect link BR6 in the original position.

5.3.1.3 Analog Circuit Board

5.3.1.3.1 Supply Voltages

	Pin	Voltage	Current
ST1	22a	+10 V	approx. 50 mA
	22b	-10 V	approx. -10 mA
	23b	+5 V	approx. 25 mA
	24b	GND	
	23a	+12 V	0/7.5 mA with AF off/AF on
	24a	+25 V	< 1 mA

5.3.1.3.2 General

All analog switching functions are performed by means of CMOS switches, a logic H = +10 V at the control input of the CMOS switch corresponding to ON and a logic L = < 1 V corresponding to OFF.

For driving the required inputs (Table 4-1), TTL levels must be applied which are converted to 0 or 10 V by means of level shifters.

If switches off, the resistance of the CMOS switches is > 10 MΩ, and if switched on approx. 300 Ω.

NOTE: Analog DC voltage values given assume a supply voltage of +10 V ±1%.

5.3.1.3.3 Analog Level Path

5.3.1.3.3.1 Level Calibration

- After the supply voltage has been applied, apply a variable voltage (0.2 to 2 V) to ST1/17a.
- Measure the voltage at B1/III pin 3 by means of a digital voltmeter. V_{center} = 2 V with a tolerance of ±0.02 V. While the input voltage being measured is at V_{center} ±20 mV, a +5-V signal (H level) must appear at ST1/21b signifying calibration complete.
- If $V_{in} < V_m$, the output of the comparator B1/III pin 1 should be approx. +9 V and if $V_{in} > V_m$ it should be approx. -5 V.
- If the logic signal CISPR 1 v CISPR 3 is applied, the output B1/IV pin 9 should be -9 V, and if the logic signal $\overline{\text{CISPR 1}} \wedge \overline{\text{CISPR 3}}$ is applied, it should be +9 V.

5.3.1.3.3.2 Programmable Amplifiers B2/I, B2/II

- Switch on B6/I and B6/IV (AV., 20 dB).
- Apply 2 V to ST1/17a. The voltage measured at the analog level output 7a via B6/I, B2/I, B7/III, B3/II should be 3.55 V ±2% and the voltage measured at B2/II pin 15 should be 4 V ±2%.
- Apply a logic L to the input (ST1 pin 2b).
- Measure voltage at the output to the sample/hold amplifier (ST1 pin 3a). It should be 2 V ±2%.

- When B6/III is turned on (log 40 dB or log 60 dB or etc.; see Table 4-1), the voltage at B2/II pin 15 should rise to 8 V $\pm$2%.

5.3.1.3.3.3 Adjusting the Logarithmic Converter

- Apply a variable DC voltage to pin 17a and switch on B6/I by means of B7/I.
- Switch on LIN (B7/II).
  Adjust with a digital voltmeter at pin 18a and measure at pin 7a.

- By alternately adjusting R37 and R40, the following requirements must be met:

Pin 18a	0.4 V →	pin 7a	0.355 V $\pm$1%
(V_{input})	4.0 V →	(V_{output})	3.55 V $\pm$1%.

- Repeat these adjustments alternately until these values are reached.

5.3.1.3.3.4 Max. Level and Min. Level

For test setup see 5.3.1.3.3.3.

If the input voltage is less than 0.4 V, the MIN. LEVEL LED must light up (comparator output B3/III pin 9 approx. +9 V).

If V_{in} > 4 V, the MAX. LEVEL LED must light up (comparator output B3/III pin 4 approx. +9 V).

If these LEDs do not light up as required, check T3, T4 and the signal path up to the LEDs of the Display Unit.

It must be possible to scan the entire analog level indication LED array with the V_{in} setting range 0.4 to 4 V. Beyond these range limits, the LEVEL MAX. and LEVEL MIN. LEDs must light up.

5.3.1.3.4 Frequency Offset Signal Path

5.3.1.3.4.1 Offset Calibration

- After applying the supply voltage to the board, connect a voltage source with a control range of $\pm$5 V EMF (Z_{source} = 10 kΩ) to ST1/14b. Set V_{in} to 0 V.

- Apply +5 V to ST1/5a (CAL. button).

- After this voltage has dropped (St1/5a = < 0.8 V), measure with a digital voltmeter at ST1/11a (2.5 V ±1%).
- Press CAL. button 15 and then measure.
- Repeat this process until with V_{in} (ST1/14b) = +5 V, 4 V ± 1% is obtained.
- Final testing: Set to the limit values and measure (after offset calibration).

V_{in}	V_{out} (2%) ST1/11a	V_{out} (2%) ST1/8b	V_{out} (TTL) ST1/5b	LED offset centre
0 V ±0.025 V	2.5 V	0 V	+5 V	ON
-5 V	1 V	-5 V	< 0.8 V	OFF
+5 V	4.0 V	+5 V	< 0.8 V	OFF

5.3.1.3.4.2 Peak-value Rectification

- Connect ST1/14b to ground and switch in B8/II ST1/4a = High ($\overline{m}$).
- Connect digital voltmeter to B14/I pin 15 and set 2.5 V by means of R99.
- Connect digital voltmeter to B14/II pin 1 and set 2.5 V by means of R98.
- When a logic (TTL) H is applied to 10a (peak value 50 ms), the output voltage must drop to a maximum of $V_{orig.}/2$ (storage capacitor).
- When logic H is applied to select m, Δf(-) at ST1/1a and m, Δf(+) at ST1/1b, no voltage difference must occur (< 25 mV).
- The calibrated frequency offset signal (see 5.3.4.1) can be directly connected through to the output ST1/3a.
- The level can be taken to the peak-value rectifier via B8/3 (AM measurement).

5.3.1.3.4.3 Frequency Correction Voltage

NOTE: Vary R111 only if the frequency of the mother oscillator is to be calibrated (pulled) for the synthesizers of the ESH 3 (the frequency responds only very slowly). If the frequency cannot be pulled, the setting range of R111 at ST1/20a, which should be +1 V to +9 V, can be checked using a digital voltmeter at ST1/20a.

Calibrate frequency:

- Select TWOPORT mode on the ESH 3 and connect a high-precision frequency counter to the generator output.
- Adjust by means of R111 the counter frequency to that set on the ESH 3.

5.3.1.3.4.4 AF Amplifier

- Apply supply voltage.
- Apply AF signal (V_{in} = 50 mV/1 kHz) to ST1/18b.
- Connect an oscilloscope to ST1/19a. V_{out} should be approximately 12 V_{pp} if ST1/21a (volume control 50 kΩ) is connected to ground and no loudspeaker is connected.
- Apply a logic H to ST1/13a (+5 V) to switch off the AF amplifier (T7 is cut off).
- Measure gain   Voltage gain = approx. 33; P_{out} = approx. 0.33 W into 16 Ω.

5.3.1.4 Synthesizer 2 (Y4)

5.3.1.4.1 Supply Voltages

Pin	Voltage	Current
ST1,b24	Ground	-
ST1,b23	+5.25 V ±0.1 V	approx. 110 mA
ST1,a22	+10 V ±0.1 V	approx. 25 mA
ST1,a23	+12 V ±0.5 V	approx. 60 mA
ST1,a24	+25 V ±0.2 V	approx. 6 mA
ST1,b22	-10 V ±0.1 V	approx. 3 mA
ST1,ab19	+1 to +9 V	approx. <1 mA

5.3.1.4.2 Reference

- Remove ST5. Connect spectrum analyzer to ST3. f = 60 MHz, level: approx. -20 dBm.
- Adjust L68 so that the oscillator starts oscillating and the frequency is 60 MHz if +5 V is present at ST1.ab19.
- Set maximum level by means of C160.

- Vary voltage at ST1.ab19 between +1 and 9 V at the same time checking the spectral purity of the signal.
- Check the TTL reference signals at

ST1.b18	:	f = 100 kHz
ST1.ab1	:	f = 500 Hz
B41,1	:	f = 500 Hz
B41,3,13	:	f = 1 kHz

- Apply external reference signal to ST4 (f = 5/10 MHz) from 1-V, 50-Ω source. Frequency error better than 2×10^{-6}.
- Apply +5 V corresponding to external reference to ST1.a2 and b2.
- Measure frequency at ST3, the accuracy of which must be equal to that of the external reference.
  This frequency must not change when the voltage at ST1.ab19 is varied between +1 and +9 V.
- Connect the spectrum analyzer to BU1 pin 8 and ground, which permits detailed display of the spectral purity of the reference oscillator.
- Unwanted oscillations of T1 and T3 must be avoided by short circuiting the coils L4 and L21, respectively.
  Discrete non-harmonic spurious signals should be down > 80 dB.
  Sideband noise 10 kHz away should be down > 140 dB/Hz.

5.3.1.4.3 50-to-51-MHz Oscillator

- Connect spectrum analyzer to ST5 R116/ground.
- Remove shortcircuit across L21.
- Adjust frequency to 50.05 MHz, connecting ST1.a3 to a14 as follows:
  H = a3, a5
  L = a4, a6 to a14.
- Set C42 to mid-position.
  Check level at ST5: .... -10 dBm ±2 dB at 5.005 MHz
  (Adjustment by means of R117)
  Check at ST1.b13:
  H = oscillator is synchronized
  L = oscillator is not synchronized.

If oscillator not synchronized, then use a scope to check the logic levels or oscillograms at the points given, by reference to the circuit diagram:

B19, pin 11
B20, pin 8
B22, pin 6
B24, pins 1, 3, 10, 13, 4, 12
B25, pin 12
B18, pin 23
B16, pin 14
B16, pin 3 1 kHz if synchronized
B16, pins 13, 12
B17, pins 11, 8, 9, 2

- Check voltages at B15:
  Pin 3: +2.5 V ±0.2 V
  Pin 7: +25 V ±1 V

  (Adjust by means of C24:)
  Pin 6: +6.5 V ±0.3 V.

- Apply required logic levels to vary the frequency between 50.000 and 50.999 MHz and watch at the same time the synchronization indication (b13).

- Check the spectral purity:

  Discrete non-harmonic spurious signals .... down > 80 dB

  Sideband noise 10 kHz away .... > 140 dB/Hz

  Level at ST3: f = 65.0000 to 65.0999 MHz .... -16 dBm ±2 dB

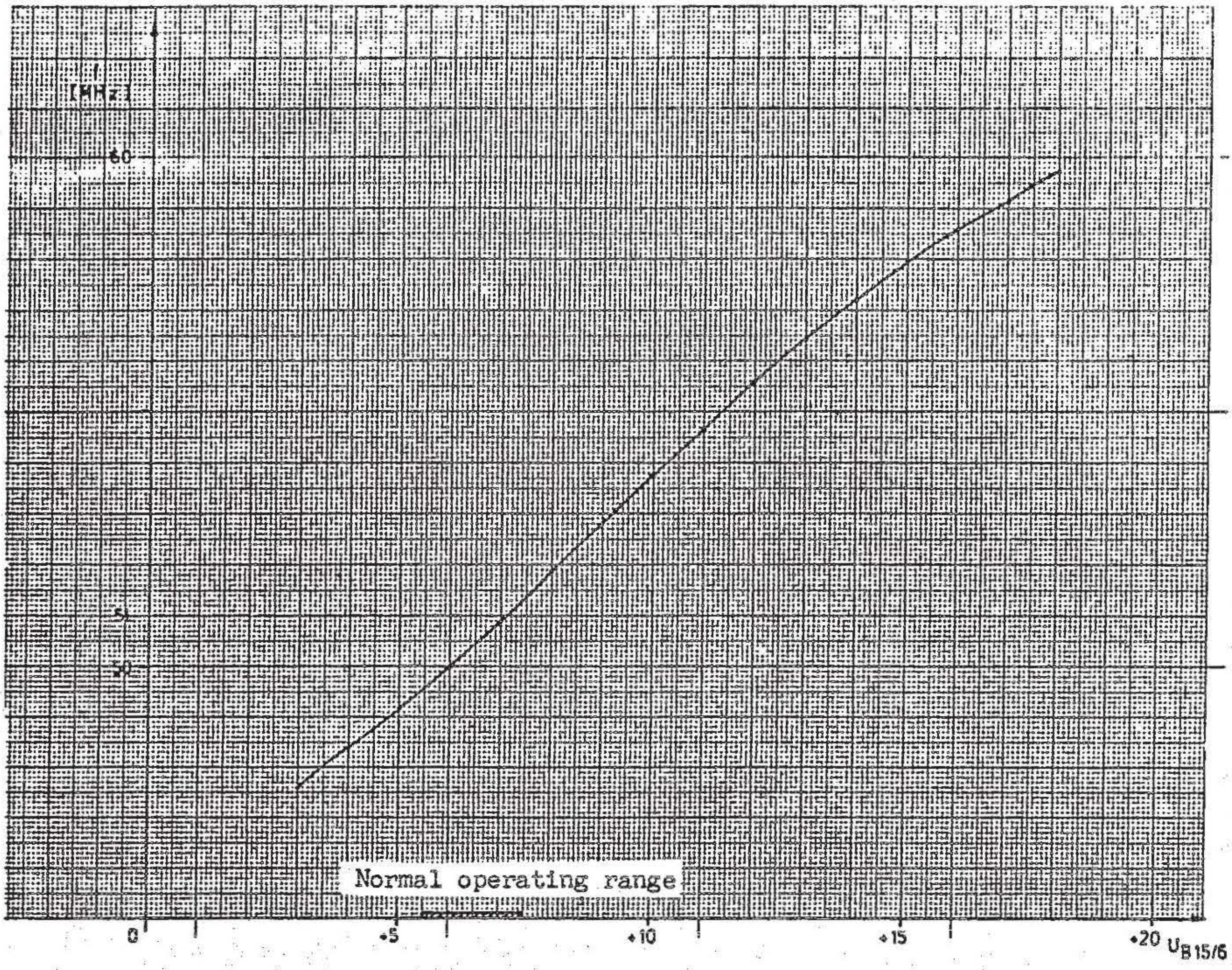


Fig. 5-1 Typical tuning characteristic of the 50-to-51-MHz oscillator

5.3.1.4.4 66-MHz Oscillator

- Connect spectrum analyzer to ST2.
- Remove short-circuit across L4.
- Rotate core of L4 inwards until the oscillator starts to operate.
  Adjust C13 for maximum.
  Level at ST2 into 50 Ω .... +7 dBm ±2 dB
  Frequency: corresponds to frequency of Q1.
- Check synchronization indication ST1.b14:
  H = oscillator synchronized
  L = oscillator not synchronized.

If oscillator not synchronized, then use a scope to check the logic levels or oscillograms at the points given, by reference to the circuit diagram:

B1, pin 11
B2, pin 8
B3, pin 6
B10, pins 1, 3, 10, 13, 4, 12
B5, pin 23
B7, pins 14, 3, 1, 2, 13
B8, pins 10, 5, 6

- Check voltages at B6: pin 3: .... +2.5 V ±0.2 V
  pin 7: .... +25 V ±1 V
  pin 6: .... see illustration

- Apply a logic H to ST1.b3: The frequency is increased by 1.5 kHz.

- Apply a logic H to ST1.b4: The frequency is decreased by 1.5 kHz.

- Check the spectral purity:
  Discrete non-harmonic spurious signals .... down > 80 dB
  Sideband noise 10 kHz away .... down > 140 dB/Hz

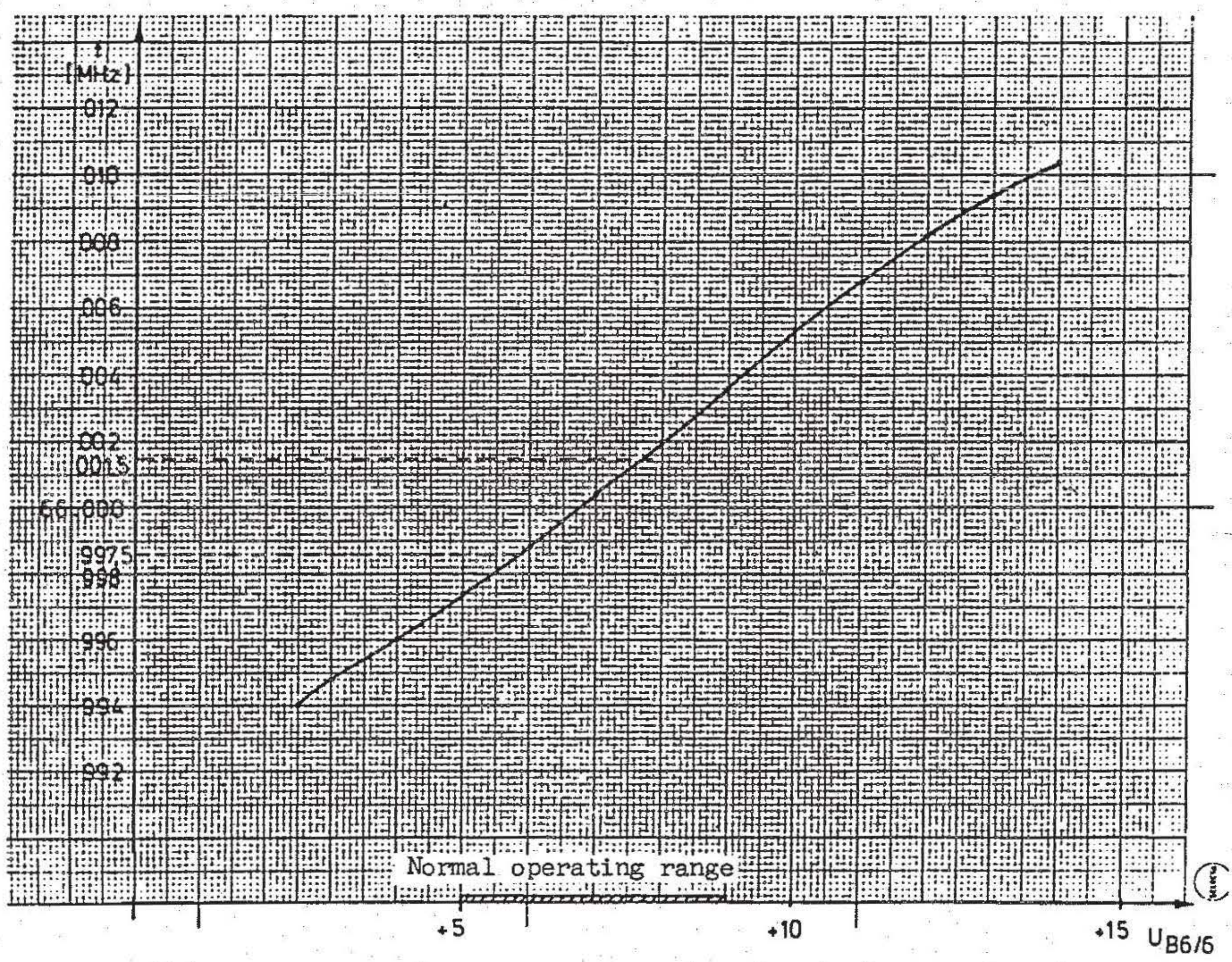


Fig. 5-2 Typical tuning characteristic of the 2nd oscillator (66 MHz)

5.3.1.5 Synthesizer 1 (Y5)

5.3.1.5.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1, b24	Ground	-	-
ST1, b23	+5.25 ±0.1 V	approx. 105 mA	0
ST1, a22	+10 ±0.1 V	approx. 35 mA	
ST1, a23	+12 ±0.2 V	max. 75 mA	0
ST1, a24	+25 ±0.1 V	approx. 4 mA	0
ST1, b22	-10 ±0.1 V	approx. 6.5 mA	0
St1, b18	TTL	< 1 mA	100 kHz
ST1, a7	TTL	< 1 mA	-
b8	100-kHz decade		-
a9			-
b10			-
a11	TTL	< 1 mA	-
a12			-
b13	1-MHz decade		-
a14			
a16	TTL	< 1 mA	-
a15	10-MHz decade		-
ST2	-17 dBm ±1 dB	-	65.0 to 65.1 MHz

5.3.1.5.2 Adjustment of 75/85/95/105-MHz Oscillators

- Connect frequency counter (50 Ω) to ST3.
- Remove B3 and connect R15 to +10 V.
  The oscillators are controlled by the TTL levels at the input lines of the decades depending on the receive frequency, and pretuned by a D/A-converted voltage.
- Check the pretuning voltage at ST1, a17 and R16:

	ST1,a17	R16
All decade inputs at logic L	0 ±5 mV	3.8 V ±20 mV
All inputs of the 100-kHz and 1-MHz decades at logic H	7.4 V ±0.2 V	17.8 V ±0.8 V

- The tuning range is adjusted by means of the variable capacitor, and the initial frequency is adjusted by means of the variable inductance (see Fig. 5-7 in the appendix).

Oscillator	Decade driving signal	Adjust with
75 to 85 MHz	0.000 to 9.9 MHz	C3, L12
85 to 95 MHz	10.0 to 19.9 MHz	C13, L13
95 to 104.0 MHz	20.0 to 29.9 MHz	C23, L14

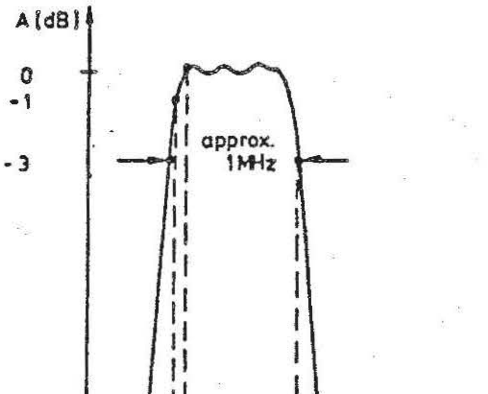
5.3.1.5.3 Adjustment of Output Level

- Connect spectrum analyzer (50 Ω) to ST3.
- Switch the decades in 1-MHz steps.
- Adjust the output level by means of C38 over the frequency range from 75 to 105 MHz to .... +23 dBm ±2 dB

5.3.1.5.4 Adjustment of 65-MHz Amplifier

Connect sweep generator (50 Ω) to ST2 and apply
level of .... -17 dBm
Frequency range .... 60 to 70 MHz

Connect display section of the sweep generator to ST7. Make coarse adjustment of L31, L32, L33 for maximum at 65.5 MHz. Connect sweep generator to ST7 (via capacitor). Level and frequency same as above. Connect display section to ST6. Make coarse adjustment of L36, L37, L38 for maximum at 65.5 MHz. Connect sweep generator to ST2. Make final adjustments to reach selectivity curve shown below.



5.3.1.5.5 Adjustment of 10-to-40-MHz Amplifier

Apply signal between 65 and 65.1 MHz with a level of 16 $\pm$1 dBm to ST2.

Check level at ST5 with the aid of a spectrum analyzer while varying the oscillator frequency between 75 and 105 MHz

Required level .... -21 dBm $\pm$2 dB

Frequency .... 10 to 40 MHz

Check level at ST4 with the aid of a spectrum analyzer by varying the oscillator frequency between 75 and 105 MHz

Required level .... +2 dBm $\pm$3 dB

5.3.1.5.6 Checking the Synchronization Indication

Synchronization indication .... logic L

(B3 removed)

5.3.1.5.7 Checking the Synchronization

Insert B3.

Apply 100-kHz reference (crystal-controlled, with low sideband noise).

Synchronization indication .... logic H

Voltage at R15 (depending on f) .... > +3 to < +19 V

5.3.1.5.8 Checking the Sideband Noise

The signal at ST2 should have minimal sideband noise.

1 kHz away .... down typ. 90 dB/Hz

10 kHz away .... down typ. 135 dB/Hz

The 100-kHz reference must be crystal-controlled with low sideband noise.

The typical sideband noise characteristic is shown in Fig. 5-3.

Excessive variations at A can be corrected by varying the gain of B3 (R95).

If there are considerable, abrupt frequency changes or warm-up transients, then that points to problems with the oscillators.

Required rejection of discrete signals over the range 0 to 50 kHz from the carrier (measured at an analyzer IF bandwidth of 10 Hz) .... typ. > 100 dB

Time required for synchronization after any change in frequency .... < 100 ms

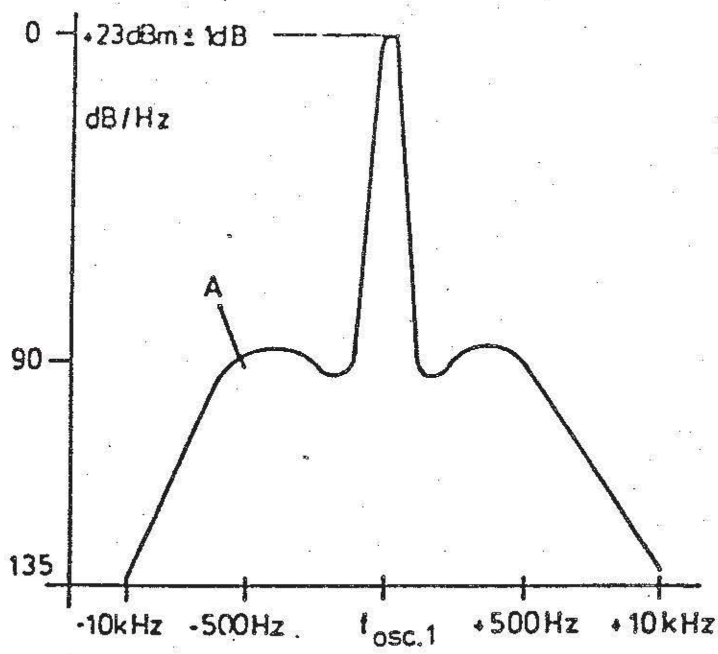


Fig. 5-3 Characteristic of typical sideband noise

5.3.1.6 Filter Control (Y6)

5.3.1.6.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	+5.25 V ±0.1 V	approx. 3 mA	0
ST1.a22	+10 V ±0.1 V	approx. 1.5 mA	0
ST1.a24	+30 V ±0.5 V	approx. 0.7 mA	0
ST1.b22	-10 V ±0.1 V	approx. 3.5 mA	0
ST1.b17	0 to 7.5 V	< 1 mA	0
ST1.ab1	TTL	-	500 Hz

5.3.1.6.2 Checking the Digital Section

Connect ST1.b20 via 470 Ω to ground.

Apply logic levels to pins ST1, 3 to 16.

Truth table

f(MHz)	Range	High level St1, a...	ST1, a2
0 to 0.14	1	21	L
0.15 to 0.19	2	19	L
0.2 to 0.27	3	17	L
0.28 to 0.38	4	15	L
0.39 to 0.53	5	13	L
0.54 to 0.74	6	11	L
0.75 to 1.04	7	9	L
1.05 to 1.44	8	7	L
1.45 to 1.99	9	6	H
2.0 to 2.69	10	8	H
2.7 to 3.69	11	10	H
3.7 to 5.19	12	12	H
5.2 to 7.19	13	14	H
7.2 to 9.99	14	16	H
10 to 19.99	15	18	H
20 to 29.99	16	20	H

While the range is being selected, St1.b20 is at low level.

Maximum time required for range selection .... < 35 ms.

5.3.1.6.3 Checking the Analog Section (Pre-adjustment)

Increase the input voltage at ST1.b17 in steps of 75 mV from 0 V to +7.4 V. The resulting output voltage at ST1.a4 and the trimmers used are shown in Table 5-1.

Table 5-1

Input voltage (V)	0	+0.75	+3.75	+6.75	+7.4
Adjusting element	R79	R55	R70	R89	R103
Output voltage (V)	+3±0.1	+6±0.1	+13.75±0.1	23±0.1	26±0.1

Make final adjustment together with Filter 2 (Y8) for minimum input reflection coefficient in range 15.

5.3.1.7 Filter 1 (Y7)

Supply voltages:

Pin	Voltage	Current
ST1.b24	Ground	-
ST1.b23	+5.25 V ±0.1 V	approx. 30 mA

Switch in the desired filter by applying a logic H to pins ST1.a7 to a21. Adjust filters 1 to 8 for a reflection coefficient characteristic in accordance with Fig. 5-4 using a sweep-frequency network analyzer.

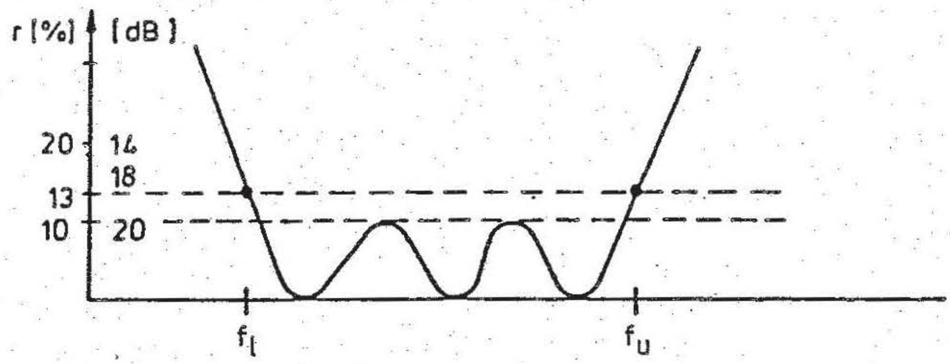


Fig. 5-4 Reflection coefficient characteristic of the fixed-tuned filters

Reflection coefficient within the filter range .... < 10%

Reflection coefficient at the cut-off frequencies .... < 13%

Insertion loss .... < 0.5 dB

Attenuation at $f_u/2$ .... > 18 dB

Test setup:

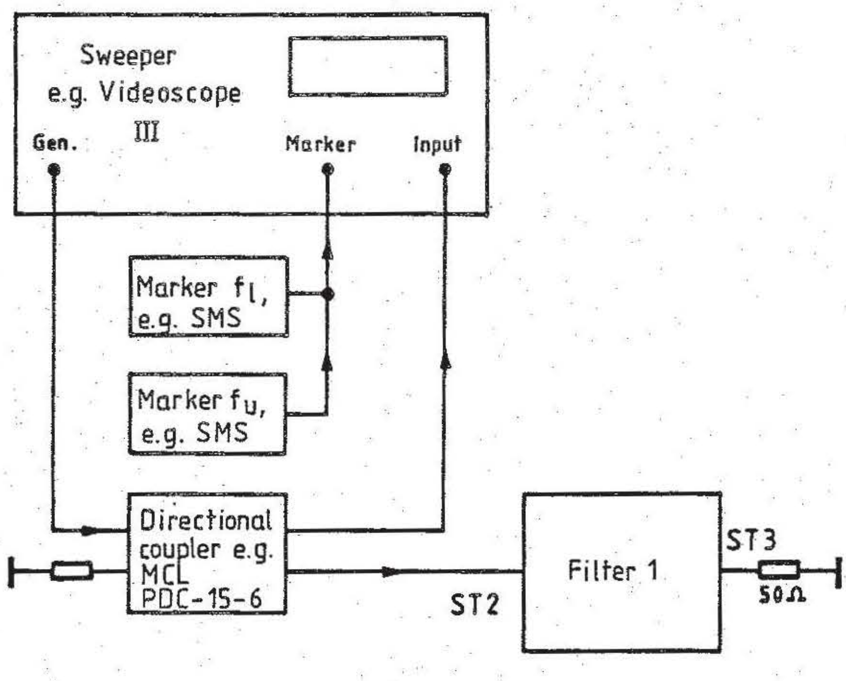


Table 5-2

Filter	Cut-off frequencies f_l	f_u	Adjust with	Logic H to ST1.a...
1	10* kHz	150 kHz	L2, L3, L4	21
2	150 kHz	200 kHz	L5, L6, L7	19
3	200 kHz	280 kHz	L10, L11, L12	17
4	280 kHz	390 kHz	L15, L16, L17	15
5	390 kHz	540 kHz	L20, L21, L22	13
6	540 kHz	750 kHz	L25, L26, L27	11
7	750 kHz	1.05 MHz	L30, L31, L32	9
8	1.05 MHz	1.45 MHz	L35, L36, L37	7

* f_l = 20 Hz for model 56 (subassembly model 53)

5.3.1.8 Filter 2 (Y8)

5.3.1.8.1 Supply Voltages

Pin	Voltage	Current
ST6.b24	Ground	-
ST6.b23	+5.25 V ±0.1 V	approx. 30/60 mA
ST6.a2	Logic H	< 0.5 mA
ST6.a4	+3 to +28 V	< 0.1 mA

Switch in desired filter by applying a logic H to pins ST6.a6, 8 to 20. Adjust filters 9 to 14 similarly to 5.3.1.7 in compliance with the following table:

Table 5-3

Filter	Cut-off frequencies f_l	f_u	Adjust with	Logic H to ST.a...
9	1.45 MHz	2.0 MHz	L40, L41, L42	6
10	2.0 MHz	2.7 MHz	L45, L46, L47	8
11	2.7 MHz	3.7 MHz	L50, L51, L52	10
12	3.7 MHz	5.2 MHz	L55, L56, L57	12
13	5.2 MHz	7.2 MHz	L60, L61, L62	14
14	7.2 MHz	10.0 MHz	L65, L66, L67	16

Feed in test signal to ST7 (terminate with 50 Ω at ST8).

5.3.1.8.2 Adjustment of Filter 15

Adjust L72, L73, C156 as follows:

f = 11 MHz, V into ST6.a4 = +6 V $\pm$0.2 V
f = 15 MHz, V into ST6.a4 = +13.75 V $\pm$0.3 V   r < 10%
f = 19 MHz, V into ST6.a4 = +26 V $\pm$0.3 V

6-dB bandwidth of filters 15 and 16 .... < 6 MHz
Attenuation at $f_u/2$ .... > 18 dB

5.3.1.8.3 Adjustment of Filter 16

Adjust L78, L79, C162, C164 for minimum reflection coefficient of the ESH 3 over the frequency range 20 MHz to 29.9999 MHz after having adjusted filter 15 using Y6.

C164: maximum effect at f_l
C162: maximum effect at f_u.

After adjustment, fix the cores of L72, L73, L78 and L79 with the cable tie provided for this purpose and secure the coils using any type of varnish or glue that is suitable for RF applications.

5.3.1.9 Mixers 1 and 2 (Y9)

Note: The pin designations in brackets (e.g. (X7)) or the component designations in brackets (e.g. (V111)) refer to model 56 of the ESH 3. Unless otherwise stated, the adjustment procedure is identical.

5.3.1.9.1 Supply Voltages

Pin	Voltage	Current
ST1.b24	Ground	-
ST1.a22	+10 $\pm$0.1 V	approx. 10 mA
ST1.a23	+12 $\pm$0.3 V	approx. 60 mA
ST1.a24	+25 $\pm$0.1 V	approx. 25 mA
ST1.b22	-10 $\pm$0.1 V	approx. 5 mA

5.3.1.9.2 Adjustment of Input Low-pass Filter

- Connect network analyzer to ST2.
- Remove BU1.
- Connect 50-Ω termination between ST8 pins 1 and 4 (r < 2%).
  Tune L1, L2, L3, L4, L5 for reflection coefficient .... < 10%
  (over frequency range 0 to 30 MHz).

5.3.1.9.3 Adjustment of 75-MHz Amplifier

- Using R1 set operating point of T1 (V111) to .... 22 mA ±2 mA
- Feed frequency of 75 MHz into ST9/2,3 (X9/1,2) using a sweep generator.
- Connect sweep display unit to ST10/1,4 (X10/A1,2)
- Adjust C14 for maximum at f = 75 MHz.
  Required gain .... 22 dB ±2 dB
- Connect sweep display unit to ST14 (X14).
- Adjust amplifier T2, T14 and T15 (V200, V140 and V150).
- Adjust C117 for maximum at f = 75 MHz.
- Required gain .... 15 dB ±3 dB
- (The ESH 3 is supplied with the 75-MHz amplifier permanently switched on (ST10 (X13) plugged on).

5.3.1.9.4 Adjustment of Diplexer of 2nd Mixer

- Connect sweep generator to ST11.2 (X11/B) and ST12.2 (X12) (50-Ω system) and adjust L18 for maximum attenuation at 9 MHz.
- Connect sweep generator to ST11.2 (X11/B) and ST7 (X7) (50-Ω system) and adjust C31 for maximum gain at 9 MHz.

5.3.1.9.5 Adjustment of 9-MHz Amplifier

Connect a sweep generator to ST11 (2,3) (X11/B) and ST7 (X7) (50-Ω system) for the adjustment.

5.3.1.9.6 500-Hz Bandwidth

- Connect ST1.a3 (X1.A3) to ground.
- Adjust R63 for maximum gain.
- Adjust C53 for minimum ripple.
- Note gain.

5.3.1.9.7 2.4-kHz Bandwidth

- Connect ST1.a5 (X1.A5) to ground.
- Set R69 to mid-position.

- Adjust C64, C67 for minimum ripple.
- Adjust R69 for same gain as with 500-Hz bandwidth.

5.3.1.9.8 10-kHz Bandwidth

- Adjust R76 for same gain as with 500-Hz and with 2.4-kHz bandwidth.
  Gain of 9-MHz amplifier .... 27 ±1 dB

5.3.1.9.9 Adjustment of Overload Detection

- Insert BU3 and BU4. (Connect X10A to X10B and X11A to X11B)
  The 2nd oscillator (f = 66.00 MHz, level = +7 dBm ±1 dB) is connected to ST5 (X5).

5.3.1.9.9.1 Overload Detection 2

Feed 75.00-MHz signal to ST9 pins 2 and 3 (X9/B).

At a level of -22 dBm ±2 dB, the logic signal at ST1.a7 (X1.A7) should change from H to L. Adjust with R35 (increasing R35 raises the response threshold).

5.3.1.9.9.2 Overload Detection 1

Feed a signal of frequency 75 to 135 MHz into ST9 pins 2 and 3 (X9/B).

At a level of ±3 dBm ±1 dB, the logic H at ST1.a9 (X1.A9) should change to logic L. Adjust with R18 (increasing R18 raises the response threshold).

5.3.1.9.9.3 Checking the Level at ST4 (X4)

Feed +23 dBm ±1 dB (frequency range 75 to 105 MHz) into ST3.

Output level required at ST4 (X4) .... -15 dBm ±2 dB
(Adjust with R94 (R208)).

5.3.1.9.9.4 Adjustment of the 1st Mixer

(to be carried out on model 56 of ESH 3 only).

- Connect X8.A1 to X8.B2 and X9.A1 to X9.B2.
  Terminate X2 with 50 Ω.
- Feed 1st oscillator (level to +23 ±2 dBm, frequency 75 to 105 MHz) at X3.

- Connect spectrum analyzer to X14.
- Level measured at X14 at 75-MHz oscillator frequency should be <-32 dBm (Note effect of cover on soldered side).
- An adjustment is possible by bending the terminal wires 3 and 6 of transformers T4 and T6.
- Following the adjustment, pins of T4 must be affixed using yellow UHU adhesige.
- Recheck level at X14.

5.3.1.9.9.5 Checking the Level at ST6

Feed +7 dBm ±1 dB (frequency 66 MHz) into ST5.

Output level required at ST6 .... -15 dBm ±2 dB (Adjust with R96).

Check the following performance specifications of Y9 using test setups as in section 3.2:

Input reflection coefficient 10 kHz to 30 MHz	....	< 20%
Noise figure 100 kHz to 30 MHz	....	< 13 dB
Oscillator reradiation 75 MHz to 105 MHz	....	< 20 dBµV
Image frequency rejection 150 MHz to 180 MHz	....	> 90 dB
IF rejection 75 MHz	....	> 100 dB
IM rejection a_{d3} - 3rd order intercept point	....	> +20 dBm

(see specifications)

IF bandwidths 10 kHz, 2.4 kHz, 500 Hz

(see specifications)

Gain .... 35 ±1 dB

5.3.1.10 Calibration Generator (Y10)

5.3.1.10.1 Supply Voltages

Pin	Voltage/Level	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	+5.25 ±0.1 V	approx. 0/65 mA	0
ST1.a22	+10 ±0.1 V	approx. 65/6 mA	0
ST1.b22	-10 ±0.1 V	approx. 3 mA	0
ST1.a1	TTL		500 Hz
ST4	-15 dBm	-	30 kHz
ST5	-13 dBm	-	8.97 MHz
ST6	-15 dBm	-	66 MHz (±1.5 kHz)
ST3	-15 dBm	-	75 MHz to 105 MHz

5.3.1.10.2 Adjustment of Sinewave Generator

- Connect +5 V to ST1.a4.
- Connect spectrum analyzer to ST2.
- Connect voltmeter to ST1.a15.
- Adjust for maximum level on the spectrum analyzer and minimum voltage on the voltmeter at:
  9 MHz by means of C9 (C10, C20)
  75 MHz by means of C45, C52, C61, C66.

The adjustment of C61, C66 is interactive.

Level at ST2 in the frequency range 10 kHz to 30 MHz .... 80 dBµV $\pm$3 dB = -27 dBm $\pm$0.3 dB
(Variable with R84; measured with a power meter.)

Spectral purity of the output signal at ST2:
Non-harmonic spurious signals .... > 40 dB down

Check the control voltage at ST1.a15:
When tuning through the range from 10 kHz to 30 MHz, the voltage must not change abruptly and there must be no AC voltage superimposed on it.

Check by means of oscilloscope; typically .... 0.8 V to 4 V

5.3.1.10.3 Adjustment of Temperature Compensation of Sinewave Generator

The temperature compensation can be adjusted in several cold/warm cycles. For the relationship between change in level and required sense of rotation of R77 see Table 5-4.

Table 5-4

Increase in temperature causes level increase. Decrease in temperature causes level drop.	Turn R77 counterclockwise.
Increase in temperature causes level drop. Decrease in temperature causes level increase.	Turn R77 clockwise.

Permissible total change in level due to change in frequency and temperature over the range from -10 to +45°C .... < 0.5 dB

Required level at ST2 .... 80 dBµV $\pm$0.3 dB = -27 dBm $\pm$0.3 dB

over the total temperature and frequency range.

Table 5-5

Input level (measured with spectrum analyzer)

Pin	Level	Frequency
4	-15 dBm $\pm$1 dB	30 kHz
5	-13 dBm $\pm$1 dB	8.97 MHz
6	-15 dBm $\pm$1 dB	66 MHz
3	-15 dBm $\pm$1 dB	75 MHz to 105 MHz

Table 5-6

Mixer level
(measured by means of RF probe at pin 8)

Mixer	Level	Frequency
B1	0 dBm ±2 dB	8.97 MHz
B3	0 dBm ±2 dB	66 MHz
B5	0 dBm ±2 dB	75 MHz to 105 MHz

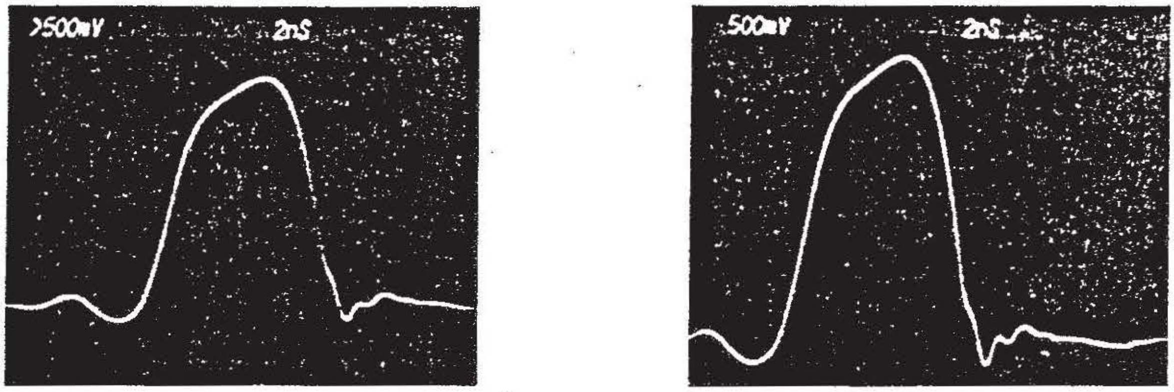
Level required at C70 (f = 10 kHz to 30 MHz, with AGC,
measured by means of high-impedance probe) .... 5 mV ±3 dB
Level at ST7 .... -67 dBm ±0.3 dB
Level variation by R110 .... ±0.7 dB

5.3.1.10.4 Checking the CISPR 3 or CISPR 1 Pulse Generator

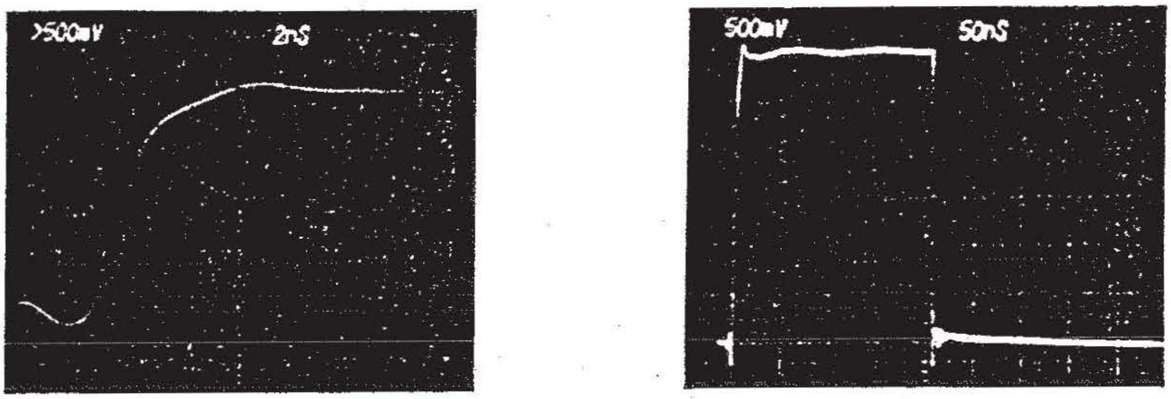
- Disconnect ST1.a4 from +5 V, and instead connect either ST1.a6 (CISPR 3) or a5 (CISPR 1) to +5 V.
- Check pulse at ST7, terminated with 50 Ω, by means of a 1-GHz oscilloscope:

Table 5-7

	Logic H to ST1	PRF	Pulse energy µVs (EMF) ±10%	Adjust with
CISPR 3	a6	25 Hz	1.35	R89
CISPR 1	a5	100 Hz	0.0316	R91



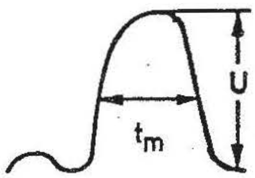
Rise time $t_r = 3$ ns
a) with CISPR 1 pulse



Rise time $t_r = 4$ ns
b) with CISPR 3 pulse

Fig. 5-5 Pulse calibration

For a rough measurement, the pulse energy can be graphically integrated or calculated according to the following simplification:



Pulse area = V • $t_{50\%}$

Accordingly, with CISPR 1 pulse (Fig. 5-5a),
the pulse area = 2.8 (V) • 5.6 (ns) = 0.01568 µVs

corresponding to an EMF pulse energy of 0.03136 µVs.

This calibration pulse of the ESH 3 is 20 dB below the CISPR 1 standard pulse.

Fig. 5-5b: CISPR 3 pulse

$V \cdot t_{50\%} = 3(V) \cdot 210(ns) = 0.63\ \mu Vs$

$V \cdot t_{50\%} = 1.26\ \mu Vs$ (EMF pulse area)

Hence, this calibration pulse is 20 dB below the CISPR 3 standard pulse (13.5 µVs).

5.3.1.11 Mixer 3 (Y11)

5.3.1.11.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	-5.25 ±0.1 V	approx. 12 mA	0
ST1.a22	+10 V ±0.1 V	approx. 48 mA	0
ST1.b22	-10 V ±0.1 V	approx. 18 mA	0
ST1.b1	TTL	-	500 Hz

5.3.1.11.2 Adjustment of 8.97-MHz Oscillator

- Apply exact 500-Hz reference to ST1.b1 (TTL level squarewave; for repair purposes, use ESH 3 reference)
- Measure control voltage $V_{control}$ at R40/R41
  Adjust C43 so that $V_{control}$ .... 5 V ±1V
  (If adjustment is not possible, vary L11 slightly)
- Measure output level on ST3 .... -13 dBm ±2 dB
- Measure oscillator frequency at ST3 .... 8.97 MHz
  (The accuracy of the measured value depends on the accuracy of the reference used.)
- Check synchronization indication at ST1.b2: logic H (loop is synchronized).

5.3.1.11.3 Adjustment of Basic Gain between ST2 and ST5

a) Initial settings:

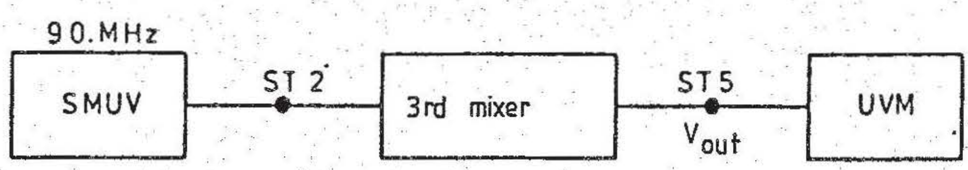
- Settings on the ESH 3:
  IF bandwidth <u>5</u>: 500 Hz to 10 kHz (ST1.a11 = L)
  IF attenuation <u>40</u>, <u>41</u>: 40 dB

- Connect ST1.b12 to +10 V.
- Apply external DC voltage of -5 to +10 V to ST1.a12.
- Set external DC voltage to ≧ 4 V (= maximum gain).

  V_{EMF} at ST2 with f = 9.000 MHz = 20 mV.

  Measure at ST5 via a high impedance using a millivoltmeter.

Test setup:



b) Adjustment

Set output voltage V_{out} by means of R20.

V_{out} .... 200 mV

5.3.1.11.4 Checking the Noise Filter Bandwidth

Measure between ST2 and ST5 with any IF bandwidth other than 0.2 kHz (ST1.a11 = L). Vary the signal-generator frequency to determine the upper and lower 1-dB and 3-dB cut-off frequencies of the noise filter.

Table 5-8

	$f_{cut\text{-}off\ lower}$/kHz	$f_{cut\text{-}off\ upper}$/kHz
1-dB cut-off frequencies	25 ±1	35 ±1
3-dB cut-off frequencies	23 ±1	37 ±1

The pass-band characteristic should be approximately flat and must not exhibit a dip.

5.3.1.11.5 Checking the Calibration Gain Control Range

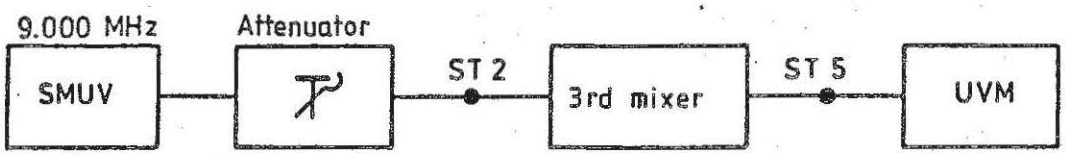
- Apply +10 V to ST1.b12 (calibration = ON).
- Feed DC voltage $V_{control}$ into ST1.a12.
- Vary the voltage at the base of T1 from 0 to +5 V.

- The gain between ST2 and ST5 should be variable between about -15 dB and 0 dB referred to maximum gain G_{max}.

  When the voltage at the base of T1 is 2 V, the gain is typically 6 dB below G_{max}.

5.3.1.11.6 Checking the IF Attenuation Steps

Test setup:



Use as accurate an attenuator as possible, such as the DPVP.

- Set $V_{control\ CAL}$ at the base of T1 again to about 2.0 V.
- Set the attenuator to 50 dB.
- Set the IF attenuation of the 3rd mixer to 0 dB (= maximum gain).
- Adjust signal generator level such that the millivoltmeter gives a deflection approximately 2 dB < 100 mV (near the 0-dB marker).
- Increase the IF attenuation of the 3rd mixer in steps of 10 dB and reduce the attenuator setting in steps of 10 dB.
- Observe deflection on millivoltmeter: The difference (= attenuation error) should be less than 0.1 dB. The sum of the attenuation errors should be approximately 0 dB.

5.3.1.11.7 Checking the IF Output Amplifier

Use the same test setup as in section 5.3.1.11.5 but measure at ST4.

- All inputs ST1.b7 to b10 = logic L.
- Adjust signal generator level so that the pointer of the millivoltmeter is on 2.0 V.
- Apply logic H to ST1.b8 and reduce the attenuator setting by 20 dB.
  Difference in pointer deflection .... $\leq$ 1 dB

- Apply logic H to ST1.b7 and reduce the attenuator setting by further 20 dB. Difference in pointer deflection .... $\leqq$ 1 dB

5.3.1.11.8 Checking the 200-Hz Bandwidth and Adjustment of Gain

- ST1.a11 = logic H (200-Hz filter ON).
- Vary the signal generator frequency between the lower and the upper 6-dB cut-off frequency.

  $B_{6\ dB}$ .... 200 Hz $^{+20\ Hz}_{-30\ Hz}$

- Tune to the maximum in the pass-band curve.
- Switch over to noise filter:
  Note readout on millivoltmeter.
- Switch back to 200-Hz filter:
  Adjust for same readout on millivoltmeter by means of R102.

5.3.1.11.9 Checking the Overload Detection

Settings on the ESH 3:
IF bandwidth 5: 500 Hz to 10 kHz (ST1.a11 = logic L)
IF attenuation 40, 41: 0 dB.

ST1.b11 = logic L if EMF at ST2 .... 20 mV

5.3.1.12 Indication and AF Demodulation Board (Y12)

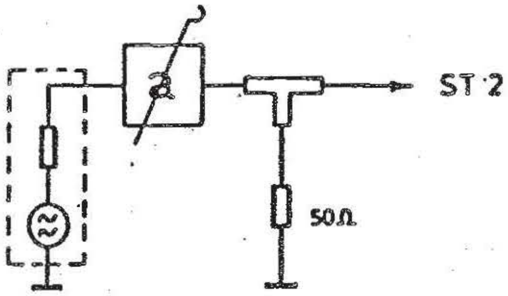
5.3.1.12.1 Supply Voltages

Pin	Voltage	Current	Frequency
ST1.b24	Ground	-	-
ST1.b23	+5.25 V ±0.1 V	approx. 1 mA	-
ST1.a22	+10 V ±0.1 V	approx. 100 mA	-
ST1.b22	-10 V ±0.1 V	approx. 55 mA	-
ST1.ab1	TTL	-	500 Hz

5.3.1.12.2 Adjustment of Indication Section

Test setup:

Connect 30-kHz signal generator via attenuator to ST2. As ST2 is a high-impedance input, use a 50-Ω termination in parallel.



a) Linearity of B14:

Settings on the ESH 3: Operating range 33: 20 dB

- DVM check point: pin 6 of B14.
- Input voltage 20 mV; note reading (e.g. 210 mV).
- Input voltage 2 mV; vary R164 until 1/10 of the above measured value is obtained (e.g. 21 mV ±0.5 mV).
- Repeat adjustment to ensure optimum voltage setting.

b) Linearity of B15:

Settings on the ESH 3: Operating range 33: 20 dB

- DVM check point: pin 2 of B15.
- Input voltage 20 mV; note reading (e.g. 210 mV).
- Input voltage 2 mV; vary R174 until 1/10 of the above measured value is obtained (e.g. 21 mV ±0.5 mV).
- Repeat adjustment to ensure optimum voltage setting.

c) Average-value indication:

Settings on the ESH 3: Operating range 33: 20 dB
35: AV.

- DVM check point ST1.a2.
- Input voltage 20 mV; vary R182 until the DVM reads ...... 2 V ±5 mV
- Input voltage 2 mV; vary R177 until the DVM reads .... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

d) CISPR indication:

Settings on the ESH 3: 35: CISPR
Frequency between 10 kHz and 149.9 kHz (CISPR 3).

- DVM check point: ST1.a2.
- Input voltage 20 mV; vary R198 until the DVM reads ...... 2 V ±5 mV
- Input voltage 2 mV; vary R195 until the DVM reads .... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

e) LOG 40:

Settings on the ESH 3: Operating range 33: 40 dB
35: AV

- DVM check point: ST1.a2.
- Input voltage 200 mV; vary R139 until the DVM reads ..... 2 V ±5 mV
- Input voltage 2 mV; vary R186 until the DVM reads .... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

f) LOG 60:

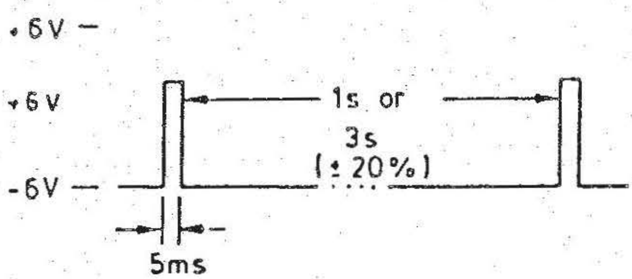
Settings on the ESH 3: Operating range 33: 60 dB
35: AV

- DVM check point: ST1.a2.
- Input voltage 2 V; vary R142 until the DVM reads .... 2 V ±5 mV
- Input voltage 2 mV; vary R188 until the DVM reads .... 0.2 V ±5 mV
- Repeat adjustment to ensure optimum voltage setting.

g) Peak-reading time constants:
(With the ESH 3, determined by PEAK and the measuring time)

Settings on the ESH 3: Operating mode 38: GEN. OFF

Oscilloscope check point: B20 pin 10



h) 4th oscillator:

Feed TTL-level reference frequency of 500 Hz into ST1.ab1. Connect frequency counter to B33/2.

Table 5-9

Switch position		Nominal frequency	
A0	GEN.OFF	30.0 kHz	(±10 Hz)
A1	GEN.OFF	31.0 kHz	(±10 Hz)
USB	GEN.OFF	31.5 kHz	(±10 Hz)
LSB	GEN.OFF	28.5 kHz	(±10 Hz)
ANY	GEN.ON	30.0 kHz	(±10 Hz)

Same as above, but connect oscilloscope to ST5 instead of frequency counter.

Settings on the ESH 3: Operating mode 38: GEN.ON

Nominal level 40 mV_{rms} = 110 mV_{pp} = 15 dBm ±1 dB into 50 Ω

i) Remote frequency measurement (RFM):

- Connect a signal generator variable between 25 and 35 kHz, approx. 20 mV, to ST2.
- Select REM. FREQ. mode.
- Counter connected to ST5 should read out signal generator frequency.
- Measure nominal level at ST5 by means of oscilloscope:
  40 mV_{rms} = 110 mV_{pp} = 15 dBm (±1 dB) into 50 Ω.

5.3.1.12.3 AF Demodulation

a) FM demodulation:

Oscillator adjustment:

- Connect signal generator to ST2: 30 kHz, approx. 20 mV
- DVM check point: ST1.a4
- Vary R19 until the DVM reads 0 V (±20 mV).

Checking the FM demodulation

- Connect signal generator and DVM as for oscillator adjustment.

Table 5-10

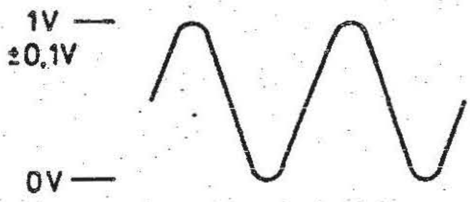
Signal generator frequency	Nominal voltage reading on DVM
25 kHz	-5 V ±0.3 V
27 kHz	-3 V ±0.3 V
29 kHz	-1 V ±0.3 V
31 kHz	1 V ±0.3 V
33 kHz	3 V ±0.3 V
35 kHz	5 V ±0.3 V

b) AM demodulation:

Settings on the ESH 3: AF demodulation 4: A3
Operating mode 38: GEN.OFF

Connect signal generator to ST2 (frequency 30 kHz, level approx. 100 mV, 100% modulation depth).

Oscilloscope check point ST4:



Vary the input voltage between 2 mV and 2 V. The voltage change at ST4 should be < 3 dB.

c) SSB demodulation:

Settings on the ESH 3: AF demodulation 4: A1
Operating mode 38: GEN.OFF
35: AV

Connect signal generator to ST2 (frequency 30 kHz, level approx. 20 mV, unmodulated).

Oscilloscope check point ST1.a3:
Nominal signal 1 kHz AF, approx. 130 mV_{rms} = 360 mV peak-to-peak (±50%).

d) SSB AGC:

Settings on the ESH 3 as for SSB demodulation, but the level at ST2 is about 100 mV.

Switch off the signal generator. It should take approximately 1 s until the AGC voltage at B8 pin 9 drops.

5.3.1.13 Performance Check of the Indication and AF Demodulation Board Y12

5.3.1.13.1 Indication Demodulation

a) Average-value indication:

Feed unmodulated 30-kHz signal V to ST2. The resulting voltages at ST1.a2 are as follows:

Table 5-11

V to ST2	Operating range		
	20 dB	40 dB	60 dB
2 mV	200 ±10 mV	200 ±20 mV	200 ±20 mV
6.3 mV	630 ±20 mV	650 ±40 mV	500 ±40 mV
20 mV	2000 ±10 mV	1100 ±40 mV	800 ±40 mV
63 mV		1550 ±40 mV	1100 ±40 mV
200 mV		2000 ±20 mV	1400 ±40 mV
632 mV			1700 ±40 mV
2000 mV			2000 ±20 mV

Amplitude-modulated signals cannot be directly measured in the 40-dB and 60-dB operating ranges. Use correction curve (Fig. 2-8).

b) Peak-value indication:

If an unmodulated input signal is applied, the same voltage is obtained at ST1.a2 as with average-value indication. A 100% amplitude-modulated signal increases the indicated value by 6 dB as against average-value indication.

c) CISPR indication:

In the frequency range from 10 kHz to 150 kHz, the signal is weighted in accordance with CISPR 3 and from 150 kHz to 30 MHz in accordance with CISPR 1. If unmodulated signals are applied to ST2, the following voltages are obtained at ST1.a2:

Table 5-12

	CISPR 1	CISPR 3
2 mV 10 mV 20 mV	217 ±10 mV 680 ±20 mV 2170 ±10 mV	200 ±10 mV 630 ±20 mV 2000 ±10 mV
Pulse weighting time constants:		
	CISPR 1	CISPR 3
Charging time constant	1 ms	45 ms
Discharging time constant	160 ms	500 ms

5.3.1.13.2 AF Demodulation

a) Demodulation outputs:

- AF output ST1.a3
  Apply 100% amplitude-modulated, or frequency-modulated (frequency deviation 5 kHz), input signal.
  AF output signal .... 200 mV_{rms} +50 mV (Z_{out} = 5 kΩ)
- AM output ST4
  This output is used for measuring the modulation depth by means of an oscilloscope: 100% modulation depth corresponds to 1 V_{pp} ±3 dB (Z_{out} = 1 kΩ).
- FM output ST3
  At this output, the frequency offset of the 30-kHz input signal can be measured:
  5 kHz deviation corresponds to ±0.5 V (tolerance 0.03 V) (Z_{out} = 10 kΩ).
- Frequency offset output ST1.a4
  Here too, the frequency offset of the 30-kHz input signal can be measured: ±5 kHz offset corresponds to ±5 V (tolerance 0.3 V) (Z_{out} = 10 kΩ).

b) IF amplifier AGC

AM AGC time constant 0.5 s

AO AGC time constant 0.5 s

A1 hang AGC with fast decay

USB hang AGC

LSB hang AGC

c) 4th oscillator

Demodulation mode	Signal generator	Frequency of 4th oscillator
AM	OFF	switched off
FM	OFF	switched off
AO	OFF	30.0 kHz
A1	OFF	31.0 kHz
USB	OFF	31.5 kHz
LSB	OFF	28.5 kHz
any	ON	30.0 kHz

d) 30-kHz output ST5

With 30 kHz ON (GEN.ON), the frequency of the output signal is 30.0 kHz. In the REM. FREQ. (remote frequency measurement) mode, the output signal is synchronized with the input signal at ST2.

Level in both cases .... 40 mV ±1 dB into 50 Ω

5.3.1.14 Attenuator Control (Y13)

5.3.1.14.1 Supply Voltages

Pin	Voltage	Current
ST3.ab2	Ground	-
ST3.ab1	+12 V ±0.1 V	approx. 2 A

The Attenuator Control (Y13) is preferably checked together with the RF Attenuator (Y16).

For production testing, it is advisable to use a control arrangement that permits the control levels at ST1.a2 to 16 to be switched on as desired. For checking the gating with B1 to B4 at the test points B to K, refer to Table 5-13.

(The attenuation values a are obtained by summing the attenuation values defined by the logic H signals at the control inputs of ST1.)

Table 5-13

Test point	B	C	D	E	F	H	I	K
Attenuator/dB	10	20	40	40	10	20	CAL	1
Attenuation a/dB								
0	L	L	L	L	L	L	L	L
10	H	L	L	L	L	L	L	L
20	L	H	L	L	L	L	L	L
30	H	H	L	L	L	L	L	L
40	L	L	H	L	L	L	L	L
50	H	L	H	L	L	L	L	L
60	L	H	H	L	L	L	L	L
70	H	H	H	L	L	L	L	L
80	L	L	H	H	L	L	L	L
90	H	L	H	H	L	L	L	L
100	L	H	H	H	L	L	L	L
110	H	H	H	H	L	L	L	L
120	H	H	H	H	H	L	L	L
130	H	H	H	H	L	H	L	L
140	H	H	H	H	H	H	L	L
CAL	H	L	H	H	X	X	H	X
1	X	X	X	X	X	X	X*)	H

*) No effect, i.e. the last setting is preserved.

It is possible to set attenuation values up to 140 dB in the ESH 3. If, when the ESH 3 is being repaired, there is any doubt as to the proper functioning of the Attenuator Control, it is recommended that the RF Attenuator be removed from the ESH 3, the base plate unscrewed and the functioning of the control be checked by observing the switching state of the contacts (for location of the attenuators, see circuit diagram 303.2813 S). An error can be tracked down with the aid of section 4.1.11.

5.3.1.15 Power Supply

5.3.1.15.1 Access to Circuits

For troubleshooting, the instrument may be operated with the power supply swung out. For this the instrument panelling is first removed. After then removing six screws on the frame, the power supply can be withdrawn horizontally. After the actuating rod of the power switch is pulled off, the power supply can be placed toward the back on the cooling body.

Note! In dismounting the power supply, only the six outermost screws may be removed, since otherwise other parts of the power supply will be loosened.

In remounting the power supply in the instrument, the flat cable must be correctly folded and the actuating rod of the power switch replaced before the power supply is moved into place and screwed to the frame.

The individual subassemblies of the power supply are best tested while connected into the instrument circuit, since all supply and control lines are then attached. The subassemblies can be swivelled apart to permit access to the components. So long as the power supply is operated for only short periods or is only partially loaded, the large heat sinks can be removed.

After the heat sinks of the analog power supply have been unscrewed, all components and test points are accessible. The solder side of the subassembly is accessible after the latter has been unscrewed. The removed subassembly must be supported in a suitable fixture to assure that no shortcircuits are possible.

For measurements on the solder side of the switching power supply board, the cover on the side of the analog power supply must be unscrewed.
The analog board remains attached to the cover. For replacement of components in the switching power supply, the board is not removed, instead the entire frame is unscrewed from the rear panel. For this the two large screws on the rear side in the cooling fins and then the six small screws in the frame be removed. The frame can then be swivelled away without having to remove the leads to the rear panel. The rectifier plate must remain in place for operation of the system.

Before reassembly, the correct seating of the socket strip on X30 and the lines on the lead-through filters must be checked. The heat sink on the switching power supply must be provided with heat-conducting paste. Then the frame screws and screws in the cooling fins are loosely screwed in. After lining up the unit the frame is first tightened and then the internal heat sink.

Note! If the internal heat sink is not tightly screwed down, the switching power supply will overheat in operation.

5.3.1.15.2 Adjustment of Reference Voltages

The only adjustment points of the power supply are potentiometers R89 and R95 on the analog power supply board, with which the monitoring and regulator reference voltages can be set.

Note! This adjustment should only be undertaken if really necessary, since other circuits will then also have to be adjusted.

Reference point for all accurate voltage measurements is the ground neutral point X5 on the rectifier board. The adjustment is made by measuring the +10-V supply voltage at a point of the sensing line (motherboard X201A4) and accurately setting it with R95. If the accessories are available, the +10-V supply can also be adjusted by measuring this voltage on the sensing line at points X18.16 or X36.1 of the analog power supply board. After this adjustment, the regulator reference voltage, measurable on test connector X9.1, must have the value +8 V ±20 mV. The monitoring reference voltage at X9.3 must be set to exactly the same value by means of R89.

The other output voltages are determined by fixed resistors and cannot be separately adjusted. The -10-V supply at sensing point X201B4 on the motherboard tracks the +10-V supply with a maximum error of 10 mV. All other voltages must lie within a tolerance limit of ±2% at the power supply. It must be noted that because of voltage drops in the lines, the output of the +5-V supply is 5.5 V at its output terminals. The output voltage of the +30-V supply lies between 31 V and 40 V depending on the loading of the -11-V supply. When the -11-V supply is not loaded, the output of the +30-V supply can drop so low that the H3 LED lights. This is of no significance in normal operation.

5.3.1.15.3 Test Points of Analog Power Supply

The analog power supply has a variety of connectors, some of which are bridged with shorting links.

X31 to X38	.1-.2	connected (comparator inputs)
X5	.2-.3	connected (short-circuit link right)
X9,X10		open
X2,X4,X8,X12	.1-.2	connected for setting 20 V (short-circuit top, ESVP)
	.2-.3	connected for setting 25 V (short-circuit bottom, ESH3)

5.3.1.15.4 Check of Output Currents

In table 5-2 are listed the maximum output currents of the power supply - these may, however, not be drawn in operation. The measured current values must lie within the tolerance range of -10% to +25%.

Table 5-14a Output Currents

Voltage (nominal)	Maximum current cold	warm	Shortcircuit current
+5 V	7 A	6 A	6 A
+12 V	4 A	3 A	3 A
-11 V	1.4 A	1.2 A	1.2 A
+33 V	0.5 A	Can only be overloaded for short period.	
+10 V	0.7 A		0.15 A
-10 V	1.3 A		0.33 A
+20 V (ESVP)	0.4 A		0.08 A
+25 V (ESH3)	0.05 A		0.01 A
+30 V	0.06 A		0.06 A

The check on analog supplies with foldback current limiting can only be made with resistors of corresponding power rating. The switching supplies can also be checked with electronic current sinks.

The sensing leads for the +10-V and -10-V supplies must be connected to the proper outputs. If these leads are not connected, the supply voltages will be about 0.3 V too high, although the voltages on the comparators are correct.

5.3.1.15.5 Check of Monitoring Circuit

When the shorting links are removed from X31 to X38, the corresponding LEDs H1 to H8 light. By applying a variable voltage to the pins .2, the limit values of the monitoring windows can be determined. The actual supply voltages can be measured at the same time on pins .1.

Note! The test with X31 may only be made if the internal supply is operating properly, since otherwise the other supplies can be switched into prohibited states.

Because of the interlocking of some of the power supplies, only one external voltage at a time must be applied and the corresponding LED observed. In case of automatic measurement the error messages are monitored at the outputs of these messages and on S1, S2, S3.

Table 5-14b Monitoring Window Data

Connector	LED	Nominal voltage	Lower limit	Upper limit	Max. shift of window
X31	H1	15 V	12.8 V	18 V No mess.	300 mV
X32	H2	24 V	↓20.8 V ↑21.3 V	40 V No mess.	400 mV
X33	H3	30 V	28.8 V	31.4 V	600 mV
X34	H4	25V (ESH3)	23.9 V	26.1 V	500 mV
X34	H4	20V (ESVP)	19.1 V	20.9 V	400 mV
X35	H5	12 V	11.4 V	12.5 V	200 mV
X36	H6	10 V	9.9 V	10.1 V	20 mV
X37	H7	-10 V	-9.9 V	-10.1 V	20 mV
X38	H8	5 V	5.1 V	5.6 V	50 mV

Table 5-14c Message Output Levels

Connector	Nominal voltage	LED	Output on	Pin	Level O.K.	Level Error	Other responses in case of error
X31	15 V	H1	S1	X18.23	0 V	>0.8 V	All the others
X32	24 V	H2	S3	X18.25	0 V	>0.8 V	All except S1,S2,12K
X33	30 V	H3	30 comp.	X14.15	high	low	-
X34	20/25 V	H4	20 comp.	X14.18	high	low	-
X35	12 V	H5	12 comp.	X14.17	high	low	-
X36	10 V	H6	10 comp.	X14.9	high	low	-
X37	-10 V	H7	-10 comp.	X14.16	high	low	-
X38	5 V	H8	S2	X18.26	0 V	>0.8 V	All except S1

The ERROR INT, TRAP and RESET outputs can be monitored simultaneously.
If all voltages are in order, ERROR INT and TRAP are low and RESET is high.

ERROR INT goes high at every error.

TRAP is high during the on-time of D4I (about 100 ms) if S3 responds.

RESET goes low when S2 responds or after TRAP has gone back to low.
RESET then goes high again only after monostable D4II, having been triggered by the negative edge of ERR INT, returns to its off-state.

The output of the 5-V comparator and of monostable D4II can be monitored on X10.

5.3.1.15.6 Notes on Troubleshooting

If the green LED in the power supply does not light, the microprocessor is blocked (by an ERROR message or RESET). The fault can be localized with help of the description for the monitoring circuit in Section 5.1.4. In any case, before any repair is attempted, it should be determined whether the error is the result of external influence (undervoltage, overload).

No LED is lit

If after instrument switch-on no LED in the power supply lights, the cause quite likely is that there is no input to the analog power supply. After check of the AC supply or battery voltage and the fuses accessible on the rear panel, the voltage on capacitor C5 of the rectifier board should be checked with the AC power supply on. Flat connectors X1 and X2 are accessible from the underside of the instrument after the panelling is removed. If a voltage is present, the power supply should be removed from the instrument and the connection to the analog power supply checked. The input voltage should also be present on regulator N5.1 of the analog power supply.

One or more red LEDs lit

The rank order of the error messages as shown in Fig. 5-2 must be observed, i.e. the higher ranking signal must be checked first. If the green LED lights when the load on the power supply is reduced or completely removed, the output currents should be checked against the values in Section 5.2.4.

Before attempting any repairs, the voltages in question and the reference voltages should be checked to eliminate the possibility of a fault in the monitoring circuit. Before opening the switching power supply, the turn-off signals S1, S2, S3 (accessible on connector X17 of the rectifier board) should be checked. If a voltage > 0.8 V is present, the corresponding switching supply is turned off.

After unscrewing the cover of the power supply, the voltages on connector X30 should be checked, in order to eliminate the possibility of a break in the connection between the switching power supply and the rectifier board.
In this condition the signals on all components of the switching power supply can be checked.

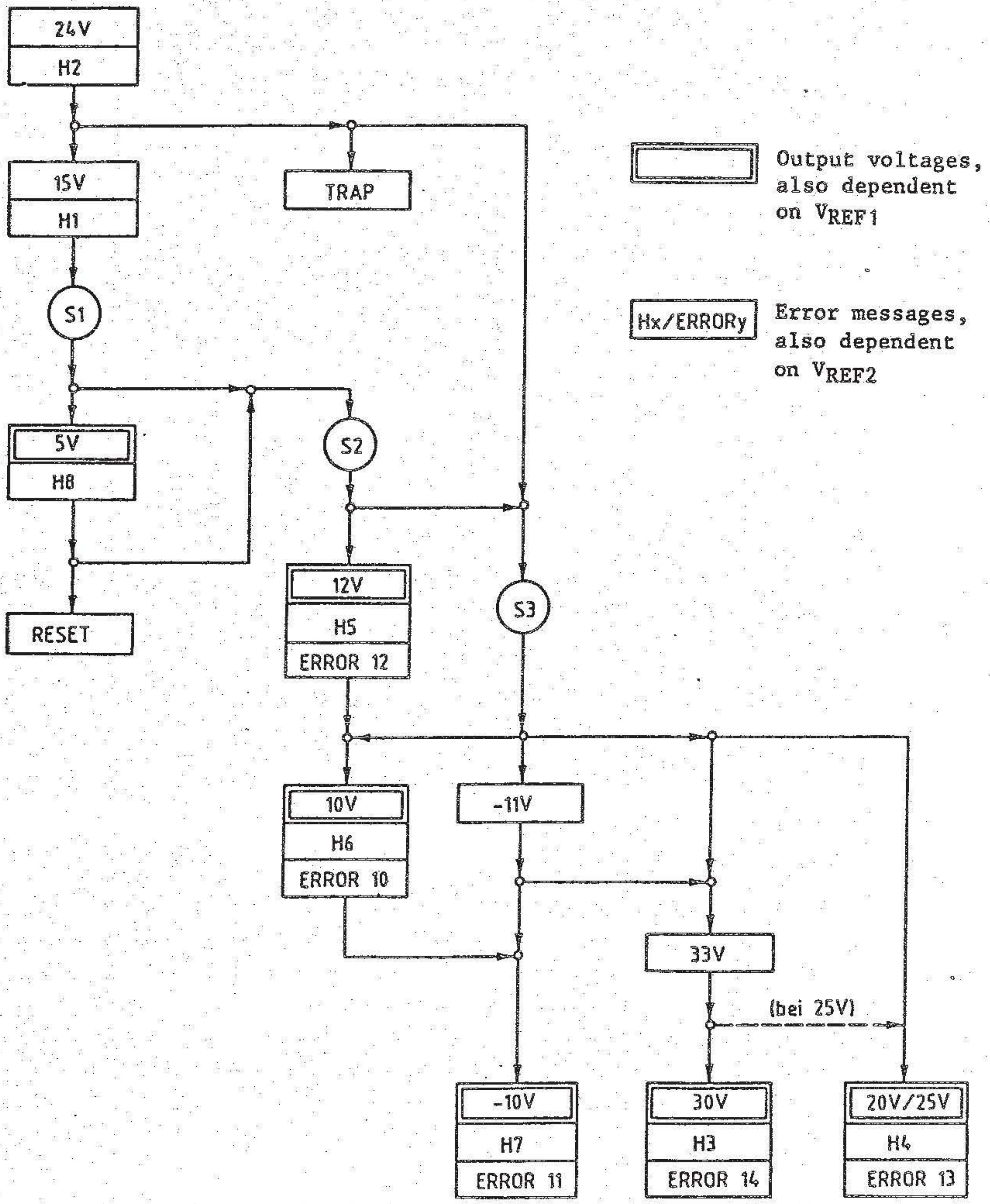


Fig. 5-6 Rank order of supply voltages and error messages

5.3.1.16 Checking the Recorder Control Board

(See circuit diagram 335.9913 S)

5.3.1.16.1 IEC-bus Section

- The IEC bus is simply connected via a flat cable (ST8) from the Computer board (BU8) to the recorder control board. For checking, unplug ST8 and use a continuity tester.

  NOTE: If the recorder control board has to be removed, protect the pins of plugs 7 and 8 against damage by sticking them in pieces of foam plastic.
- Pull out ST7 from BU7.
- Connect logic tester probe (or voltmeter) to ST7 pin 1.
- Switch on receiver and apply +5 V. Check function of the address line (a1).
- Change connections and check a2 to a5 and ton similarly.
- Connect logic tester probe or voltmeter to ST7 pin 7.
- If BU1 pin 1 is shortcircuited to ground, ST7 pin 7 should be at logic L (< 0.8 V).
- Check ST7 pin 8 with BU2 pin 2 to ground, as above.
- Check the remaining pins of ST7, by means of a continuity tester, against the circuit diagram.

5.3.1.16.2 Checking the Demultiplexer

- Unplug ST7.
- Switch on the ESH 3.
- Apply a stable voltage V = 0 to 10 V (e.g. 5 V) to B6 pin 5.
- Deliver logic L to ST7 pin 13 (penlift signal).
- Check in accordance with Table 5-15:

Table 5-15

Recorder	ST7 pin			BU2 pin					BU2 pin +)				
	12	11	10	8	9	10	11	12	10	21	22	23	24
1	H	L	L	V_{in}	X	X	X	X	L	H	H	H	H
2	L	H	L	X	V_{in}	X	X	X	H	L	H	H	H
3	H	H	L	X	X	V_{in}	X	X	H	H	L	H	H
4	L	L	H	X	X	X	V_{in}	X	H	H	H	L	H
5	H	L	H	X	X	X	X	V_{in}	H	H	H	H	L
0.6 to 8	Recorders not active								+) only for penlift				

5.3.1.16.3 Checking the External Reference Switchover

- Check the following levels using a voltmeter or logic tester probe:

Synthesizer 2/pin	Int. ref.	Ext. 5 MHz	Ext. 10 MHz
ST1/a2	L	H	L
ST1/b2	L	L	H

- Check the pulling range of the synthesizer in accordance with 5.3.1.3.4.3.

5.3.1.17 Motherboard (Y18)

Check the Motherboard in accordance with circuit diagram 303.2020 S.

5.3.1.18 RF Attenuator (Y16)

It is recommended that the RF attenuator Y16 be checked together with the attenuator control Y13.

Note: Torque range for SMA socket: 80 to 120 Ncm

- Screw down the six adjustment screws of the base plate all the way.

a) Check the residual attenuation with DC voltage.

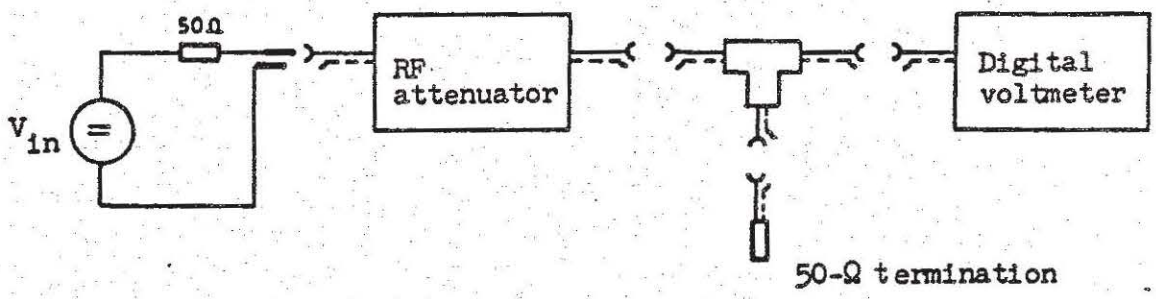
   - Set the level switch to 0 dB.
   - Measure the resistance between the inner conductor of the input and the inner conductor of the output by means of an ohmmeter with a resolution of 100 mΩ.
   - The resistance consists of the contact resistances of the 18 switching contacts and the series resistances of the thin-film conductors. The resistance of the test setup must be taken into account. The resistance R_T should be $\leqq$ 800 mΩ. The resulting residual attenuation a_0 is given by the formula

     $$a_0 = 20 \log \frac{100}{100+R_T/\Omega}$$ and is < 0.07 dB.

   - Then measure the resistance between the inner conductor of the calibration input and the inner conductor of the output. To do so, apply a short switching pulse across the coil of solenoid 7 which initiates calibration of the RF attenuator without switching the 10-dB attenuator pad into circuit. The resistance should be < 500 mΩ.

b) Checking the attenuator pads with a DC voltage

Test setup:



- Connect a constant DC voltage source $V \leq 5$ V with an internal resistance of 50Ω to the input of the RF attenuator.
- Measure the output voltage of the through-connected (0 dB) attenuator by means of a digital voltmeter. The attenuator is terminated with 50Ω.
- Successively set the attenuation values a = 1, 4, 10, 20 and 40 dB. The attenuator control cannot be used for this purpose; instead, short 12-V switching pulses must be applied directly to the terminals accessible on the control board. Open the connection to the attenuator control.

The attenuation actually provided can be calculated from the voltage ratios:

$$a = 20 \log \frac{V\ (0\ dB)}{V\ (a\ dB)} .$$

The maximum permissible attenuation error can be read off the below table:

Attenuator pad/dB	a_{min}/dB	Actual/dB	a_{max}/dB
1	0.98		1.02
4	3.98		4.02
10 (1)	9.96		10.04
10 (2)	9.96		10.04
20 (1)	19.94		20.06
20 (2)	19.94		20.06
40 (1)	39.92		40.08
40 (2)	39.92		40.08

The location of the individual attenuator pads is shown in circuit diagram 303.2813 S.

Since the RF attenuator is used only up to 30 MHz in the ESH2 even though it is designed for frequencies up to 2.7 GHz, there is no need for an RF check (VSWR < 1.2 at input and output in the range 0 to 1000 MHz).

5.3.2 Overall Adjustment

Prerequisites for the adjustment:

- All assemblies must be operational and adjusted as required.
- Remove Filter 2 (Y8), open it and connect it to the receiver via the Service Adapter.

5.3.2.1 Checking the Supply Voltages

Motherboard b23	+5.4 V ±250 mV
Motherboard a22	+10.000 V ±200 mV
Motherboard a23	+12 V ±500 mV
Motherboard a24	+25 V ±130 mV
Filter Control Y6, a24	+30 V ±1.35 V
Motherboard b22	−10 V ±400 mV

5.3.2.2 Checking the Gain of Mixers 1 + 2 (Y9) and Mixer 3 (Y11)

Settings on the ESH 3:		39: LIN.
	Indicating mode	35: AV.
	IF bandwidth	6: 500 Hz
	IF attenuation	40, 41: 40 dB
	RF attenuation	40, 41: 50 dB

Connect signal generator (f < 10 MHz, level 80 dBµV ±0.1 dB, 50 Ω) to the RF input 45 of the ESH 3. Adjust the gain by means of R20 on Y11 so that at a medium gain setting (+2 V ±0.2 V) at the base of T1 (Y11) full-scale deflection is obtained.

5.3.2.3 Checking for Equal Gain with the Various Bandwidths

Settings on the ESH 3: See section 5.3.2.4

Permissible difference in the indicated voltage when selecting a new bandwidth .... ±1 dB

Reference: 500-Hz bandwidth

Adjust the gain with

200-Hz bandwidth: on Y11 using R102
2.4-kHz bandwidth: on Y9 using R69
10-kHz bandwidth: on Y9 using R76.

5.3.2.4 Adjusting Filters 15 and 16 (Y8)

Connect the input of the receiver to a VSWR meter which can be driven from the GEN. output of the ESH 3.

a) Adjusting filter 15 for minimum reflection coefficient

Table 5-16

f	by means of R... on Y6
10.0 MHz	79
11.0 MHz	55
15.0 MHz	70
19.0 MHz	89
19.9 MHz	103

Repeat this adjustment at least once, since the settings interact.

b) Adjusting filter 16 for minimum reflection coefficient

Adjust L78, L79, C162 and C164 in the frequency range from 20.0 MHz to 29.9 MHz.

After the adjustment fasten the coils and secure the windings with a suitable varnish or glue. The board can now have the cover fitted and be inserted in the unit.

Checking the input impedance:
Filters 1 to 14: at least three readings per filter range
Filters 15 and 16: at least every 2 MHz.
VSWR with 0 dB RF attenuation .... ≦ 2 = < 33%
with RF attenuation > 0 dB .... ≦ 1.2 = < 10%

5.3.2.5 Checking the Reference Frequency

Tune the receiver to 29.0000 MHz. Switch on the generator and connect to a frequency counter with a frequency accuracy of better than 1×10^{-8}. After a warm-up period of > 5 min, adjust the counter display to 29.0000 MHz by means of R22 on Y1.

5.3.2.6 Adjustment of Calibration

a) Sinewave calibration

Settings on the ESH 3:

Indicating mode		35:	AV.
Operating range		33:	20 dB
IF bandwidth		6:	10 kHz
RF attenuation	40,	41:	50 dB
IF attenuation	40,	41:	40 dB
Frequency		20:	1 MHz
Operating mode		38:	TWOPORT
Meas. time		37:	≥ 0.1 s

Connect suitable precision level meter (50 Ω), such as specially calibrated URV 4 with 50-Ω insertion unit, to the GEN. output 44.

- Set level by means of R84 on Y10.
  Required level .... 80 dBμV ±0.1 dB
  = -27 dBm ±0.1 dB
- Press CAL. button 15 momentarily (calibration check).
- Connect the GEN. output 44 to the RF input 45.
  Required indication .... 0 dB ±0.1 dB

b) Pulse calibration (CISPR 3)
over frequency range 10 kHz to 149.9 kHz

Settings on the ESH 3:

Indicating mode		35:	CISPR
RF attenuation	40,	41:	30 dB
IF attenuation	40,	41:	40 dB
Frequency		20:	0.1 MHz

- Press CAL. button 15 and hold down (total calibration).
- Feed sinewave signal (0.1 MHz, 60 dBμV ±0.1 dB, 50 Ω) into the ESH 3.
  Nominal indication after fine tuning to
  maximum indication .... 60 dBμV ±1 dB

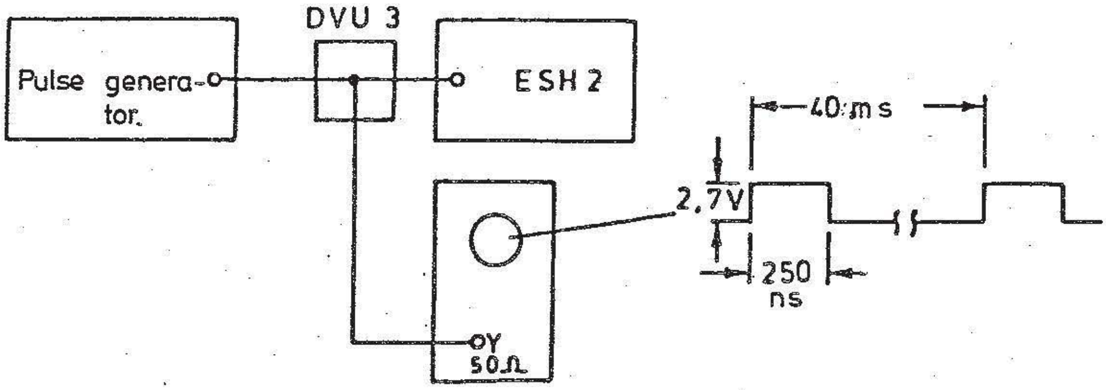
Correct, if necessary, by means of R89 on Y10:

Indicated value too high ⟶ turn R89 counterclockwise ⟶ calibrate ⟶ measure

Indicated value too low ⟶ turn R89 clockwise ⟶ calibrate ⟶ measure.

5.3.2.7 Checking the CISPR 3 Weighting Circuit

Test item:



Connect a pulse generator with an adjustable repetition frequency in compliance with CISPR 3 requirements to the input of the ESH 3. Feed a pulse with a repetition frequency of 25 Hz, a period of 250 ns and an amplitude of 2.7 V corresponding to the CISPR 3 standard pulse

$$V \cdot t = \text{approx. } 1.35\ \mu Vs\ (EMF)$$

into the input of the ESH 3.

Required indication .... 40 dBµV ±1 dB

When varying the repetition frequency in compliance with the CISPR 3 requirements, the indication on the receiver must be within the CISPR 3 tolerance limits (Fig. 5-5).

5.3.2.8 Pulse Calibration (CISPR 1) over Frequency Range > 150 kHz

Settings on the ESH 3:	Indicating mode	35	:	CISPR
	RF attenuation	40, 41	:	30 dB
	IF attenuation	40, 41	:	40 dB
	Frequency	20	:	1 MHz

- Press CAL. button 15 and hold down (total calibration).
- Feed sinewave signal (1 MHz, 60 dBµV ±0.1 dB, 50 Ω) into the ESH 3.

Nominal indication .... 60 dBµV ±1 dB
Correct, if necessary, by means of R91 on Y10:
Indicated value too high ⟶ turn R91 counterclockwise ⟶ calibrate ⟶ measure
Indicated value too low ⟶ turn R91 clockwise ⟶ calibrate ⟶ measure.

5.3.2.9 Checking the CISPR 1 Weighting Circuit

Same test setup as for CISPR 3.

Standard pulse: V • t = 0.316 µVs (EMF).

This standard pulse with a repetition frequency of 100 Hz should give an indication of .... 60 dBµV ±1 dB

The calibration pulse generator from Schwarzbeck, Type IGU 2912 supplies a CISPR 2, 4 pulse

V • t = 0.044 µVs (EMF).

This corresponds to a difference of -17.12 dB from the CISPR 1 pulse.
The required indication on the ESH 3 must therefore be .... 43 dBµV ±1 dB with the output attenuator of the IGU 2912 set to 60 dB.

When varying the repetition frequency in compliance with the CISPR 1 requirements, the indication on the receiver must be within the CISPR 1 tolerance limits (Fig. 5-6).

5.3.3 Final Check of the Receiver Performance Data

Check the logic functions in accordance with section 2.2.4 (operating manual) and the performance specifications in accordance with section 3.2 (service manual).

5.4 Electrical Repair

The easy-to-service ESH 3 is designed to minimize the time required to repair it. However, defective components must be replaced only with the parts designated in the relevant parts lists. Certain restrictions must be observed with the following components:

- The detector diodes GL9 and GL10 on Y10 affect the measurement accuracy and the temperature dependence of the receiver. When a repair becomes necessary, the temperature compensation must be readjusted.
- The attenuator Y16 is a thin-film unit whose components can only be replaced by the manufacturers. No attempt should, therefore, ever be made to repair it. The complete defective attenuator must be replaced.

If a great number of ESH 3s are used at one and the same location, it is recommended that a set of receiver modules be kept as replacement to minimize the down-time of the receiver concerned. The replacement of a receiver module is uncritical as the interfaces within the receiver are precisely defined. (Exception: Filter Control and Filter 2 must be replaced together.)

5.5 Mechanical Repair

Since the receiver contains practically no mechanical parts that are subject to mechanical wear and tear - with the exception of the tuning knob and the carrying handle - little mechanical repair will be required.

A normal service tool kit will do for any mechanical repair work that may become necessary.

5.6 Spare Parts

The parts lists of the various receiver modules in the appendix contain the manufacturer's identification numbers (= order numbers) of all the electrical components used. When replacing ICs, make sure to use an IC from the same manufacturer, if possible, since the differences are considerable in spite of the same designation.

To achieve optimum reliability, the boards and modules used in the receiver undergo rigid quality control prior to final assembly.
Components from other makers, such as resistors, capacitors, diodes, transistors, ICs and displays are required to comply with R&S specifications ensuring optimum reliability. It is therefore recommended that defective components should only be replaced by original components that have been passed by R&S.