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MANUAL

FSK ANALYZER
GA 082

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Contents

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1. Characteristics

1.1 Uses

- Measurement of shift
- Crystal-referenced measurement of baud rate
- Continuous analysis of transmission code using standard programs or specific user programs
- Recording of standard-code signals

1.2 Description

1.2.1 General

The FSK Analyzer GA 082 is made up of large-scale integrated electronic circuits. Its high efficiency is based on a 16-bit microprocessor system with a 24-kbyte memory. In addition, it has a built-in demodulator for F1 and F6 operation.

The measurement results are displayed on the front panel together with all essential information. Via a standardized interface (IEC-625 or RS 232C) the measurement results or the identified code can be output to a printer, a visual display unit, or to a computer for further processing.

An integrated demodulator permits the Analyzer GA 082 to be directly connected to the IF or AF output of a monitoring receiver. The GA 082 can also be connected to external demodulators, as for instance to VF telegraph transmission systems, or be operated from the line current of a teletype line. In these cases measurement of the shift is not possible and the associated indicators remain unlit.

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1.2.2 Framing Program for Analysis

The framing program of the microprocessor organizes the execution for the analysis of the method. In mode 0 the analysis programs for the various methods are called up in a search run in fixed sequence and are compared with the incoming bit stream until a positive result is reported. The designation of the reported method which is contained in the program descriptor as well as its internal code number are indicated on the ANALYSIS display (e.g. BAUDOT C7 or ASY-ASCI C10).

In mode 2 only a manually selected analysis program is compared with the incoming signal and a positive or negative statement is made. With the STEP keys the individual methods can be called up successively in the given sequence or directly with the code number by means of the SELECT key.

Parallel with the identification of an available method in mode 0, or with the selection of a method in mode 2 the framing program searches for an associated text decode program. If such a program is available, the signal is decoded according to the selected method when switching to mode 1 and the text is read out on the ANALYSIS display. In mode 1 the text is printed out on a printer and in the other modes the measurement and analysis results as well as bit patterns.

1.2.3 Standard Analysis

The first 6 standard programs recognize idling cycles, which might otherwise easily be misinterpreted. The following 4 programs recognize methods with the CCITT codes No. 2, 3 (ARQ 28 and ARQ 56) and 5. If no method is recognized, the period program tries to detect periodically recurring bit combinations up to a period of 64 bits. If there is no result either, the statistics program is finally used to determine the mark-to-space ration and the average number of bits between two polarity changes. The tabulated programs are based on the following methods:

N 00: STOP-MOD

There is a permanent mark or space condition.

N 01: IDLE 1:1

An idle signal with alternately one mark on one space.

N 02: IDLE 1:6

An idle signal with alternately one mark and six spaces.

N 04: IDLE 14:

A period of 14 bits is exactly repeated. The 14-bit idling cycle can have any format.

N 05: IDLE 28

An idle signal with continuous repetition of 28 bits.

N 06: IDLE 56

An idle signal with continuous repetition of 56 bits.

N 07: BAUDOT

Asynchronous signal of 7.5 bit character length with 1 start bit, 5 data bits with 5-unit code according to CCITT No. 2 and 1.5 stop bits. With the C key the case shift can also be made manually.

N 08: ARQ - 28

Synchronous method according to the 7-unit code CCITT No. 3. Each character has 3 marks and 4 spaces. Every fourth character is transmitted with inverse polarity.

N 09: ARQ - 56

Same as N 08. However, every eighth character is transmitted with inverse polarity.

N 10: ASY - ASCI

Asynchronous signal of 10 bit character length with 1 start bit, 7 data bits according to 7-unit code CCITT No. 5, 1 parity bit with even parity, 1 stop bit.

N 78: Periodicity check

For all periods between 2 and 64 bits it is checked whether single bits or bit groups occur periodically. The individual display formats are shown in Table 1.

The following definitions are used:

IDLE for continuous repetition of a bit group

MARK for periodic repetition of a mark bit

SPAC for periodic repetition of a space bit
ASY for periodic change in mark/space
-ASY for periodic change in space/mark.

N 79: Statistics program

The M/S ratio of the mark and space bits as well as the average number of bits L between the polarity changes are calculated.

Table 1 Standard programs

Code No. N	Indication of analysis display		Recording
00	STOP-MOD	eC00	
01	IDLE 1:1	eC01	
02	IDLE 1:6	eC02	
04	IDLE 14	eC04	
05	IDLE 28	eC05	
06	IDLE 56	eC06	
07	BAUDOT	eC07	X
08	ARQ-28 (CCITT 3)	eC08	X
09	ARQ-56	eC09	X
10	ASY-ASCI	eC10	X
78	PERIOD = aa bbb		
79	M/S = ccc L = dddBIT		

aa = period length in bit

bbbb = IDLE for periodic idling cycle
MARK for periodic mark bit
SPAC for periodic space bit
ASY for periodic change in mark/space
-ASY for periodic change in space/mark

ccc = floating-point number for mark/space ratio

ddd = floating-point number for average number of bits between polarity changes

e = "-" for inverted codes

1.2.4 User-specific Programs

In addition to the standard analysis methods the instrument can however readily be adapted to used-specific methods. For this purpose an EPROM capacity of up to 8 kbyte is available in area A and B. In order to protect this area from inadvertent access, a lockable external EPROM unit can be supplied as an option.

1.2.5 Pin Assignment of 7-way Female Tuchel Connector "FSK SIGNAL"

Pin	Signal
1	Regenerated signal
2	Bit clock
3	F6 relay B+
4	F6 relay A+
5	F6 relay B-
6	F6 relay A-
7	Ground

2.1 Legend for Figs. 2-1 and 2-2

No.	Marking	Function
1	TIME	3-digit readout of measurement time in minutes.
2	DEMOD	Indication of momentary frequency by 32 LEDs. The frequency spacing between the outer marking points below the display window is determined by the shift indication 3. By switching the SHIFT/FREQ key 13 to FREQ, a fixed frequency scaling of 64 Hz per display element is used.
3	SHIFT/FREQ	4-digit readout of line shift in Hz. With the SHIFT/FREQ key switchover to indication of the centre frequency in kHz can be made.
4	RATE	8-digit readout of baud rate. Leading zeros are suppressed. The digits after the decimal point are indicated according to the measuring accuracy achieved. There is a maximum of 5 digits after the decimal point and for values greater than 1000 baud, 4 digits are indicated after the decimal point.
5	SYNC	16 LEDs indicating the position of the signal edges referred to the measured baud rate.
6	MODE	1-digit display of the mode for the code display and code analysis.
7	CODE	Display of the individual code bits by 48 LEDs. Display mode depends on mode 6.
8	ANALYSIS	16-digit alphanumeric display of the code analysis results and the operating states of the instrument. After switching the GA 082 on, the system version and the fitted user programs are indicated. If CONST function 11 has been selected, the time constant of the control loop

No.	Marking	Function
		for bit synchronization is indicated. In mode 1 the clear text is read out in running mode.
9	START	Function key for starting a new measurement. The LED integrated in the key lights until the first determination of the baud rate has been completed.
10	SELECT	Yellow prefix key. After switching on the SELECT function, the yellow designations are valid for the subsequent two keyboard entries. The numbers 00 to 79 are reserved for code numbers and 80 to 99 for user-specific additional functions. The following additional functions can be selected with X0 to X9: X0... front panel off (front panel on when actuating the power switch) X1... F6 on X2... phase control loop on X3... phase control loop off X4... baud rate control loop on X5... baud rate control loop off X6... user programs off X7... user programs on X8... bit clock off X9... bit clock on
11	CONST	Function key for switching on the control loop constants on ANALYSIS display 8. The constants can be manually varied from 0 to 15 by means of the STEP keys 23. Automatic stepping of the constants is disabled.
12	PRINT	Function key for output of the measured data in mode 0 and 2 with a spacing of 1024 bits. Output of clear text in mode 1. Output of 16-line contents of the refresh memory in modes 6 to 9. Output of the code bits in mode 0 and 2 to 5 provided that the auxiliary functions B (19) and/or C (18) have been switched on. With B single bits, which C four bits and with B plus C eight bits are output with an ASCII character.

No.	Marking	Function
13	FREQ/SHIFT	Function key for switching on the centre-frequency indication on 3 and for indication of the momentary frequency on 2 with a fixed frequency scaling of 64 Hz.
14	CHAN1/2	Function key for switching on the second signal input at socket 34. In F6 mode the internal demodulator switches over to the 2nd channel.
15	DEMOD	Function key for switching on the internal demodulator. The indications 2 and 3 are activated.
16	TEST	Function key for switching on the test run for all indications on the front panel. The internal 75-baud test is triggered by additionally actuating the C key. 1200 and 2400 Hz are used as F1 frequencies.
17	POWER	Power switch for switching on the GA 082 and for resetting the microprocessor.
18	C	Auxiliary function key for PRINT, TEST and FIX. With Baudot signals the case shift is made in mode 1. In mode 2 inverted code is selected.
19	B	Auxiliary function for PRINT and FIX.
20	A	Auxiliary function for suppressing the sync test for the first baud rate evaluation. With Baudot signals each individual character is sychronized.
21	FIX	Function key for switching off the automatic restart. After pressing START, the first baud rate evaluation is skipped and the control loop directly started with the previously measured or adjusted baud rate. The control loop is adjusted for Baudot signals by means of key B. By additionally actuating key C, it is adjusted for inverted Baudot signals.

No.	Marking	Function
22	LENGTH ↑↓	Keys for increasing or reducing the line length for the code display in modes 6 to 9 and for the code output with PRINT-B or PRINT-C in mode 0 and 2 to 5. The selected length is indicated on the ANALYSIS display in modes 4 to 9.
23	STEP ↑↓	Keys for increasing or reducing various parameters which are indicated on the ANALYSIS display. In mode 2 the code number is varied. In modes 4 to 9 the bits displayed on the CODE display 7 are shifted in either direction. If the CONST function 11 has been switched on, the time constant of the control loop is varied in steps.
24	MODE ↑↓	Keys for varying the mode in steps up or down.
25	RATE ↑↓	Keys for manual change of the baud rate adjusted in the control loop. The change rate steadily increases until it reaches a maximum speed. It is scaled with the aid of the control loop constant.
26	SHIFT/FREQ ↑↓	Keys for manual change of the shift or, if the FREQ/SHIFT function 13 has been selected, of the centre frequency with steadily increasing speed.
27	220/240 V ...	AC supply connection with voltage selector.
28	INPUT F PROGRAM UNIT	Plug-in module for user programs (option).
29	ADDRESS	Coding switch for IEC-bus address and for switchover between IEC-bus and V24 output.
30	IEC 625	24-way female connector for IEC-bus connection.

No.	Marking	Function
31	RS232C-V24/V28	25-way female connector for V24 connection.
32	AF/IF	BNC female connector for AF or IF input.
33	FSK SIGNAL -30...+30 V	BNC female connector for input of demodulated signal.
34	FSK SIGNAL 10...60 mA	8-way female Tuchel connector for 2 inputs for demodulated signals and outputs for bit clock and regenerated signal.
35	EXT. REF. 1, 5, 10 MHz	BNC female connector for input of external reference frequency.
36	SPARE FUSES	Place for four spare fuses

2.2 Preparation for Use

2.2.1 Setting Up

Bench model:

The bench model of the GA 082 contains the basic unit in an aluminium case with carrying handle. The instruments can be stacked. When unlocking the two swivel joints by exerting lateral pressure on them, the handle can be adjusted to various positions. It can also be removed altogether by undoing the screws at either side in the swivel joint.

Rackmount:

The rackmount model has a handle at the two sides of the front panel and the unit itself is fixed in a 19" rack by means of four screws. The perforations in the top and bottom plate are provided for air circulation and must not be covered up.

2.2.2 AC Supply Voltage, Grounding

The GA 082 is factory-adjusted for an AC supply voltage of 220 V. The following voltages can be selected: 110, 120, 220 and 240 V; permissible deviations: +10% to -10%; AC supply frequency: 47 to 440 Hz.

The set can readily be adjusted for another AC supply voltage with the aid of the voltage selector 27. In this case the fuse link with the fuse must be removed and the following be inserted instead:

For 220 and 240 V: T1D
For 110 and 120 V: T2D

The cabinet is grounded via the AC supply connector.

2.2.3 Selection of Frequency Standard

see Fig. 2-3

The GA 082 is fitted with an internal frequency standard with a drift of 10^{-6}. Switchover to an external frequency standard is made by means of switch S1 on the interface board, which is accessible after opening the cover of the cabinet (Fig. 2-3). Depending on the position of the two switches S1.1 and S1.2, switchover can be effected between the internal frequency standard and an external frequency fed in via the EXT. REF. input 35.

Table 2 Selection of frequency standard

S1.1	S1.2	Frequency standard
0	0	internal 5 MHz
1	0	external 1 MHz
0	1	external 5 MHz
1	1	external 10 MHz

The input voltage of the externally fed in standard frequency should be in the range from 0,3 V to 1 V_{rms} into 1 kΩ.

The location of switch S1 on the interface board is shown in Fig. 2-3.

2.2.4 Connection to External Demodulator

If the DEMOD function 15 has not been selected, an externally demodulated signal is evaluated which is applied to one of the inputs 33 or 34. Only one of the two input sockets may be connected at a time, since the voltage input 33 is internally connected to the current input 34. Fig. 2-4 shows the input circuit diagram for demodulated signals.

The current input 34 has two channels which can be selected with the aid of the CHAN1/2 function. Both channels can be externally demodulated with an F6 signal and then be selected. Two optocouplers are connected with opposite polarity and are linked up via a flipflop and a 2-way switch so that both positive or negative single current and double current can be processed.

All voltages below +1 V at input 33 are regarded as logic 0 and those above 1.2 V as logic 1. The input can also be operated from TTL or V.28 levels.

2.2.5 Connection to Receiver IF

For measuring the shift the GA 082 needs the AF or IF signal of the receiver at the AF/IF socket 32. For this purpose the internally adjustable mixer oscillator must be matched to the given IF. The mixer frequency is adjusted in steps of 360 Hz by means of the switches S2 and S3 on the interface board (see Fig. 2-3). The values of the individual switches are listed in the following table.

Table 3 Adjusting the mixer frequency

Switch	Frequency value [Hz]
S2.1	360
S2.2	720
S2.3	1,440
S2.4	2,880
S3.1	5,760
S3.2	11,520
S3.3	23,040
S3.4	46,080
S3.5	92,160
S3.6	184,320
S3.7	368,640
S3.8	737,280

The maximum adjustable frequency is 1,474,200 Hz. The mixer frequency must be selected below or above the given IF so that a difference of about 2 to 3 kHz is obtained. The IF can be checked by feeding in a constant tone. With the functions DEMOD - FREQ - FIX - START the light dot on 2 must appear above the central marking after the centre frequency on the display 3 has been

adjusted to the calculated frequency difference with the aid of keys 26. A blurred indication implies that either the mixer frequency is wrongly adjusted or the IF signal is too weak. The amplitude of the AF/IF signal should be between 50 mV and 1 V_{rms} into 50 Ω.

The mixer frequency is derived from the processor crystal. The frequency of the crystal can be checked as described in 2.9.4.

For AF signals the mixer frequency ist set to zero. The signal frequencies should be within the range 1.2 to 8 kHz. Frequencies as low as possible should be used since the accuracy of the internal demodulator decreases with increasing frequency. This should particularly be noted for the magnetic-tape recording of AF signals for later analysis. The flutter and wow during the playback can be prevented by limiting the control loop constants of the baud rate control loop with the aid of the CONST function 11 (see 2.4.2).

For the most common IFs the mixer frequencies listed in table 4 can be used.

Table 4 Adjusting the mixer frequency for common IFs

IF kHz	S2 1234	S3 12345678	Mixer frequency kHz	Centre frequency kHz
30	0011	00100000	27.36	2.64
	0101	10100000	32.40	2.40
200	1010	01000100	197.64	2.36
	0100	11000100	202.32	2.32
525	1101	01011010	522.36	2.64
	1001	11011010	527.40	2.40
1400	0101	01001111	1,397.52	2.48
	1110	11001111	1,402.20	2.20

The 1 position of the switch corresponds to the open switch position. Care should be taken whether the mixer frequency has been set above or below the IF, i.e. whether the sequence of the signal frequencies should be inverted or not.

With correctly tuned receiver the adjusted centre frequency is indicated on the SHIFT/FREQ display 3 if FREQ function 13 has been switched on.

2.2.6 Connection of Serial V.24 Interface

The serial interface 30 is designed to standards V.24/28 and RS232C.

The pin assignment of the 25-way Cannon connector is shown in Table 5.

Table 5 Pin assignment of V.24 interface

Pin	V.24 signals	Internal links
1	E1 (101) safety ground	
2	D1 (103) transmitted data	
3	D2 (104) received data	
4	S2 (105) switching on transmitter section	<—
5	M2 (106) ready for transmission	<— DSR
6	M1 (107) ready for operation	<— DSR
7	E2 (109) return line	
20	S1.2 (108/2) data terminal equipment ready for operation	<— DTR

The signals S2 and S1.2 as well as M1 and M2 are combined in the instrument. The two signal states are:

0 = +12 V
1 = -12 V

After switching the GA 082 on, S1.2 is adjusted to +12 V and signals that the GA 082 is ready to accept serial data. The data output is only released if the data receiver (e.g. printer) has signalled via M1 its readiness to receive data by a signal above +2.5 V. The M1 line is checked at time intervals of 3.3 ms and a

character may then be output. By externally connecting S1.2 to M1 (pin 4 or 20 to pin 5 or 6) a permanent release of the data output is enforced. The maximum output rate is 300 characters/sec provided that a sufficiently high baud rate has been selected.

The baud rate for the serial interface is internally adjusted on the processor board by means of the S1 switches (see Fig. 2-3). Table 6 shows the switch positions for the various baud rates. Position 1 corresponds to the open switch contact. The switch position can only be read in after the GA 082 has been switched on. Any variation of the set values becomes only effective if the GA 082 is switched off and on again.

Table 6 Baud rates for V.24 interface

S1 5 6 7 8	Baud rate
0 0 0 0	-
1 0 0 0	50
0 1 0 0	75
1 1 0 0	100
0 0 1 0	110
1 0 1 0	134,5
0 1 1 0	150
1 1 1 0	200
0 0 0 1	300
1 0 0 1	600
0 1 0 1	1200
1 1 0 1	1800
0 0 1 1	2400
1 0 1 1	4800
0 1 1 1	9600
1 1 1 1	-

The 4th switch of the S1 switches on the processor board cuts in the AUTOFEED function. If the AUTOFEED function is switched on (switch closed), the LF character (line feed) following the CR character (carriage return) is suppressed in the data output. A connected printer, for instance, must then also be set to AUTOFEED and after CR automatically carry out LF.

The data input and output is made in 8-bit ASCII code without parity. Each character starts with a start bit (space) and ends with a stop bit (mark), so that a total of 10 bits/character is sent.

2.2.7 Switching On

Prior to switching on the GA 082 for the first time, care should be taken that the adjusted AC supply voltage agrees with the local AC supply.

The GA 082 is switched on with the power switch 17. Upon switching on the microprocessor and the peripheral modules are reset. After a memory check of the RAMs and EPROMs, which might lead to error indications, the system version and the user programs that may be fitted are indicated at ANALYSIS display 8 for about 1.5 sec, as for instance:

SYSTEM2.0 USER12

The equipment functions are then set to an initial state which enables immediate processing of a demodulated signal present at a signal input in mode 0. At this time only mode 6 and the decimal point after the 3rd digit in the baud rate readout 4 are indicated on the front panel.

2.3 Operation of Built-in Demodulator

2.3.1 Automatic Adjustment for F1 and F6 Signals

The built-in demodulator is switched on by means of the DEMOD key 15. It operates in the range from 2 to 200 baud for frequency shifts of 30 to 2000 Hz.

The built-in demodulator measures the momentary frequency 1200 times per second and thus evaluates the current signal status. The bandwidth of the receiver connected ahead must be adjusted so that only a single frequency-modulated signal can be received. For the suppression of noise components the bandwidth should be matched as closely as possible to the signal bandwidth, i.e. correspond approximately to the sum of shift and baud rate.

In F1 mode two frequencies f_1 and f_2 are allocated to the two signal states of the teletype signal, i.e. mark (1) and space (0). Mark corresponds to the lower frequency f_1. The shift is expressed by the frequency spacing $f_2 - f_1$. The most common shifts are between 70 Hz and about 1 kHz. In some cases even greater shifts are used.

In F6 mode two teletype channels can be transmitted simultaneously. Since there are four different status combinations of the two channels, four different frequency values f_1 to f_4 with equal spacing from each other are used. Fig. 2-5 shows the allocation of the frequencies to the individual channel states. Like in F1 mode, channel 1 is also determined by the position of the frequency with respect to the centre frequency. Status 1 is assigned to the frequencies f_1 and f_2 which are below the centre frequency, and status 0 to the frequencies f_3 and f_4 which are above the centre frequency. Channel 2 decides whether within the frequencies below or above the centre frequency the lower frequency (status 1) or the higher frequency (status 0) is used.

The shift indicated on the GA 082 refers for F6 signals to the spacing between the two outer frequencies $f_4 - f_1$. The spacing between adjacent frequencies is 1/3 of the indicated shift.

By starting a new measurement, the built-in demodulator is automatically adjusted for the incoming F1 or F6 signal. For this purpose the measured momentary frequencies are statistically recorded until individual frequency lines are displayed. With 2 lines F1 modulation is expected and with 4 lines F6 modulation. For F6 modulation "F6" is directly indicated on the ANALYSIS display 8.

2.3.2 Indications of the Demodulator

After the demodulator has been adjusted to the given centre frequency and the shift, the shift is read out in Hz on the SHIFT/FREQ display 3. By means of the SHIFT/FREQ key 13 the indication can be switched to the centre frequency in kHz.

The momentary frequency of the signal is indicated by 32 LEDs on the DEMOD display 2. With correctly adjusted demodulator the two frequency lines in F1 mode and the two outer frequency lines in F6 mode are directly above the marking points. The frequency scale for the spacing between the marking points can be read off the SHIFT display 3. With the aid of the SHIFT/FREQ key 13 a fixed scale can be selected for display 2. The frequency spacing between the individual LEDs is exactly 64 Hz and a total frequency range of 32 x 64 = 2048 Hz is covered.

2.3.3 Demodulation of F1 Signals

For the demodulation of F1 signals frequency thresholds are defined according to Fig. 2-6 in order to fix the assignment of the momentary frequencies to the two signal frequencies. With $\Delta f = f_2 - f_1$ each frequency line has a range of $\Delta f/2$. The momentary frequencies falling within this range are averaged for accurate determination and tracing of the frequency line. With several frequencies in the same range, the change from one range to the other is recorded as a change of the signal status.

Two conditions of the demodulator cause a new start if the FIX function 21 has not been switched on. Firstly it is checked whether there are sufficient momentary frequencies within the ranges of the two frequency lines. If there are too many frequencies out of these ranges, a new start is triggered. And secondly, a new start is also triggered if there is an insufficient number of status changes. This is the case, for instance, with a continuous tone.

2.3.4 Demodulation of F6 Signals

For the demodulation of F6 signals adjacent frequency ranges according to Fig. 2-7 are created for the four frequency lines, to which the momentary frequencies can be assigned. Each frequency range corresponds to a different status combination of the two channels. The particular combination is assumed as being given if several successive momentary frequencies fall within the associated frequency range. For further processing one channel must be selected. With CHAN1/2 function 14 switched off, channel 1 is evaluated and with CHAN1/2 function switched on, channel 2 is evaluated.

It should be noted that the shift indicated on 3 corresponds to the difference $f_4 - f_1$ and is equal to three times the spacing between adjacent frequencies.

Like in the F1 mode, a new start is automatically triggered if too many frequencies are out of the f_1 and f_4 range or if there are no status changes of the signal.

2.3.5 Manual Setting of the Demodulator

The two setting parameters of the demodulator, i.e. centre frequency and shift, can also be varied manually by means of the SHIFT/FREQ keys 26. If the keys are pressed for a longer time, the change rate increases steadily until it reaches maximum speed. If the SHIFT/FREQ function 13 has been switched off, the shift is varied and if the SHIFT/FREQ function is switched on, the centre frequency can be varied. It should be noted that there is a different scale on the DEMOD display 2.

If no momentary frequencies have yet been indicated on display 2, the automatic presetting of the demodulator can be skipped by switching on the FIX function 21 and pressing the START key 9.

With SELECT - X1 the demodulator can be adjusted for F6 signals. If a new start is triggered, it is reset for F1 demodulation.

2.4 Measurement of Baud Rate

2.4.1 Checking of Single Bits

The demodulated teletype signals can only assume two different status, i.e. mark (logic 1) and space (logic 0). For picking up the signal, it is therefore sufficient to record the time of the status changes. For this purpose the time intervals between successive status changes as well as the status present during the intervals are measured and stored into a ring buffer which has a capacity of 768 intervals.

At the beginning of the measurement the start program is executed first and this is indicated by lighting up of the START key 9. Fig. 2-8 shows the program sequence in simplified form. The start program is triggered by pressing the START key or, if the FIX function 21 has not been switched on, by automatic start. In the case of very high baud rates there is also an automatic start after the current signal processing has been aborted (see 2.4.6).

At the beginning of the start program all parameters required in the course of the measurement are set to their initial state. The measuring time is set to zero. The LED of the START key lights up. The first determination of the baud rate is skipped if the FIX function has been switched on. The control loop is retriggered with the old values. With the aid of the auxiliary functions B and C the control loop can be adjusted for Baudot signals (see 2.4.5).

If the FIX function has not been switched on, the built-in demodulator - if used - is adjusted automatically (see 2.3.1). The demodulator then waits until 128 signal intervals have been collected. The waiting time depends on the given baud rate. Since generally are approximately two bits per interval, a waiting time for about 256 bits must be allowed for. For 50 baud this means 5 sec, for 100 baud still 2.5 sec.

As soon as 128 intervals have been collected, the first determination of the baud rate is made with the aid of the single-bit check. The collected mark and space intervals are separately statistically evaluated. The smallest interval occurring sufficiently often is taken as a single bit and used for the first baud rate determination. The accuracy of the measured value can be futher improved by taking all 128 intervals into account.

Part of the single-bit check is also the Baudot check which determines whether the asynchronous Baudot code with 7.5-bit character length applies to the signal. If this is the case, a "B" is directly indicated on the ANALYSIS display 8.

If the single-bit check does not yield a useful result, the start program is repeated. Usually the single-bit check is followed by a synchronous test before the determined baud rate is finally accepted. It is checked whether the signal edges more or less match with the cycle of the determined bit length. If the test result is negative, the start program ist also repeated. If the A function 20 is switched on, the synchronous test is skipped. The baud rate can thus be determined even for signals with strong interference. The measured values supplied should be checked in this case by the user for reliability. A probable value should be selected from several measurements.

After completion of the first baud rate determination the control loop is adjusted to the baud rate determined and the LED of the START key is switched off. All intervals already collected as well as the new intervals are now processed in the control loop. The single-bit check with subsequent synchronous test is continued to be carried out in the background after every 128 intervals and the result is compared with the baud rate adjusted in the control loop. If the deviation is greater than 3%, the control loop is directly started with the new baud rate. By switching on the FIX function 21, the continuous single-bit check can be switched off and the baud rate adjusted in the control loop be fixed.

2.4.2 Control Loop for Bit Synchronization

After the first baud rate determination by the start program the control loop is the centre for further processing. Fig. 2-9 shows a functional diagram.

The control loop consists of two series-connected subcircuits which fulfill different tasks. The phase loop is synchronized to the signal edges and determines from each interval the correct number of marks or spaces, which are stored as bit pattern in the code memory for later code analysis. The baud rate loop considers

the phase loop as frequency discriminator and improves the baud rate if there is a continuous phase error. The time constant for the fault determination is in both control loops automatically switched from 0 to 10. With the CONST function 11 enabled, it can be manually switched in steps from 0 to 15 by means of the STEP keys 23. With the CONST function switched on, each variation of the constant is indicated in minutes on the ANALYSIS display 8 together with the integration time which is determined by the baud rate. The CONST function also interrupts the automatic stepping up of the time constants beyond the value 3. When the CONST function is disabled, the ANALYSIS display is erased and the time constant selected last is automatically switched again.

The individual parts of the control loop can be switched on and off by means of the following auxiliary functions:

- SELECT - X2 - phase control loop on
- SELECT - X3 - phase control loop off
- SELECT - X4 - baud rate control loop on
- SELECT - X5 - baud rate control loop off

These switching possibilities are useful for certain applications. If the baud rate of a signal is already known, the synchronization of the signal edges can be carried out by the phase control loop alone if the baud rate control loop is switched off. With the phase control loop switched off, the comparator still remains active and determines the code elements from the measured signal intervals. This operating mode is recommended for recording with a higher sampling rate. When setting, for instance, four times the baud rate, four code elements are produced for each bit. A message appearing at any time can thus always be correctly recorded.

The comparator determines for each signal edge the deviation from the continuous baud rate clock. This error is indicated by 16 LEDs on the SYNC display 5. The LEDs always cover an error range of ±1/2 bit. Zero error is in the centre above the marking point. From the fluctuations about the centre point conclusions can be made as to the quality of the signal. By comparing the signal edges falling in the range of the five central LEDs with the edges outside of this range it is determined whether the internal

baud rate clock has been synchronized to the signal edges. If this is not the case, a new start of the measurement is triggered. The new start can be prevented by means of the FIX function 21.

The control loop triggers also the TIME indication 1. It reads out the measurement time in minutes.

2.4.3. Automatic Start

A new measurement can be triggered at any time by pressing the START key 9. To facilitate the operation and to suppress erroneous results a number of tests are incorporated which may cause an abortion of the current measurement. The various conditions for an automatic start are given in Table 7. The conditions 1 to 4 for a new start can be disabled by switching on the FIX function 21.

When switching the receiver to new signals, mainly the conditions 3 and 4 cause the GA 082 to be also automatically adjusted for the new signals.

Table 7 Conditions for new start

No.	Condition
1	Insufficient number of frequency samples of the demodulator falling within the range of the frequency lines.
2	Continuous tone present at the demoduator.
3	Signal edges not predominantly within the central range of SYNC indication.
4	Baud rate from single-bit check differing more than 3% from indicated baud rate.
5	More than 9700 intervals/sec being produced. OUT OF RANGE being indicated.
6	Processing of signal intervals lagging behind. OVERLOAD being indicated.

2.4.4 Manual Setting of the Baud Rate

The baud rate adjusted in the control loop can be varied with the aid of the RATE keys 25. When keeping the keys depressed for a while, the rate of change increases steadily until it reaches a maximum speed. The change of speed is also proportional to the adjusted control loop time constant. With large time constants small variations in the last digits of the indicated baud rate are thus also possible. For a quick change the time constants must be limited to small values by switching on the CONST function 11 and pressing the START key 9. Automatic adjustment of the baud rate can be disabled by means of the FIX function 21.

By observing the SYNC indication 5, multiples of the given baud rate can be adjusted. This is necessary, for instance, if the signal is to be sampled with four times the baud rate.

2.4.5 Processing of Baudot Signals

The Baudot signals with their character length of 7.5 bits require a special treatment for entering them into the processing scheme of the GA 082. Together with the single-bit check a Baudot check is therefore also carried out in order to recognize any Baudot signals. It is also determined whether the Baudot signal is present in normal or in inverted position.

Special attention must then be given to the Baudot signals in the comparator of the control loop shown in Fig. 2-9. The comparator is synchronized to the individual Baudot characters by carrying out a 1.5 bit after every six single bits. Thus it reaches a character length of 7.5 bits. For the 1.5 stop bit just one code bit is counted in this way, so that only 7 bits/character in all are entered into the code memory. Due to the stop-start transition of the Baudot signal the comparator has always the opportunity to match its internal 7.5-bit counting rate to the signal.

Since the Baudot code is an asynchronous method (see 2.6.7), each character can stand for itself and a new character need not begin after 1.5 stop bits. Therefore, there must be the possibility of interrupting the continuous baud rate clock and synchronizing it

to each start edge. This is done when switching on the auxiliary function A 20. The bits are then counted beginning from the start edge of the Baudot character. A more accurate determination of the baud rate is not possible in this case since the code is not based on a continuous clock.

If the individual characters are entered manually (e.g. radio amateurs), the Baudot method cannot directly be recognized since there are hardly any 1.5 stop bits. In this case the GA 082 can be manually adjusted to the Baudot code. For this purpose the functions - FIX - B - START must be switched on for normal signals and - FIX - B - C - START - for inverted signals. "B" or "B-" is indicated on the ANALYSIS display.

2.4.6 Limitation at High Baud Rates

Even the powerful 16-bit microprocessor used in the GA 082 is limited at high baud rates. A maximum of about 1500 intervals/sec can be accepted and processed. The work load of the microprocessor can be reduced and more intervals per unit time be handled when switching off individual functions like

- FIX for switching off the automatic START
- SELECT - X4 - for switching off the baud rate control loop
- SELECT - X2 - for switching off the phase control loop.

Signal intervals are recorded up to about 10 kbaud. They are first entered into a buffer for 768 intervals. In the case of overload further signal recording is stopped and all stored intervals are processed. With about 2 bits/interval a first code analysis over 1024 bits is thus even possible in the range from 2400 to 9600 baud with the aid of the stored intervals. After display of the analysis result OVERLOAD is indicated for about 1.5 sec on the ANALYSIS display 8 and then a new start triggered.

Prior to the code recording the number of signal intervals/sec is checked and in case of more than 9600 intervals/sec a new start is triggered after OUT OF RANGE has been indicated.

2.4.7 Bit Clock and Regenerated Signal

Independent of the signal interval processing, a bit clock and a regenerated signal is made available up to about 600 baud for external recording and display of the internally or externally demodulated signal. The two signals can be switched on by means of the auxiliary function - SELECT - X9 - and switched off by the auxiliary function - SELECT - X8. The position with reference to the demodulated signal is shown in Fig. 2-10.

The bit clock consists of 100 µs pulses. The regenerated signal is delayed by half a bit as against the demodulated signal. The edges of the regenerated signal always follow the positive leading edge of the bit clock. Both signals are supplied as TTL levels at the Tuchel socket 34 with an output impedance of about 500 Ω.

Pin assignment:

Bit clock at pin 2
Regenerated signal at pin 1
Ground at pin 7

2.5 Code Display

2.5.1 Single-Bit Display in Modes 3, 4, 5

The CODE display 7 with its 48 LEDs offers the possibility of displaying the single code bits in different ways in modes 3 to 9. One bit is assigned to each LED. For observing the single bits, modes 3 to 5 should be used.

In mode 3 the single bits are shifted into a 768-bit memory at the same speed as they are generated. The last 48 bits are displayed as running code on the CODE display 7. The LED that lights corresponds to the mark bit (logic 1).

In mode 4 the incoming bit stream is stopped and the last 48 bits are on the CODE display. By means of the STEP keys 23 the bit stream can be shifted right or left. When keeping the keys depressed, the shift speed is steadily increased up to a maximum. The number of shift steps is indicated on the ANALYSIS display 8, e.g.

STEP = 27 LEN = 35

By pressing both STEP keys, the shift counter is reset. For step numbers below zero the negative sign "-" is indicated after STEP. The line length LEN can also be varied in this mode with the aid of the LENGTH keys 22. This is however only significant for the code output (see 2.7.2).

In mode 5 the inverted bits are displayed, i.e. the lit LED corresponds to the space bit (logic 0).

2.5.2 Dynamic Code-Line Superimposition in Modes 6 and 7

In mode 6 the code bits are continuously entered into 16 lines of the refresh memory and the rapidly changing lines are superimposed on CODE display 7. Periodically recurring bit combinations can thus be recognized. In mode 7 the code of mode 6 is inverted.

Table 8 Code line superimposition

12345678901234567890...	Zeile
> 10010101011011	1
> 10100011001101	2
> 10011011010110	3
	.
	.
	.
> 10001101010101	15
> 10100111001011	16

Table 8 shows the example for a Baudot code displayed with a line length of LEN = 14. The individual bits are currently entered into individual lines: the first 14 bits into the first line, bits 15 to 28 into the second line etc. until after 16 x 14 = 224 bits all lines are filled and the bits are entered into the first line again. In a cycle of 107 ms each line is displayed for 6.7 ms in the CODE display. In the above example the character length is 7 bits so that 2 characters are entered into each line. The start-stop transitions are at positions 1 and 2 as well as at 8 and 9. The positions 2 and 9 remain completely dark since there is not a single logic 1 in all 16 lines. It is difficult to recognize whether in positions 1 and 8 all lines have a logic 1. Therefore it is reommended to switch from mode 6 to mode 7 for this check. Since in this mode all bits are inverted, it is easier to recognize whether in positions 1 and 8 there is logic 0 in all lines.

A line length of up to 256 bits can be selected, but only 48 bits thereof can be displayed. With the aid of the STEP keys 23 the displayed code can be shifted left or right. As in modes 4 and 5, the step count and the line length which can be varied with the LENGTH keys 22 are indicated on the ANALYSIS display 8.

By switching on the PRINT function 12, the momentary contents of the 16 lines of the refresh memory can be output (see also 2.7.3). It should however be noted that the bit entered last may be at any place.

Mode 6 or 7 is particularly useful to show the activity of the individual channels in view of the numerous multiplex methods.

2.5.3 Static Code-Line Superimposition in Modes 8 and 9

In modes 8 and 9 there is the same superimposed code display as in modes 6 and 7. The code bits are however no longer entered straight away, but the incoming code bits are first stored in a code memory which can accept up to 8192 bits. After switching on mode 8, the CODE display 7 remains dark until 1024 bits have been collected. These are used to fill 16 lines of the refresh memory all at once. For loading the bits from the code memory into the refresh memory, the two parameters LEN for the line length and STEP for the selection of the first bit, which are indicated on the ANALYSIS display 8, are decisive. Upon any variation of one of these parameters by means of the associated STEP or LENGTH keys the refresh memory is reloaded from the code memory. This enables rapid scanning of the code.

By switching on the PRINT function 12, the contents of the 16 lines of the refresh memory can be printed out. By stepping up the STEP counter by 16 x line length, the subsequent code block can be displayed and also output when switching on the PRINT function again. The complete contents of the code memory can thus be successively displayed in sorted sequence. It is recommended for this purpose to reset the STEP counter at the beginning of each code block by simultaneously pressing both STEP keys. For resetting the counter the left key must be pressed first and released again. Then the right key must be pressed and then the left key. The counter is now reset and both keys can be released.

2.6 Code Analysis

2.6.1 Search Run in Mode 0

After determination of the baud rate, the code bits are derived from the signal intervals in the control loop (see 2.4.2) and stored in the code memory which has a capacity of 8192 bits. This memory is ring-structured, i.e. it enables continuous writing and the least-significant memory address is directly followed by the most-significant address. The code analysis evaluates the code memory contents with the aid of various programs. There are programs for finding out the coding method being used. They are called up in mode 0 or 2 after 1024 bits have been collected. In addition, individual decode programs can be used for the output of a clear text. In mode 1 a previously selected decode program is called up after every 8 collected bits.

The basic model of the GA 082 already contains a number of analysis programs. The program structure of the code analysis is such as to permit an extension of the program simply by adding futher programs. For this purpose the EPROM locations A and B are provided internally on the microprocessor board (Fig. 2-3), or the program unit option 28 on the rear panel (see 2.6.10).

In mode 0 a search run is executed for all programmed codes. The analysis programs for the various codes are called up in a fixed sequence and the stored code bits are checked for the characteristics of the individual codes. The first code yielding a positive result is indicated on the ANALYSIS display 8. The standard programs are tabulated in the following table 9.

If the EPROMs A and B are fitted with the user programs, they determine the sequence of the code analysis. When switching the GA 082 on, it is checked whether user EPROMs are fitted. By means of the auxiliary functions X6 and X7 the user EPROMs can be switched on and off also during operation.

Table 9 Standard analysis programs

Code No.	Indication on ANALYSIS display		Text progr.	For details see section
00	STOP-MOD	N00		2.6.6
01	IDLE 1:1	N01		2.6.6
02	IDLE 1:6	N02		2.6.6
04	IDLE 14	N04		2.6.6
05	IDLE 28	N05		2.6.6
06	IDLE 56	N06		2.6.6
07	BAUDOT	N07	X	2.6.7
08	ARQ-28	N08	X	2.6.9
09	ARQ-56	N09	X	2.6.9
10	ASY-ASCI	N10	X	2.6.8
78	PERIOD = 28	MARK		2.6.4
79	M/S = 1.0 L = 2.0	BIT		2.6.5

The display format on the analysis display may be determined by the code itself or follow a standard pattern. In the latter case the designation of the code in the program header is indicated by 8 characters in the left-hand part of the 16-digit display. The 2-digit code number from 00 to 79 allocated to the code is indicated with a preceding "N" in the right-hand corner. With inverted code, the negative sign "-" is indicated ahead of the code number. Four display fields are reserved for the identification of the different versions of the code.

The first six standard programs recognize idling cycles, which might otherwise easily be misinterpreted. The following four programs recognize methods with the CCITT codes No.2, 3 and 5. If no code is recognized, the period program N78 tries to detect periodically recurring bit combinations up to a period of 64 bits. If there is no result either, the statistics program N79 is finally used to determine the mark-to-space ratio and the average number of bits between the signal edges.

Parallel with the identification of a code it is checked whether a test decode program with the same code number is available. This program for decoding is enabled in mode 1.

2.6.2 Single-Code Analysis in Mode 2

Like in mode 0, the code analysis is called up every 1024 bits also in mode 2. Only a single, pre-selected code is however checked. If the characteristics of this code hold true, the code designation is indicated on the ANALYSIS display 8 in the format shown in Table 9 (2.6.1). There is the same indication also in the case of a negative test result, with the difference that "NO" is indicated between code designation and code number. With the C function 18 switched on, the negative sign "-" is indicated ahead of the code number. This is important for the decode program for mode 1 which is made available at the same time. The negative sign indicates that the decode program under the same code number is adjusted to the inverted code.

The code checked in the single-code analysis is selected either by selecting the code number with the aid of the SELECT key 10 or by stepping with the STEP keys 23. After pressing the yellow SELECT key, the imprinted yellow numbers are valid for the following two keyboard entries. During this entry the LED in the SELECT key lights. When pressing the SELECT key again before the entry is completed, the digital entry is aborted and the LED switched off. The two-digit numbers from 00 to 79 are reserved for the code numbers and from 80 to 99 for additional functions which can be defined by the user. After selection of the code number a code analysis is immediately carried out with the 1024-bit code block which was completed last, and the result is indicated. If at the beginning of the measurement 1024 bits have not yet been collected, only the code number is indicated and the analysis is carried out with the selected program after the 1024-bit block is complete. The analysis is repeated after each complete 1024-bit block. If a code number is selected which is not used, there is no indication. The selection of the code number by means of the SELECT function is independent of the mode. The code inversion by means of the C function is however only effective in mode 2 in conjunction with the "NO" indication.

With the aid of the STEP keys the individual codes can be checked in mode 2 in the sequence used in mode 0. The right key selects the following, the left key the preceding code. The stepped switching functions only if the code number selected last is really used in the GA 082. It may happen, for instance, that a code number used in the user program area connot be accessed any more after switching off the user EPROMs and switching by means of the STEP keys has no effect.

The Baudot code is a special case in the code analysis. As already described in section 2.4.5, a Baudot check is made together with the first determination of the baud rate. The code analysis relies on this check and only indicates the Baudot code and makes available the decode program required in mode 1. After calling up the code No. N07 it is not necessary to wait for this analysis until the first 1024-bit block has been completed.

2.6.3 Output of Clear Text in Mode 1

When selecting a coding method by means of a search run in mode 0, single-code analysis in mode 2 or by means of the SELECT function, decode programs, if any, are also made available. In mode 1 the signal is then decoded according to the selected code and the clear text is read out in running mode on the ANALYSIS display 8. If the PRINT function 12 has been enabled, the text is output.

The standard analysis of the GA 082 already includes the CCITT alphabets No. 2, 3 and 5 which occur in the decode programs for the codes with the code numbers N07 to N10 listed in Table 9. For the text output the alphabets No. 2 and 3 are converted into alphabet No. 5 which is identical with the ASCII code.

2.6.4 Periodicity Check of the Code

In the standard analysis (see Table 9) the period program N78 comes in the last but one place. If no code is recognized at all, a check is made for periodically recurring bits. Periods of 2 to 64 bits are checked. As soon as a periodically occurring bit is detected, the immediate vicinity is also checked and the result is indicated in the following format:

PERIOD = aa bbbb

where

aa = period length in bit

bbbb = MARK for periodic MARK bit
SPAC for periodic space bit
ASY for periodic change in mark/space
-ASY for periodic change in space/mark
IDLE for periodic repetition of all bits.

2.6.5 Code Statistics

The statistics program with the number N79, which always yields a result, takes the last place in the analysis programs. The display format is

M/S = ccc L = dddBIT

with the floating-point numbers ccc and ddd. The statistics is made for every 1024 bits. The first number ccc shows the mark/space ratio. This is obtained from the number of mark bits (logic 1) divided by the number of space bits (logic 0). The second number ddd is the average number of bits in a signal interval. It is determined by the number of status changes of the signal and is calculated from 1024 divided by the number of changes from 0 to 1 and from 1 to 0.

For a 1:6 idle signal the following statistics is obtained:

M/S = .16 L = 3.5

With statistical methods using a statistical scrambling of the bits very accurate values have been obtained, as for instance:

M/S = 1.0 L = 2.0

2.6.6 Idle Signals

For the sequence of the code analysis it is essential to check the idle signals first, since otherwise there might easily be misinterpretations. An IDLE 1:1 signal may for instance also be interpreted as ASY-ASCI. The following idle signals are therefore considered in the standard analysis:

STOP-MOD N00: There is a permanent mark or space condition.

IDLE 1:1 N01: A squarewave signal with alternately one mark and one space.

IDLE 1:6 N02: An idle signal with alternately one mark and six spaces.

IDLE 14 N04: A period of 14 bits is exactly repeated.

IDLE 28 N05: A period of 28 bits is continuously repeated.

IDLE 56 N06: A period of 56 bits is continuously repeated.

2.6.7 Baudot Code

The Baudot code designated "BAUDOT N07" is the most widely used code in telegraphy. It is used for handling the data traffic to and from the teletype. It is an asynchronous code, i.e. each character can be sent by itself at any time. The code structure is shown in Fig. 2-11.

Each character starts with a start bit with space polarity and ends with a 1.5 stop bit with mark polarity. The next character can directly follow. As explained in section 2.4.5, the 1.5 stop bit is counted as 1 bit so that the Baudot character has only a length of 7 bits for the code analysis. A continuous code transmission has the following structure:

.....10xxxxx10xxxxx10xxxxx10xxxxx10xxxxx1.....

It is characterized by the 7-bit spacing between the 1-to-0 transitions. The five data bits are formed according to the CCITT alphabet No. 2 which is shown in Table 10.

Table 10 CCITT alphabets No. 2 and 3

Letters	Figures	No.2 5 bits 1 2 3 4 5	No. 3 7 bits 1 2 3 4 5 6 7
A	-	1 1 0 0 0	0 0 1 1 0 1 0
B	?	1 0 0 1 1	0 0 1 1 0 0 1
C	:	0 1 1 1 0	1 0 0 1 1 0 0
D	Who are you?	1 0 0 1 0	0 0 1 1 1 0 0
E	3	1 0 0 0 0	0 1 1 1 0 0 0
F		1 0 1 1 0	0 0 1 0 0 1 1
G		0 1 0 1 1	1 1 0 0 0 0 1
H		0 0 1 0 1	1 0 1 0 0 1 0
I	8	0 1 1 0 0	1 1 1 0 0 0 0
J	Bell	1 1 0 1 0	0 1 0 0 0 1 1
K	(	1 1 1 1 0	0 0 0 1 0 1 1
L	)	0 1 0 0 1	1 1 0 0 0 1 0
M	.	0 0 1 1 1	1 0 1 0 0 0 1
N	,	0 0 1 1 0	1 0 1 0 1 0 0
O	9	0 0 0 1 1	1 0 0 0 1 1 0
P	0	0 1 1 0 1	1 0 0 1 0 1 0
Q	1	1 1 1 0 1	0 0 0 1 1 0 1
R	4	0 1 0 1 0	1 1 0 0 1 0 0
S	'	1 0 1 0 0	0 1 0 1 0 1 0
T	5	0 0 0 0 1	1 0 0 0 1 0 1
U	7	1 1 1 0 0	0 1 1 0 0 1 0
V	=	0 1 1 1 1	1 0 0 1 0 0 1
W	2	1 1 0 0 1	0 1 0 0 1 0 1
X	/	1 0 1 1 1	0 0 1 0 1 1 0
Y	6	1 0 1 0 1	0 0 1 0 1 0 1
Z	+	1 0 0 0 1	0 1 1 0 0 0 1
Carriage return		0 0 0 1 0	1 0 0 0 0 1 1
Line feed		0 1 0 0 0	1 0 1 1 0 0 0
Figures		1 1 0 1 1	0 1 0 0 1 1 0
Letters		1 1 1 1 1	0 0 0 1 1 1 0
Space		0 0 1 0 0	1 1 0 1 0 0 0
blank		0 0 0 0 0	0 0 0 0 1 1 1
Repetition request charcter RQ			0 1 1 0 1 0 0
Idle character α			0 1 0 1 0 0 1
Idle character β			0 1 0 1 1 0 0

2.6.8 ASCII Code

The ASCII code designated "ASY-ASCI N10" is used for the serial interfaces of visual display unit. It is certainly the most frequently used coding method; it is however hardly used in short-wave transmissions. The structure of the asynchronous ASCII character is shown in Fig. 2-12. Each character can be sent by itself.

A parity bit which complements the number of the 1s to an even number, is added to the 7 data bits. Thus at least 10 bits are required for one character. With continuous transmission the 1-to-0 transitions occur every 10 bits, so that the following structure is obtained:

...10xxxxxxxp10xxxxxxxp10xxxxxxxp10xxxxxxxp10.....

Table 11 shows the CCITT alphabet No. 5 which is identical with the ASCII code. The characters shown in brackets are the 9 deviations in the German version. With serial transmission care should be taken that the least-significant bit is sent first.

Table 11 CCITT-Alphabet No.5 (ASCII code)

				b_7	0	0	0	0	1	1	1	1
				b_6	0	0	1	1	0	0	1	1
				b_5	0	1	0	1	0	1	0	1
				Column	0	1	2	3	4	5	6	7
b_1	b_2	b_3	b_4	Line								
0	0	0	0	0	NUL		SP	0	@ [§]	P	`	p
1	0	0	0	1			!	1	A	Q	a	q
0	1	0	0	2			"	2	B	R	b	r
1	1	0	0	3			#	3	C	S	c	s
0	0	1	0	4			¤ [$]	4	D	T	d	t
1	0	1	0	5			%	5	E	U	e	u
0	1	1	0	6			&	6	F	V	f	v
1	1	1	0	7			'	7	G	W	g	w
0	0	0	1	8			(	8	H	X	h	x
1	0	0	1	9			)	9	I	Y	i	y
0	1	0	1	10	LF		*	:	J	Z	j	z
1	1	0	1	11		ESC	+	;	K	[[Ä]	k	{ [ä]
0	0	1	1	12			,		L	\ [Ö]	l	| [ö]
1	0	1	1	13	CR		-	=	M	] [Ü]	m	} [ü]
0	1	1	1	14			.		N	^	n	~ [ß]
1	1	1	1	15			/	?	O	-	o	DEL

2.6.9 ARQ Method

In shortwave telegraphy the synchronous ARQ methods (automatic request) have gained great importance. They use a 7-bit code which recognizes transmission errors. If an error occurs, a repetition request character is sent back to the information source. The 3 or 7 characters sent last are then repeated with a preceding repetition request character.

Several 7-bit codings are in use. There is often also a time-division multiplex of several channels as well as subchannels, resulting in a great variety of different methods. Multiplex periods of 28 and 56 bits are most frequently used. Since the channels are very often in idle condition, the code structure can easily be recognized with the superimposed display in modes 6 to 9.

The methods designated "ARQ-28 N08" and "ARQ-56 N09" use the CCITT code No. 3 which is shown in Table 10 together with the Baudot code. All characters have a mark-to-space ratio of 3:4. In addition to the 32 characters, which are allocated to alphabet No. 2, there are another 3 characters which are required for the repetition request (RQ), continuous start (α) and continuous stop (β) polarity. Single-bit errors can be recognized with this code, since the characters differ from each other by at least 2 bits.

In the ARQ multiplex method individual characters are inverted for the identification of individual channels according to the CCIR Recommendation 342-2 so that a characteristic structure is obtained, which enables unambiguous synchronization of the system.

The ARQ-28 method N08 recognizes a code in which every 4th character is inverted so that there is a cycle over 28 bits. The ARQ-56 method N09 has a 56-bit cycle in which every 8th character is inverted.

When the text is output in mode 1, all characters are successively output, irrespective whether they are from one or from several channels.

2.6.10 User Programs

The great number of teletype transmission methods presently used and the employment of new methods call for an analysis concept, which can be adapted to the present and future requirements of the user. The program structure of the code analysis is such as to permit adding of further analysis programs without difficulties. A large program area is reserved for this purpose in the GA 082. The EPROM locations A and B on the internal microprocessor board (see Fig. 2-3) or in the program unit plugged into the rear panel input 28, are provided for accommodating the user programs. A change of the programs is greatly facilitated when using the program unit. It enables rapid adaptation to the special requirements of a particular operator's position.

After switching on, the GA 082 checks automatically whether the user programs are present. Even during operation the user programs can be switched off by SELECT - X6 and switched on by SELECT - X7.

If the user programs are on, they determine the execution of the code analysis. The arrangement of the program vectors at the beginning of the program area determines the number, sequence and code numbers of the programs used for the analysis.

There are three different types of program:

1. Program for code analysis in mode 0 or mode 2 are called up every 1024 bits.
2. Programs for decoding and text output in mode 1 are called up every 8 bits.
3. Programs with the numbers 80 to 99 are provided for additional functions. They are executed immediately upon entry of the number.

Rohde & Schwarz will offer general-purpose program modules adapted to the latest telegraphy codes. Special programs can be prepared as required by the user. Users with program writing capability the microprocessor 8086 may obtain on request a detailed description of the software interfaces for the code analysis.

2.7 Output Formats for IEC and V.24 Interfaces

2.7.1 Output of Measured Data

For the output of the measured data the IEC or V.24 interface is available. The interface is selected by means of the IEC/V.24 switch 29 on the rear panel. The switch is only operative after the GA 082 has been switched on and any change becomes only effective if the GA 082 is switched on and off again. In position 1 the output is switched to the IEC bus, in position 0 to the V.24 output. If the IEC bus is only provided for output to another IEC-bus device, the TON switch (talk only) must be set to position 1.

Table 12 shows the data and code outputs selectable by means of the PRINT function 12 and the auxiliary functions B 19 and C 18 in the individual modes. The measured data displayed on the front panel are output in mode 0 and mode 2 if the PRINT function has been enabled.

Table 12 Data and code output

MODE	PRINT	PRINT-B	PRINT-C	PRINT-B-C
0	Measured data	Code 1 bit/character	Code 4 bits/character	Code 8 bits/character
1	Text	C carries out case shift in Baudot code		
2	Measured data	Code 1 bit/character	Code 4 bits/character	Code 8 bits/character
3				
4				
5				
6 7 8 9	Contents of refresh memory is output once when switching on PRINT function. B and C are irrelevant.			

After the first determination of the baud rate once a header and then the first measured value of centre frequency, shift and baud rate are furnished. The format is in Table 13.

Table 13 Output format for measured data

FREQ	SHIFT	Q	S	MIN	BAUD	ANALYSE	
1.79	1199	0	0		75.0		
1.79	1199	0	0		75.0003	IDLE 1:1	NO1
1.79	1199	0	0		75.00034	IDLE 1:1	NO1
1.79	1199	0	0		75.00033	IDLE 1:1	NO1
1.79	1199	0	0		75.00033	IDLE 1:1	NO1
1.79	1199	0	0	1	75.00033	IDLE 1:1	NO1

A new line is output after every 1024 bits upon completion of the code analysis. In mode 2 the measured data are additionally output also after each code analysis which is carried out after calling up a program by means of the SELECT function 10 or by stepped switching with the STEP keys 23.

In the two columns Q and S the DEMOD indication 2 and the SYCN indication 5 are evaluated. Q determines the quality of the frequency-modulated signal and evaluates in how far the momentary frequency is in the vicinity of the frequency lines. S shows whether the SYNC indication is mainly in the centre. With good signals Q and S have the value 0. If Q and S are not 0, the measured results should be regarded critically. Q and S may assume values up to 7. This will however only happen if the FIX function 21 has been selected, since the poor signal conditions would otherwise cause a new start.

2.7.2 Output of Code Bits

After determination of the baud rate or bit rate the internal baud rate clock in the GA 082 is synchronized to the edges of the signal. From sampling the signal status in the centre, the binary code is derived which is first stored in 8-bit groups in the code memory. There are various possibilities of directly outputting the signal code after every 8 bits collected.

Table 12 shows the various possibilities of code output for the different modes. Direct output of the code bits is possible in the modes 0, 2, 3, 4 and 5. For the output the IEC/V.24 switch 29 on the rear panel enables selection of IEC bus or V.24 interface. In both cases the output is in bytes of 8 bits, with parallel transmission via the IEC bus and serial transmission via the V.24 interface with an additional start bit and a stop bit.

The most efficient output is achieved if 8 code bits are also included in each output byte. For this purpose PRINT-B-C must be selected. This output format is particularly suitable for transmitting the code to other data processing systems. It is however not suitable at all for direct printout of the code bits on a printer or display on a visual data unit, because these facilities use the ASCII code shown in Table 11, which has a character set of about 96 characters, whereas for the 8-bit display a character set of 256 characters would be required.

The most comprehensive output is at the same time the easiest for the observer. It is made with the aid of the PRINT-B function and for each code bit a 8-bit ASCII character is produced, in which every 8th bit = 0. For the signal status mark and space a 1 or 0 is printed out for each bit. The line lenght LEN of the printout can be varied in modes 2 to 5 with the aid of the LENGTH keys 22. This output format puts a heavy load on the printer, since for 200 baud also 200 characters/sec must be printed out. The internal buffer for the data output has a capacity of 1024 characters. This FIFO memory (first in first out) buffers the rapid data to be outputted to a slow printer. If the memory is full, the data output is stopped until the printer has emptied the memory. After termination with a "-" character the data output is continued in a new line with the now current data. Thus even a slow printer can print out coherent code blocks with a length of more than 1000 bits.

With the PRINT-C function a more rapid output of 4 bits per ASCII character can be selected, in which case the 4 code bits are interpreted as a hexadecimal number and output as ASCII character.

Table 14 Hexadecimal notation

Code bits				Printed out	ASCII code in
b_4	b_3	b_2	b_1	hexadecimal number	hexadecimal notation
0	0	0	0	0	30
0	0	0	1	1	31
0	0	1	0	2	32
0	0	1	1	3	33
0	1	0	0	4	34
0	1	0	1	5	35
0	1	1	0	6	36
0	1	1	1	7	37
1	0	0	0	8	38
1	0	0	1	9	39
1	0	1	0	A	41
1	0	1	1	B	42
1	1	0	0	C	43
1	1	0	1	D	44
1	1	1	0	E	45
1	1	1	1	F	46

Table 14 shows the correlation between code bits, printed out hexadecimal number and output ASCII character. The 8 bits of the ASCII code are shown in hexadecimal notation. It should be noted that only for the figures 0 to 9 the 4 least-significant bits of the ASCII character agree with the 4 code bits. For joining up the 4-bit groups, it should be noted that the least-significant bit appears first in each group, so that for instance the following printout is obtained:

Binary:	1011	0011	1010	0011	0101	1100	1000
Hexadecimal:	D	C	5	C	A	3	1

2.7.3 Output of Code Lines in Mode 6 to 9

In modes 6 to 9 the PRINT function, when switched on, has just one task, i.e. to read out once the contents of the refresh memory. In the refresh memory the code bits are either entered currently in mode 6 or 7 (see 2.5.2) or from a fixed memory area in mode 8 or 9 (see 2.5.3) and displayed on the CODE display 7 in rapid succession.

For the code output the modes 8 or 9 are of particular interest, since they permit arrangement of the code bits in the desired pattern. For this purpose a signal length of 8192 bits can be retained in the code memory. The starting point of the code output can be varied by means of the STEP keys 23 and the line length LEN by means of the LENGTH keys 22. After a length of 48 bits the lines are terminated and a "-" character is printed out at the line end. By shifting the starting point with the aid of the STEP keys, all bits of the code memory can successively output in a clear format. For simple counting the STEP counter can be reset at the beginning of each code block by pressing both STEP keys simultaneously. To this effect the value that is to become zero must be indicated with one key being depressed. By additionally pressing the second key, the reset is then carried out.

For each new output the PRINT function must be switched off and on again.

2.8 Remote Control

The GA 082 can be simultaneously controlled from 3 different places. In addition to the keyboard entry on the front panel, the control commands can also be entered via the IEC bus or via the V.24 interface. The ASCII characters required for the remote control are identical for both interfaces. At the V.24 interface the 8-bit characters are entered serially with an additional start bit and stop bit (see 2.8.2). At the IEC bus the 8-bit characters are entered in parallel; in this case the GA 082 must however first be addressed by a controller (see 2.8.3).

2.8.1 Remote Control Commands

The remote control commands are shown in Table 15 together with the keyboard operation. The horizontal line above the key designation means that the key function is switched off (LED does not light). Each command is only processed when the prescribed number of characters has been entered. Each command begins with a letter. A new letter before completion of the numerical entry causes an abortion of the current command entry and start of a new command. Numbers entered after completion of the numerical entry are ignored. The individual commands can be successively linked up without any further delimiters. With the numerical sequence

D 1 C 1 T 1

the same is achieved as with keys

DEMOD - C - TEST,

i.e. the demodulator and the 75-baud test are switched on. The remote control is executed in the same way as the operation via the front-panel keyboard. For presetting the measured values such as baud rate, frequency, shift and line length direct numerical values can however be entered.

Table 15 Remote control commands

Command	Function	Keys
AØ	Auxiliary function A off	$\overline{\text{A}}$
A1	Auxiliary function A on	A
BØ	Auxiliary function B off	$\overline{\text{B}}$
B1	Auxiliary function B on	B
CØ	Auxiliary function C off	$\overline{\text{C}}$
C1	Auxiliary function C on	C
DØ	Demodulator off	$\overline{\text{DEMOD}}$
D1	Demodulator on	DEMOD
EØ	User EPROM off	SELECT-X6
E1	User EPROM on	SELECT-X7
FØ	FIX function off	$\overline{\text{FIX}}$
F1	FIX function on	FIX
Gnnnnnn	Entry of baud rate, decimal point after 4th digit	RATE ↑↓
Hnnnn	Entry of shift in Hz	SHIFT ↑↓
Innn	Entry of frequency in kHz, decimal point after 1st digit	
JØ	AUTOFEED off	
J1	AUTOFEED on	
KØ	CONST function off	$\overline{\text{CONST}}$
K1	CONST function on	CONST
Lnnn	Entry of line length	LENGTH ↑↓
MØ	Mode = 0	MODE ↑↓
M1	Mode = 1	
M2	Mode = 2	
Nnn	Entry of code number	SELECT-n-n
Onn	Same as Nnn	
PØ	PRINT function off	$\overline{\text{PRINT}}$
P1	PRINT function on	PRINT
QØ	Bit clock off	SELECT-X8
Q1	Bit clock on	SELECT-X9
R	Prints out status	
S	START function on	START

Command	Function	Keys
TØ	TEST function off	$\overline{\text{TEST}}$
T1	TEST function on	TEST
UØ	Channel 1 switched on	$\overline{\text{CHAN1/2}}$
U1	Channel 2 switched on	CHAN1/2
VØ	- STEP } for CONST and for	STEP ↓
V1	+ STEP } code No. in mode 2	STEP ↑
WØ	SHIFT indication switched on	$\overline{\text{FREQ/SHIFT}}$
W1	FREQ indication switched on	FREQ/SHIFT
XØ	Front panel switched off	SELECT-XØ
X1	F6 switched on	SELECT-X1
YØ	RATE LOOP on	SELECT-X4
Y1	RATE LOOP off	SELECT-X5
ZØ	PHASE LOOP on	SELECT-X2
Z1	PHASE LOOP off	SELECT-X3

The momentary setting of the equipment functions can be called up by means of the R command. The equipment status is then printed out in the format shown in Table 16. The letters in the first row together with the numbers in the second row indicate which functions are switched on. The same characters are used as for the remote control shown in Table 15. The example given in Table 16 states that the demodulator, the 75-baud test function, autofeed and the user EPROMs are switched on.

Table 16 Response to R command

S	N	P	U	F	K	Y	Z	T	D	W	C	A	B	J	E
0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1

MODE = 0 CONST = 5

2.8.2 Remote Control via V.24 Interface

Connection to the serial interface to CCITT V.24/V.28 and EIA RS-232-C standards is described in section 2.2.6. The input and output via this interface is made by means of asynchronous characters with 8 data bits. Fig. 2-13 shows the format of these characters. For the data output the potential -12 V is used for mark (logic 1) and +12 V for space (logic 0). For the input, potentials above +2.5 V are considered as space and below +1 V as mark. The input impedance is approximately 4 kΩ. The permissible input voltages are within ±30 V.

The remote control commands according to Table 15 are entered in 7-bit ASCII code (see Table 11). The bits are sent in ascending order, the 8th bit must be 0. The input rate must be matched to the baud rate selected in the GA 082 (see Table 6). The data output is effected at the same rate and in the same 8-bit format. The ASCII characters are also output without parity, i.e. the 8th bit is 0.

2.8.3 Remote Control via IEC Bus

The IEC bus is connected via the 24-way Amphenol connector 30. The IEC-bus devices are interconnected via standard cables. The pin assignment is shown in Table 17. There are 8 data lines DI01 to 8 for 8-bit parallel transmission. For the data acceptance the three handshake lines DAV, NRFD and NDAC are required. There are also the five control lines EOI, IFC, SRQ, ATN and REN. The REN line is not used in the GA 082. All lines are set active to 0 V for the logic 1 state. For logic 0 the lines are pulled high to about 3 V by the terminations incorporated in each device.

Table 17 Pin assignment of IEC bus

Pin	Signal	
1	DIO1	Data Input/Output
2	DIO2	Data Input/Output
3	DIO3	Data Input/Output
4	DIO4	Data Input/Output
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready For Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	
13	DIO5	Data Input/Output
14	DIO6	Data Input/Output
15	DIO7	Data Input/Output
16	DIO8	Data Input/Output
17	REN	Remote Enable
18	Ground to 6	
19	Ground to 7	
20	Ground to 8	
21	Ground to 9	
22	Ground to 10	
23	Ground to 11	
24	Ground	

For operation of the IEC bus a controller is usually required, which allocates the talker and listener function to the individual devices. The controller is not required where only data are to be output (e.g. to a printer with IEC-bus interface). In addition to the IEC/V.24 switch the TON switch 29 (talk only) on the rear panel must also be set to 1. In this case the GA 082 is permanently set as talker and can output data without the aid of a controller to an IEC-bus device having the LON function (listen only), i.e. which acts permanently as listener.

Prior to a data transmission the device must be addressed as talker or as listener by the controller with the aid of interface commands. The address of the GA 082 is adjusted to a value between 0 and 30 by means of the address switches A1 to A5 29 having a value of 1, 2, 4, 8, 16. The address switches are only read in after the GA 082 has been switched on. Each change becomes only effective when the GA 082 is switched off and on again.

The byte applied to the data lines is understood as interface command by the connected devices if at the same time the ATN line (attention) is active (≈ 0 V). According to the IEC 625 standard, the commands with 7 data bits, which can also be represented as ASCII characters, are divided into various groups. In hexadecimal notation these are the following groups:

00_H to $0F_H$	Addressed commands are only received by previously addressed listeners.
10_H to $1F_H$	Universal commands are observed by all devices connected.
20_H to $3E_H$	MLA (my listen address). Device is addressed as listener if the last five command bits agree with the setting of the address switches A1 to A5.
$3F_H$	UNL (unlisten). All listeners are unaddressed.
40_H to $5E_H$	MTA (my talk address). Device is addressed as talker if the last five command bits agree with the setting of the address switches A1 to A5.
$5F_H$	UNT (untalk). All talkers are unaddressed.
60_H to $7E_H$	Secondary commands are only accepted by a device if it has been previously addressed by a primary command from one of the other groups.

In the GA 082 only that part of these interface commands is used which is listed in Table 18.

Table 18 IEC-bus interface commands for GA 082

Hex code	Symbol	Function
05	PPC	Parallel poll configure. Setting up PPE and PPD.
15	PPU	Parallel poll unconfigure. PPE and PPD is disabled for all devices.
18	SPE	Serial poll enable. Devices are set up for serial poll.
19	SPD	Serial poll disable. Serial poll condition is switched off for all devices.
20 to 3E	MLA	My listen address. 31 listener addresses.
3F	UNL	Unlisten. All listeners are switched off.
40 to 5E	MTA	My talk address. 31 talker addresses.
5F	UNT	Untalk. The talker is switched off.
68 to 6F	PPE	Parallel poll enable. One of the 8 data lines is allocated to parallel poll.
70 to 7F	PPD	Parallel poll disable. Parallel poll is switched off.

The handshake with the lines DAV, NRFD and NDAC used for the data transfer is such that several listeners may be connected to one talker, the transmission speed being determined by the slowest listener. NDAC is active (≈ 0 V = logic 1) as soon as a listener is addressed. The talker activates DAV after the data are made ready on the data lines DIO1 to DIO8. The listener activates NRFD, accepts the data and enables NDAC (≈ 3 V = logic 0). Thereupon the talker enables DAV and the listener activates NDAC. As soon as the listener is ready for the next data acceptance, it enables NRFD again. The listener may only enable NDAC if NRFD is active. Simultaneous enabling of both lines is signalled as error by the talker, since it assumes that no listener is connected.

The data input for remote control of the GA 082 via the IEC bus is such that first the GA 082 is addressed as listener and then the data input is carried out according to the command list in Table 14. Finally, the GA 082 is unaddressed by the UNL interface command or by the IFC line. A special end character is not required at the end of the character string. The EOI line need also not be activated at the end. In Table 19 the command sequence DEMOD-C-TEST for the device address 0 is shown as an example. Each line represents the transmission of a byte, with a cycle of the handshake described above being carried out in parallel. Lines 2 to 7 transfer the character string for the GA 082 control.

Table 19 Example of remote control via IEC bus

Line	DIO Hex code	Active control lines	Function
1	20	ATN	MLA
2	44		D
3	31		1
4	43		C
5	31		1
6	54		T
7	31		1
8	3F	ATN	UNL

The data output via the IEC bus is somewhat more complicated since the GA 082 must first inform the controller if its request for data output. There are two possibilities which the GA 082 can use: serial poll and parallel poll.

With serial poll the GA 082 activates the SRQ line if data are ready for output. The controller must now determine which device has activated the SRQ line. An example for the serial poll is shown in Table 20. Line 1 shows that the GA 082 has activated the SRQ line. The controller then initates the serial poll by the SPE command (serial poll enable) shown in line 2.

Table 20 Example of serial poll

Line	DIO (hex) Controller	GA 082	Active control lines	Function
1			SRQ	Service request
2	18		SRQ, ATN	SPE
3	41		SRQ, ATN	MTA (other device)
4		(00)	SRQ	Status (other device)
5	40		SRQ, ATN	MTA
6		40		Status
7	19		ATN	SPD
8		44		D
9		41		A
10		54		T
11		41	EOI	A
12	5F		ATN	UNT

The devices connected to the IEC bus are now successively addressed as talker and answer with their status word. The 7th bit of the status word of the calling device is set to 1. The other bits may contain further information on the device status. In line 3 for instance another device is addressed first, which has not activated the SRQ line. After disabling of the ATN line, this device answers with a status word in which DIO7 = 0. Finally the calling device is addressed in line 5 with its address 0, which then immediately enables the activated SRQ line. In line 6 this device also signals the status with DIO7 = 1. Since the controller has now found the calling device, it terminates in line 7 the serial poll by the universal command SPD (serial poll disable). The device remains addressed after the serial poll and can now carry out the data output in lines 8 to 11. The letters DATA have been selected in the above example. With the last byte output the EOI line (end or identify) is activated in line 11. The controller

can then disable the talker function of the device by the UNT command (untalk) given in line 12. This can also be done by addressing another talker or by activating the IFC line (interface clear).

The GA 082 makes practically no use of furnishing information on the device status by means of the status word. There are only two different status words:

40_H for desired data output

FF_H for error signal if the GA 082 has been addressed as talker and cannot find a listener.

The time-consuming serial poll for the calling device can be cut down by parallel poll. In this case one of the 8 data lines is allocated to each device which it can use for announcing data output if the EOI and the ATN line are both active. Table 21 shows the example of a parallel poll.

Table 21 Example of parallel poll

Line	DIO (hex) Controller	GA 082	Active control lines	Function
1	20		ATN	MLA
2	05		ATN	PPC
3	68		ATN	PPE
4	3F		ATN	UNL
5		01	ATN, EOI	Parallel Poll
6	40		ATN	MTA
7		44		D
8		41		A
9		54		T
10		41	EOI	A
11	5F		ATN	UNT
12	20		ATN	MLA
13	05		ATN	PPC
14	70		ATN	PPD
15	3F		ATN	UNL

For setting up the parallel poll a data line is allocated to each device when the IEC bus is initialized. In lines 1 to 4 for instance the data line 1 is allocated to the device with the address 0. A similar command sequence must be carried out for all devices so that they can participate in the parallel poll. Different are line 1 with the device address contained in the last 5 data bits, and line 3 with the data line allocation contained in the last 3 data bits.

It is now the task of the controller to carry out the parallel poll either regularly or upon an SRQ request. In line 5 of the example shown above the data line DI01 is activated by the GA 082 in parallel poll mode with the aid of the active lines ATN and EOI if data are ready for output. The controller can thus directly recognize which device wishes to output data and can allow it to talk in line 6. The data output can immediately begin and is terminated by the EOI line activated with the last character. Line 11 shows the unaddressing. This sequence can be repeated as often as desired. If a device is to be excluded from the parallel poll method, this can be done with the command sequence shown in lines 12 to 15 for the device with the address 0. Parallel poll can be simultaneously disabled for all devices by means of the universal command PPU (parallel poll unconfigure). With parallel poll switched on, the data line allocated to the device is noted in the GA 082 only for the data output and not for an error signal. In any case the SRQ line is additionally activated for request for data output.

In the notation used in the IEC 625 standard, the following interface functions are available in the GA 082:

SH1	Source handshake
AH1	Acceptor handshake
T5	Talker function, serial poll, unaddress, tone
L3	Listener function, unaddress
SR1	Serial poll
PP1	Parallel poll

2.8.4 Program Example for IEC Bus linked to PPC/PUC

The Process Controllers PPC and PUC supplied by Rohde & Schwarz enable convenient operation of an IEC-bus system in which case user need not familiarize himself with all the details described in the preceding section. A set of clear IEC bus commands is available for this purpose. In the following a few typical examples are given for data input, data output, serial poll and parallel poll.

Data input:

```
.
.
.
100  INPUT A$
110  IEC OUT X, A$: REM X = DEVICE ADDRESS
120  GO TO 100
```

Data output:

```
.
.
.
100  IEC IN X, A$: REM X = DEVICE ADDRESS
110  PRINT A$
```

Data output in talk only mode:

```
.
.
.
100  IEC $ IN A$
110  PRINT A$
120  GO TO 100
```

Data output with parallel poll:

```
.
.
.
100  IEC LAD Ø: REM Ø = GA 082 ADDRESS
110  IEC PPC
120  IEC PPE 12: REM 1 = SENSE BIT, 2 = LINE
130  IEC UNL
140  IEC PPL A %
150  PRINT A %
```

```
160  IF A % = Ø THEN 130
170  IEC IN Ø, A$
180  PRINT A$
190  GO TO 140
```

2.9 Built-in Test Facilities

Proper functioning of the GA 082 can be checked with the aid of the built-in test facilities. The tests start with the RAMs and ROMs and end up in the 75-baud test which includes almost the entire GA 082. The signature analysis is provided for further troubleshooting down to component level.

2.9.1 Testing the RAMs and EPROMs

After switching on the GA 082, a test is carried out first which is based on the assumption that at least a few modules of the microprocessor system are properly functioning. Therefore a small test program is executed first for checking the RAMs. Bits with different polarity are alternately written into each cell of the RAM and read. In the case of errors the following information is read out on the 16-digit alphanumeric display 8:

-H-L-RAM ERROR

The letters H or L show which of the two RAM modules, whose location is shown in Fig. 2-3, is faulty.

After detection of a RAM error the RAM test is started from the beginning again. The processor stops in this test phase until the error is eliminated.

After successful completion of the RAM test the front-panel display is blanked and an EPROM test is carried out. Only the EPROMs C, D, E and F (see Fig. 2-3) belonging to the basic equipment of the GA 082 are checked in this test. In each EPROM the cross-sum must be identical with the check sum stored in the EPROM. In the case of an error the faulty EPROM detected first is indicated in the following format:

--C--ROM EPROM

Instead of C there may also be a D, E or F. The indication is held for about 1.5 sec and then the program is continued as if there were no errors.

At the end of the test phase the system version stored in the EPROMs C and D are compared and in case of agreement

SYSTEM2.0 USER12

is indicated. If the user EPROMs A and B are fitted, the system number is also compared and indicated after USER. This indication is held for about 1.5 sec until the GA 082 can start up operation.

The EPROM test for all EPROMs fitted is repeatedly carried out during operation after the baud-rate control loop has been switched on, and in case of a fault an error indication is briefly superimposed on the current display. The front-panel operation can be switched off by means of SELECT X0 so that a steady error indication is obtained.

2.9.2 Signature Analysis

The signature program can be switched on by means of the NMI switch of the S1 switches on the microprocessor board (see Fig. 2-3). With the GA 082 ready to operate, the NMI switch must be set from 0 to position 1. In about 370 µsec the program is looped through all data paths accessible from the microprocessor without the program being influenced by the data. A characteristic pattern is obtained on the front-panel displays.

With the aid of the signal characteristics at the various modules, defective components can be located by comparing these characteristics with the nominal curves. A useful aid is provided in this case by signature analyzers of various makes, which determine a 3- or 4-digit hexadecimal number for each test point. By comparing the signature number of a properly functioning euqipment with that of the faulty equipment, the error source can be located. The signature analyzers receive the necessary trigger signals from the following pins of the 8086-CPU on the microprocessor board (see Fig. 2-3).

Start and stop:	pins 35 and 36	(200 ns pulses)
Clock:	pin 19	(5 MHz)

The signature analyzers determine the signature number at the test point by gating the clearly defined signal characteristic between start and stop with an also clearly defined noisy signal. The signature analysis is an important aid in repairing a defective equipment for troubleshooting down to component level.

2.9.3 Checking the Front Panel

The front-panel indicators are checked by switching on the TEST function 16 (DEMOD remains switched off). All displays are successively driven by their character set in 1/2-sec clock mode.

For checking the function keys are their LEDs, each function is switched on and off by pressing the keys. The LED of the START key 9 should be switched off when the START key is pressed with the FIX function 21 being enabled. The variation keys 22 to 26 can be tested with the aid of the FIX-DEMOD function. By alternately pressing these two associated keys, the indicated parameters can be increased and reduced. For checking STEP 23 and LENGTH 22 mode 4 must be switched on.

2.9.4 Performance Check with 75-baud Signal

The most comprehensive performance check is carried out with the aid of the internal squarewave signal of 75 baud. The only signal paths which are not covered by this test are the input circuit for demodulated signals shown in Fig. 2-4, als well as the input and mixer for IF/AF signals. These inputs can only be checked by feeding in external signals.

The test signal is switched on by means of the DEMOD-C-TEST functions and yields the following measured values:

SHIFT: 1199 Hz
FREQ: 1.79 kHz (switchover with SHIFT/FREQ key)
RATE: 75.000... baud
ANALYSIS: IDLE 1:1 N01 for mode = 0

The test signal is derived from the microprocessor cyrstal, which can be tuned by means of the trimmer C38 on the microprocessor board. When using the internal standard frequency for determining the baud rate, this must be derived from crystal G1 on the interface board, which is adjusted with the aid of trimmer P1 by comparing the frequency measured at D17.9 with an accurate frequency standard. If the baud rate indication is above 50 in the last two digits, it is recommended to adjust the microprocessor crystal using C38.

3. Maintenance

3.1 Required Measuring Equipment

1 digital multimeter
1 function generator 1 Hz to 1.5 MHz
1 frequency counter 1 x 10^{-8} for 1 Hz to 10 MHz
1 oscillocope with 2 channels
1 printer with V.24 interface
1 ASCII keyboard with V.24 interface
1 IEC-bus controller

3.2 Checking the Rated Specifications

3.2.1 Power Supply

a) Adjust the 5-V voltage to 5 ±0.05 V using R3 on the power supply board II (see Fig. 2-3). Measure the voltage on the microprocessor board at the feed points.

   Load is caused by switching on
   FIX-CONST-FREQ-DEMOD-PRINT-CHAN2-A-B-C-SELECT.

   In MODE = 5 all LEDs of the CODE display light.

b) Adjustment as in a). For switchover to different AC supply voltages use voltage selector 27. Fluctuation of AC supply voltage ±10%.

c) Check the voltage +12 V ±0.5 V at the feed points on the microprocessor board.

d) Check the voltage -12 V ±1 V at the feed points on the microprocessor board.

3.2.2 Clock Frequencies

a) Adjust the internal standard frequency using P1 on the interface board (see Fig. 2-3). Test point for 1 MHz at D17.9. Compare it with an external frequency source of 1 MHz with an error of 10^{-8} on a dual-channel ocilloscope. The first channel receives the external 1-MHz reference frequency and triggers the deflection.

The second channel is fed from the internal frequency via pin D17.9. For selection of the internal frequency standard the S1 switches are set to 0. Adjust so that the two displayed frequencies are shifted less than 1 period within 10 seconds from each other.

b) Check the selection of the frequency standard with the S1 switches:

S1.1	S1.2	Frequency selection
0	0	internal
1	0	external 1 MHz
0	1	external 5 MHz
1	1	external 10 MHz

For each external frequency applied to the EXT REF input 35 a frequency of 1 MHz must be available at D17.9 if the S1 switches are in correct position. Check the input voltage range from 85 to 1400 mV_{pp} into 1 kΩ input impedance.

c) Check the clock rate of 300 Hz at pin D10.18 of the microprocessor board after the GA 082 has been switched on. All S1 switches are set to 0 (switch closed).

d) Check baud-rate clock for V.24 interface at pin U2.9 on the microprocessor board. Use switches S1.5 to S1.8 for the adjustments. Switch on the switches successively and measure the frequency at U2.9. After each change of the switch position the GA 082 must be switched off and on again so that the new switch position will be noticed by the microprocessor.

S1 on micro-processor board 5	6	7	8	Frequency at pin U2.9
1	0	0	0	3,200 Hz
1	1	0	0	6,400 Hz
1	1	1	0	12,800 Hz
0	0	1	1	153,600 Hz

e) Adjust the mixer frequency for the IF input 32 with the aid of the switches S2.1-4 and S3.1-8 on the interface board and measure at pin D9.12.

Interface board S2 1	2	3	4	S3 1	2	3	4	5	6	7	8	Frequency at pin D9.12
1	0	0	0	0	0	0	0	0	0	0	0	360 Hz
0	1	0	0	0	0	0	0	0	0	0	0	720 Hz
0	0	1	0	0	0	0	0	0	0	0	0	1,440 Hz
0	0	0	1	0	0	0	0	0	0	0	0	2,880 Hz
0	0	0	0	1	0	0	0	0	0	0	0	5,760 Hz
0	0	0	0	0	1	0	0	0	0	0	0	11,520 Hz
0	0	0	0	0	0	1	0	0	0	0	0	23,040 Hz
0	0	0	0	0	0	0	1	0	0	0	0	46,080 Hz
0	0	0	0	0	0	0	0	1	0	0	0	92,160 Hz
0	0	0	0	0	0	0	0	0	1	0	0	184,320 Hz
0	0	0	0	0	0	0	0	0	0	1	0	368,640 Hz
0	0	0	0	0	0	0	0	0	0	0	1	737,280 Hz

3.2.3 Front Panel

a) Check the indicating elements with the aid of the TEST function. All displays are successively switched on.

b) Check the function keys and their LEDs by pressing the individual keys. After pressing the key twice, the LED is switched off again. This does not apply to the START key. If the FIX function is additionally switched on, the START LED goes out shortly after pressing the START key as soon as the baud rate is indicated.

c) Check the dual keys with the aid of FIX-DEMOD for SHIFT, RATE, MODE. The left key reduces and the right key increases the parameter indicated. Select MODE = 4 and check the STEP and LENGTH keys.

3.2.4 75-baud TEST

a) Switch on test signal by means of C - TEST. There should be the following indication:

RATE: 75 baud ±1 x 10^{-4} of reading
ANALYSIS: IDLE 1:1 NO1 for mode = 0.

If the first three digits after the decimal point of the baud rate are not zero, the microprocessor crystal must be adjusted using C38 on the microprocessor board.

b) Switch on test signal by means of C - TEST - DEMOD. There should be the following indication:

SHIFT: 1199 Hz
FREQ: 1.79 kHz (after switchover with SHIFT/FREQ key)

3.2.5 Signal Input for AF/IF Signal

a) Adjust internal mixer frequency on interface board to 90 kHz using switches S2 and S3.

S2 1 2 3 4	S3 1 2 3 4 5 6 7 8	Mixer frequency
0 0 1 1	0 0 1 0 0 0 0 0	27.36 kHz
0 1 0 1	1 1 1 1 0 0 0 0	90.00 kHz
1 1 1 0	1 1 0 0 1 1 1 1	1402.20 kHz

Switch on FIX-DEMOD-FREQ functions. Apply a frequency between 91 and 98 kHz from the function generator to the AF/IF input 32. Adjust the light dot on the DEMOD display 2 to the centre marking using the SHIFT/FREQ keys. The indicated centre frequency on the SHIFT/FREQ display 3 must correspond to the signal frequency less 90 kHz. Check the input sensitivity by increasing the input voltage from zero until the DEMOD indication remains in the range of two LEDs. This should be the case with an input voltage which is below 140 mV_{pp} into 50 Ω. Check for proper functioning in the range from 140 to 2850 mV_{pp}.

b) Adjust mixer frequency to 27.36 kHz. A signal frequency of 30 kHz should yield a FREQ indication of 2.64 kHz. Check input sensitivity of 140 mV_{pp}.

c) Adjust mixer frequency to 1402.20 kHz. A signal frequency of 1400 kHz should yield a FREQ indication of 2.20 kHz. Check input sensitivity of 140 mV_{pp}.

d) Adjust mixer frequency to zero. All switches S2 and S3 are closed. Vary the input frequency between 1 and 8 kHz; with the light dot in the centre of the DEMOD indication 2, the FREQ indication should agree with the signal frequency fed in. Check input sensitivity of 140 mV_{pp}.

3.2.6 Signal-Inputs for Demodulated Signal

a) Apply a positive squarewave signal with a mark-to-space ratio of 1:1 to the BNC socket 33. Adjust the amplitude of the squarewave to about 3 V and vary the frequency until about 100 baud is indicated. Switch on the FIX function and slightly vary the frequency until the SYNC LEDs 5 are lit up one after the other. Reduce the amplitude of the squarewave until the SYNC indication is permanently on. Check the higher potential of the squarewave signal with an oscilloscope. It should be between 1 and 1.2 V.

b) Switch off the FIX function and vary the frequency of the positive squarewave signal with 3 V amplitude in the range 2 to 9600 baud. Observe the RATE indication 4.

c) Apply a squarewave signal with 3 V amplitude and about 100 baud to Tuchel socket 34 between pin 4 and pin 6. Switch on the FIX function and vary the frequency until the SYNC LEDs are lit up

one after the other. Reduce the amplitude of the squarewave until the SYNC indication is permanently on. The amplitude should be below 3 V. Interchange the connections at pin 4 and pin 6 and repeat the sensitivity measurement.

d) Switch on CHAN2 and apply a squarewave signal between pin 3 and pin 5. Measure sensitivity as in c). Interchange the connections at pin 3 and pin 5 and repeat the sensitivity measurement.

e) Switch off the FIX function and check the measurement range from 2 to 9600 baud.

3.2.7 Signal Outputs

a) Switch on C - TEST. Switch on the bit clock by means of SELECT-X-9. Connect an oscilloscope to pin 2 and pin 7 (ground) of the Tuchel socket 34 and observe the displayed voltage characteristic. There should be 100-µs positive pulses with a pulse repetition frequency of 75 Hz. The amplitude should be approximately 4 V. Switch off the bit clock pulses by means of SELECT-X-8.

Pin assignment of Tuchel connector 34:

Pin	Signals
1	Output of regenerated signal
2	Output of bit clock
3	+ input for channel 2
4	+ input for channel 1
5	- input for channel 2
6	- input for channel 1
7	Ground
8	Not used

b) The regenerated signal with 75 baud and approximately 4 V amplitude can be observed at pin 1 of the Tuchel socket. Switch on by means of SELECT-X9. Switch off by means of SELECT-X8. After switching off there remains a positive potential.

3.2.8 V.24 Interface

a) Connect a printer with V.24 interface to the 25-way Cannon socket 31. Adjust printer for 8-bit ASCII code without parity, autofeed and 2400 baud. Set address switch 29 to V.24. Set GA 082 to 2400 baud and autofeed as described in section 2.2.6. Switch on B-TEST-PRINT. Individual lines of 28 alternating 1 and 0 characters should be printed out.

   Open switch 4 of S1 on the microprocessor board (no autofeed) and repeat the test after switching the GA 082 off and on again. A blank line should now follow each line.

b) Check the input via the V.24 interface with the aid of the ASCII keyboard. The keyboard must have a serial V.24 interface with 8 data bits without parity and 2400 baud. Input of the ASCII character string

   C1T1D1

   should switch on the functions C - TEST - DEMOD.

3.2.9 IEC Bus

Connect an IEC-bus controller to the 24-way Amphenol connector 30. Set the address switches 29 to various values so that each switch is used once in each position. Use the program examples given in section 2.8.4.

3.2.10 Factory-selected Values

Checking of the rated specifications should be completed by checking the following settings of the selector switches:

Address switches 29 on rear panel:

Designation	1	0	Function
A1		x	} Address 0
A2		x	
A3		x	
A4		x	
A5		x	
TON		x	No talk only
•		x	
IEC/V.24		x	Output to V.24 interface

Switches S1 on microprocessor board:

Switch No.	1	0	Function
1		x	CPU on
2		x	ALE on
3		x	NMI off
4		x	Autofeed on
5		x	} 2400 baud
6		x	
7	x		
8	x		

Switches S1 on interface board:

Switch No.	1	0	Function
1		x	} Internal frequency standard
2		x	
3		x	Not used
4		x	Not used

Switches S2 and S3 on interface board for mixer frequency 1402.20 kHz:

S2 1 2 3 4	S3 1 2 3 4 5 6 7 8
1 1 1 0	1 1 0 0 1 1 1 1

4. Circuit Description

4.1 Modules of GA 082

Fig. 4-1 shows the individual modules of the GA 082 and their connections. The microprocessor board contains all elements pertaining to a fully operative microprocessor system. In addition to the CPU there are the data memories, the program memories, the interrupt chip, the timer chip, the serial interface and the 300-Hz clock. The microprocessor board can be operated as a stand-alone unit in conjunction with the interface board or with the control board. The control board is mounted behind the front panel and carries the operating controls and the display elements. The interface board carries all interface circuits required for performing the measurement.

4.2 Microprocessor Board

See circuit diagram 624.0758 S

Fig. 4-2 shows a block diagram of the microprocessor board. The 8086 CPU D10 receives the 5-MHz clock from the clock generator D3 which oscillates at 15 MHz and also feeds the frequency dividers D4, D5 and D6. The other clock frequencies required in the GA 082 and the 300-Hz clock are derived therefrom. The oscillator frequency of 14.7456 MHz is an integral multiple of 9600 Hz and enables easy derivation of the baud rates required for the serial interface.

The data traffic between the CPU and the memory chips is handled via a 16-bit data bus. For the peripheral chips a 8-bit data bus is sufficient which is connected to the lower 8 bits of the 16-bit bus via the transceiver D28. This connection is however only enabled for the time of the data transfer to the peripherals. Another transceiver D26 connects the data lines supplying the control board to the 8-bit data bus.

The interrupt chip U3 processes eight interrupt requests, three of them coming directly from the microprocessor board. IR3 is connected to the 300-Hz clock D6. IR4 responds to the overflow of the counter 0 in timer 1 (D1). IR7 signals that the serial interface has received a character.

The USART chip U2 feeds the serial interface, which is connected to the V.24 socket 31 via the V.24 drivers U1 and V.24 receiver U4 and through the interface board. The baud rate for this interface is selected at the switches S1 and via the input D25 entered into the CPU (D10). The counter 1 in timer 1 (D1) is adjusted so that the frequency of 1.2288 MHz is divided into 64 clocks per step.

With the two timers D1 and D2 six counters of 16 bits each are available which are required for measuring the momentary frequency and for determining the signal intervals. Two counters alternately count the number of AF or IF periods of a measured interval and its duration in µs. The counter 0 in timer 1 continuously counts 16-µs clocks as time basis for determining the duration of the signal intervals.

Via the output register D9 control signals are taken to the interface unit for switching on the TEST function, the channel switchover and the output of the regenerated signal.

With the aid of the connectors X17 and X18 a direct connection to the INTEL board SDK-86 can be established for test purposes. The switches S1.1 and S1.2 must be open for this purpose so that the internal CPU and the address latches are switched off (see 5.3).

4.3 Interface Board

See circuit diagram 624.0770 S

Fig. 4-3 shows the block diagram on the interface board. G1 is the built-in crystal oscillator of high accuracy. S1 and D17 are provided for selecting the internal or external frequency reference. The fed-in frequency is divided in D19 to 1 MHz. This 1-µs clock is used as time basis for measurement of the momentary frequency, for the bit clock produced in D25 and - after division to 16 µs in D11 - as clock for determining the duration of the signal intervals.

For demodulated signals there are three different inputs. The relays K1 and K2 enable switchover between two current inputs at the connector X30. Via the optocouplers U28 and U29 the selected input is isolated from the voltage input which is taken via X40. Both inputs are combined in D13 to D15. The input signal or the 75-baud test signal can be switched to the interrupt lines IR0 and IR1. IR0 produces an interrupt at a negative and IR1 at a positive signal edge.

The AF/IF signal at the input X50 is first converted by N1 into a binary squarewave signal. In the mixer D9 the signal is mixed with a mixer frequency which is selected by the switches S2 and S3 and produced in the LO synthesizer made up of D2 to D8. The AF signal thus obtained is filtered in the lowpass filter and then digitized again in N2. The subsequent switch D10 enables switch-over to a modulated test signal which switches between 1200 and 2400 Hz. In the trigger circuit D12 the 1200 measurement intervals/s for determining the momentary frequency are selected so that they contain an integral number of signal periods. At the end of each measurement interval the interrupt IR2 is actuated. The flipflop D13 switches the counters used for counting the signal periods and the length of the measurement interval alternately on and off.

The lines of the V.24 interface are only through-connected on the interface board. The IEC bus is fed by U1 and the transceiver D21 to D24. The interrupt line IR5 combines various conditions which are defined during the interrupt processing in the interrupt register of the IEC module.

The three counters of the timer D25 are required for the generation of the bit clock. The first counter is adjusted to the measured baud rate and produces 16 clocks/bit. The second counter divides the clock down to one clock/bit, which is adjusted to the centre between the signal edges. The third counter finally produces the pulse length of 100 µs for the bit clock.

4.4 Control Panel

See circuit diagram 624.0712 S

Fig. 4-4 shows the block diagram of the control panel. The keyboard/display interface U4 drives the mutiplexed 7-segment displays and reads the position of the operating controls.

The 4:16 decoder D21, D22 successively connects the anodes of the 16-digit display with the pnp Darlington transistors V1 to V16 to the positive voltage. For each number the active segments are connected to ground by U4 via the drivers D24, D25. The dot following the number is driven as 8th segment.

The switches S1 to S22 are also read in in multiplex operation. The 3:8 decoder D23 successively connects the four rows of switches arranged in a 4-by-6 matrix to zero. For each row, 6 column values are read in which are at zero for closed switches.

The 16-digit 16-segment display H27, H28 is driven via the driver U14, U15. The LED lines for DEMOD, SYNC and CODE display require an own latch for each LED which is directly loaded by the data bus.

4.5 Power Supply

See circuit diagram 624.0512 S B1.2

The individual components belonging to the power supply are mounted on the power supply boards I and II and directly on the chassis. The 5-V stabilizer N1 and the overvoltage protection N2 are mounted on a heat sink on the rear panel. N3 and N4 stabilize the voltages of +12 V and -12 V.

A further program loop can be produced by removing one of the two CMOS RAMs D23 or D24 after closing the switch S1.2. After switching on the GA 082 a permanent repetition of the RAM test should cause the error indication

-H-L-RAM ERROR

If this loop operates successfully, the microprocessor itself can be used for further tests after reinserting the removed CMOS RAM.

5.2 Troubleshooting using Signature Analysis

All address and data lines on the microprocessor, the interface and the control board can be checked with the aid of the signature analysis described in section 2.9.2. For complete checking of the GA 082, use the procedures described in section 3.2.

5.3 Connection to SDK-86

With the aid of the connectors X17 and X18 on the microprocessor board it is possible to connect the GA 082 directly to the INTEL SDK-86 board. The connection to the corresponding connectors of the SDK-86 can be established by means of two 50-way flat cables. The CPU must be switched off by opening the switches S1.1 and S1.2 on the microprocessor board. The GA 082 can be operated with the CPU of the SDK-86 when using the hexadecimal start address F7FD:0000. The RAMs of the SDK-86 are also used since they are accessible under the same address 0 to 1000_H link the RAMs of the GA 082. Since the RAMs of the GA 082 are also accessible under the address 1000 to 2000_H, this area can be used for test programs. The I/O addresses of the microprocessor peripherals are listed in Table 22.

Table 22 I/O Addresses of peripherals

Hex address	Chip	Identification	Unit	Designation
00	8259	U3	A3	Interrupt
02	"			"
08	8253	D1	A3	Timer 1, Counter 0
0A	"			Counter 1
0C	"			Counter 2
0E	"			Mode
10	8253	D2	A3	Timer 2, Counter 0
12	"			Counter 1
14	"			Counter 2
16	"			Mode
18	365/174	D25/D9	A3	Parallel I/O
38	8251	U2	A3	USART, Data
3A	"			Control
40-4E	8291	U1	A2	IEC-bus
50	LS244	D20	A2	Address switch
60	8253	D25	A2	Timer 3, Counter 0
62	"			Counter 1
64	"			Counter 2
66	"			Mode
80	LS373	D20	A1	CODE Byte 0
82	LS373	D19	A1	Byte 1
84	LS373	D18	A1	Byte 2
86	LS373	D17	A1	Byte 3
88	LS373	D16	A1	Byte 4
8A	LS373	D15	A1	Byte 5
8C	LS373	D6	A1	SYNC Byte 0
8E	LS373	D5	A1	Byte 1
90	LS373	D4	A1	DEMOD Byte 0
92	LS373	D3	A1	Byte 1
94	LS373	D2	A1	Byte 2
96	LS373	D1	A1	Byte 3
98	LS373	D7	A1	LEDs for Keyboard
9A	LS373	D8	A1	LEDs for Keyboard
A0-AE	7243	U15	A1	Disp.1,Characters 1 to 8
B0-BE	7243	U14	A1	Disp.2,Characters 9-to 16
C0	8279	U4	A1	Keyb/Disp. Data
C2	"			Control