Errata

Title & Document Type: 3437A System Voltmeter Operating and Service Manual

Manual Part Number: 03437-90003

Revision Date: January 1979

HP References in this Manual

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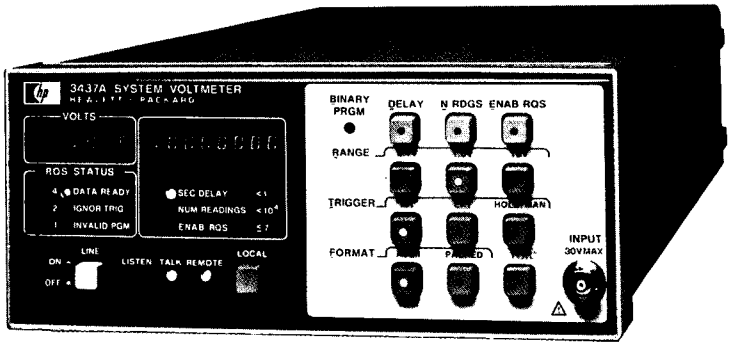
OPERATING AND SERVICE MANUAL

SYSTEM VOLTMETER
3437A



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SUPERSEDES
NONE

-hp- MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: 1630A04431 and Above

EXCESS DELAY

Certain performance verification procedures contained within the 3437A Operating and Service Manual check the delay capabilities of instrument. Some instruments may not be able to duplicate the instrument delay specifications, this is generally observed by having an extra 100 nanoseconds introduced into the Delay Accuracy/Jitter performance verification procedure. This extra delay can be removed by replacing A2R251 and A2R252 of the 03437-66502 assembly with jumpers. These resistors are located close to the pc board edge and have the characteristics of being 220 ohm, 1 watt. These resistors are to be removed only if the 3437A exhibits an extra 100 nanoseconds of delay in the Delay Accuracy/Jitter performance verification procedure.

The purpose of resistors A2R251 and A2R252 is to protect the 3437A internal circuitry from excessive voltages which would damage the instrument. Removing the resistors reduces the instrument capability of surviving from excessive voltages applied to the DELAY OUTPUT and EXTERNAL TRIGGER terminals, therefore caution must be exercised in use with the instrument if the resistors are removed.

Some instruments with a serial number less than 1630A04431 may contain the 03437-66502 assembly due to its use in the Blue Stripe Exchange program as the 03437-69502 assembly.

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OPERATING AND SERVICE MANUAL

MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: 1630A00101 and greater

IMPORTANT NOTICE

This loose-leaf manual does not normally require change sheets. All change information is integrated into the manual by means of revised pages. Each revised page is identified by a revision letter located at the bottom of the page. A reference symbol, located directly below the revision letter, indicates which of the backdating changes in Section VIII apply to that page. If the serial number of your instrument is lower than the serial number indicated on this page, this manual may contain revisions that do not apply to your instrument. Refer to Section VIII for complete backdating information.

WARNING

To prevent potential fire or shock hazard, do not expose equipment to rain or moisture.

Manual Part No. 03437-90003
Revision A
Microfiche Part No. 03437-90051

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Printed: January 1979

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Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the National Institute of Standards and Technologies, to the extent allowed by the the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

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This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment [,except that in the case of certain components listed in Section I of this manual, the warranty shall be for the specified period]. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used On Equipment or In Manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).

OR

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.

OR

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which,if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE:

The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

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Herstellerbescheinigung

Hiermit wird bescheinigt, daβ das Gerät/System HP 3437A in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation fur Meβ- und Testgeräte

Werden Meβ- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Meβaufbauten verwendet, so ist vom Betreiber sicherzustellen, daβ die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that the equipment HP 3437A is in accordance with the Radio Interference Requirements of Directive FTZ 1046/84. The German Bundespost was notified that this equipment was put into circulation, the right to check the series for compliance with the requirements was granted.

Additional Information for Test- and Measurement Equipment

If Test- and Measurement Equipment is operated with unscreened cables and/or used for measurements on open set-ups, the user has to assure that under operating conditions the Radio Interference Limits are still met at the border of his premises.

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This section contains general information concerning the -hp- Model 3437A System DVM. Included is an instrument description, specifications, information concerning instrument and accessory information, and safety considerations.

1-3. DESCRIPTION.

1-4. The Model 3437A is a Microprocessor controlled 3½ digit, successive approximation system voltmeter, capable of sampling voltages at rates up to 5700 samples per second.

1-5. Chassis isolated input terminals, a wideband input amplifier, auto-zero, auto-polarity, sample and hold, and 100% overrange on each of the input voltage ranges (.1 volt, 1 volt, and 10 volts) provide floating measurement capability (± 20 V) over the frequency range of DC through 1.0 MHz.

1-6. Hewlett-Packard Interface Bus is standard. All front panel functions are programmable. The output data format is selectable between an ASCII (8 byte) and Packed (2 byte) format. The packed data format allows the controller additional data storage as well as allowing the input voltage to be sampled at rates up to 5700 samples per second.

1-7. The 3437A digital delay logic is capable of delaying an external trigger from 0 to 1 second (100 ns steps), and of generating up to 9999 triggers (for each trigger received) at rates of 1 Hz through 5700 Hz. The internally generated triggers provide a burst sampling capability (up to 9999 samples) at a maximum rate of 5700 sampled per second. Figures 1-1 and 1-2 illustrate the delayed measurement and burst sampling capabilites of the 3437A.

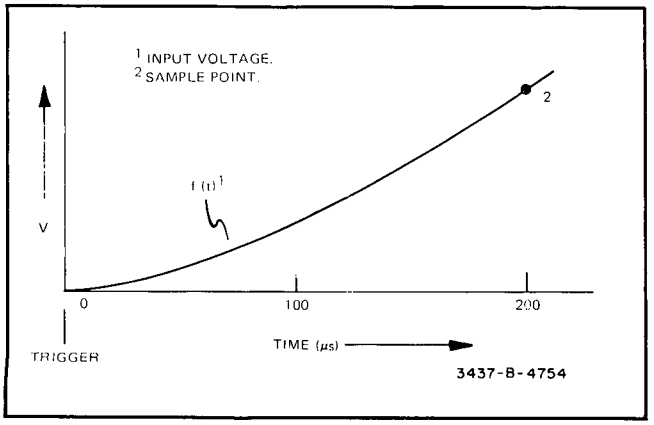


Figure 1-1. NRDGS = 1 DELAY = 200 μs.

1-8. (Figure 1-1) 200 μs after being triggered, the 3437A will sample and (after conversion) display the instantaneous value of the input voltage. If the 3437A is addressed to talk, the sampled input voltage will be output onto the HP-IB.

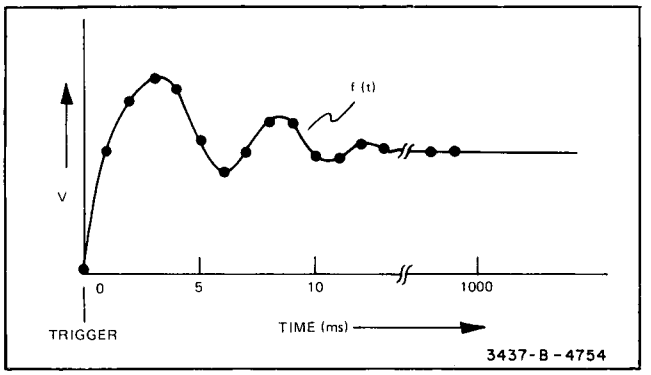


Figure 1-2. NRDGS = 1000 DELAY = 1 ms.

1-9. (Figure 1-2) When triggered, the 3437A will sample the input voltage 1000 times at 1 ms intervals. Between samples, the instantaneous value of the sampled input voltage is converted and output onto the HP-IB.

1-10. The Binary Program mode provides a means of programming the 3437A using an abreviated program code. When interrogated in the Binary Program mode. The 3437A responds by writing 7 bytes (completely describing the programmed state of the instrument) onto the HP-IB. The controller can use these 7 bytes as an abreviated program code to reprogram the 3437A to its previous configuration.

1-11. Model 3437A applications include:

a. Fast multipoint data-acquisition.

b. Repetitive-waveform analysis.

c. Low frequency transient characterization.

d. Low frequency True RMS measurements.

1-12. SPECIFICATIONS.

1-13. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Any change in the specifications due to manufacturing, design, or traceability to the U.S. National Bureau of Standards will be covered by revised pages, a change sheet, or both, to this manual. Addi-

Table 1-1. Specifications.

VOLTAGE MEASUREMENT CHARACTERISTICS.

Range	Bandwidth (3dB)		Display*
10 Volt	1.0 MHz	± 19.98 (max)	± 99.99 (ovrld)
1 Volt	1.1 MHz	± 1.998	± 9.999
.1 Volt	40 kHz	± .1998	± .9999

Static Accuracy (90 days, 23°C ± 5°C)

10 Volt Range	± 0.05% of Reading	± 1.6 Digits
1 Volt Range	± 0.03% of Reading	± 1.6 Digits
.1 Volt Range	± 0.06% of Reading	± 1.8 Digits

Static Accuracy (1 year, 23°C ± 5°C)

10 Volt Range	± 0.05% of Reading	± 2.0 Digits
1 Volt Range	± 0.03% of Reading	± 2.0 Digits
.1 Volt Range	± 0.06% of Reading	± 2.2 Digits

Static Accuracy Temperature Coefficient (0°C to 50°C)
± 0.002% reading/°C ± 0.05 digits/°C

Dynamic Accuracy

Range	Step Input	mV within Final Value	Time
10 Volt	10 V	± 200 mV	700 ns
10 Volt	10 V	± 30 mV	7.5 μs
1 Volt	1 V	± 20 mV	700 ns
1 Volt	1 V	± 3 mV	1.5 μs
.1 Volt	.1 V	± 200 μV	25 μs

DELAY CHARACTERISTICS.

Delay
For NRDGS equal to 0 or 1
0 to .9999999 sec in 100 ns steps

For NRDGS > 1

Data Format	Delay between readings
ASCII	277.8 μs to .9999999 sec
Packed	175.4 μs to .9999999 sec

Offset (actual delay with 0 delay programmed)
100 ns ± 25 ns

Accuracy
± 0.008% Delay + Delay offset

Repeatability (Jitter)
For NRDGS equal to 0 or 1

Delay	Jitter
0 or 100 ns	2 ns
200 ns to 50 ms	10 ns + .002% of Delay
> 50 ms	110 ns

NUMBER OF READINGS. **(For each trigger received.)**

From 0 to 9999

INPUT CHARACTERISTICS.

Input Impedance

Range	Impedance	
10 Volt	1 MΩ (± 20%)	< 75 pF
1 Volt	> 10^8 Ω	< 75 pF
.1 Volt	> 10^8 Ω	< 75 pF

Maximum Input Voltage (All ranges)

HI to LO	< ± 30 V Peak
LO to CHASSIS	< ± 42 V Peak

PROGRAMMABILITY.

(In accordance with IEEE - 488-1975)

AH1	Acceptor	PPØ	Parallel Poll
CØ	Controller	RL1	Remote/Local
DC1	Device Clear	SR1	Service Request
DT1	Device Trigger	SH1	Source
L4	Listener	T5	Talker

COMMON MODE REJECTION RATIO.

⩾ 75 dB (1 kΩ unbalance in low input lead at 60 Hz)

*Display will indicate overload if input is unterminated (.1 volt range).

Table 1-2. Supplemental Characteristics.

MAXIMUM READING RATE.[1]

ASCII	3600 Readings per second
Packed	5700 Readings per second

[1]Actual reading rate is given by:

ASCII $\frac{3600 \times 7 \text{ Byte Listen Rate}}{3600 + 7 \text{ Byte Listen Rate}}$

Packed $\frac{5700 \times 2 \text{ Byte Listen Rate}}{5700 + 2 \text{ Byte Listen Rate}}$

Where Listen Rate = Data acceptance rate of listener

GENERAL.

Power Requirements

100 V, 120 V, 220 V, 240 V (+ 5% –10%, 48–440 Hz)
⩽ 42 VA

Operating Temperature

0°C to 50°C

Storage Temperature

–40°C to 75°C

Humidity Range

< 95% RH (0°C to 40°C)

Dimensions

212.7 mm wide x 88.9 mm high x 527.1 mm deep

Weight

Net	5.6 kg
Shipping	7.6 kg

Model Number and Name

3437A System Voltmeter

tional information describing the operating characteristics (Table 1-2) are not specifications but are supplemental information for the user.

1-14. OPTIONS.

1-15. The following options are available for the -hp- Model 3437A System Voltmeter:

Option	-hp- Part Number	Description
907	5061-0088	Front Handle Kit
908	5061-0072	Cabinet Assembly
909	5061-0075	Cabinet Assembly

1-16. ACCESSORIES.

1-17. The following accessories are available and can be ordered from your nearest -hp- Sales and Service Office:

1. DSA Test ROM -hp- 34115A
2. Performance Test Source Interface -hp- 34114A
3. Performance Test Trigger Interface -hp- 34113A

1-18. SAFETY CONSIDERATIONS.

1-19. If, to preserve the apparatus from damage, it is necessary for the user to refer to the instruction manual, the apparatus will be marked with the symbol ⚠.

1-20. INSTRUMENT IDENTIFICATION.

1-21. A three-section serial number (XXXXAXXXXX) is used to identify the Model 3437A. Figure 1-3 illustrates the meaning of the three parts of the number.

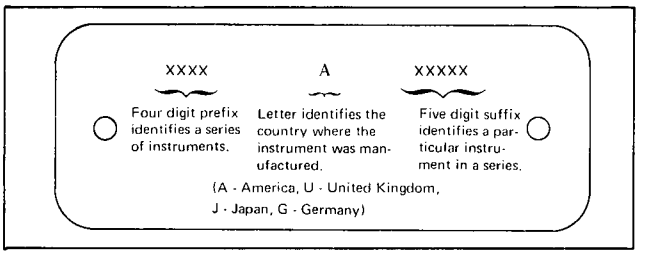


Figure 1-3. Instrument Serial Number.

Table 1-3. Message Transfer Rates (Listen).

Listen	Handshake (μs/Byte)[A]
Commands (ATN True)	
Addressed to Listen (ATL)	58
Addressed to Talk (ATT)	38
Group Execute Trigger (GET)	160
Local Lockout (LLO)	37
Selected Device Clear (SDC)	124
Serial Poll Enable (SPE)	35
Serial Poll Disable (SPD)	36
Unlisten (UNL)	36
Untalk (UNT)	36
Program Code (ATN False)	
Delay	100
" . "	92
0	64
1	69
2	74
3	79
4	84
5	89
6	94
Store	176
NRDGS	112
1	94
2	68
3	68
4	68
Store	112
Enab RQS	108
7	59
Store	90

Listen	Handshake (μs/Byte)[A]
Program Code (ATN False) Cont'd	
Range 1	56 88
Range 2	56 89
Range 3	56 90
Trigger 1	56 97
Trigger 2	56 98
Trigger 3 [B]	56 90
Trigger 3 [C]	56 74
Format 1	56 98
Format 2	56 99
Binary Prgm	83
1st Byte	95
2nd Byte	78
3rd Byte	66
4th Byte	75
5th Byte	42
6th Byte	42
7th Byte	140

[A] Typical

[B] Initial

[C] Subsequent—maximum rate (due to conversion time)≅240 μs.

Table 1-4. Message Transfer Rates (Talk).

Talk	Handshake (μs/Byte)[A]
Data Formats (ATN False)	
ASCII	22 μs
Packed	20 μs

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information and instructions pertaining to initial instrument set-up. Included are initial inspection procedures, power and grounding requirements, environmental information, bench and rack mounting instructions, a description of interface connectors, and repackaging instructions.

2-3. INITIAL INSPECTION.

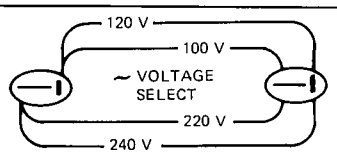
2-4. This instrument was carefully inspected both mechanically and electrically before shipment. It should be free of mars or scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage that might have occurred in transit, and the electrical performance should be tested using the performance tests outlined in Section V. If there is damage or deficiency, refer to the warranty inside the front cover of this manual.

2-5. POWER REQUIREMENTS.

2-6. This instrument can be operated from ac line voltages of 100 V, 120 V, 220 V, 240 V, at corresponding line frequencies of 48 through 440 Hz.

CAUTION

Verify that the 110 V/220 V Line Voltage Selection switch, (Figure 2-1) located on the rear panel of Model 3437A, is set to the ac source voltage to be used before inserting the power cord and turning the instrument on. Also insure that the proper fuse is installed.



LINE VOLTAGE (VOLTS)	OPERATING RANGE (VOLTS)	FUSE (mA)
100	90–105	500
120	108–126	500
220	198–231	250
240	216–252	250

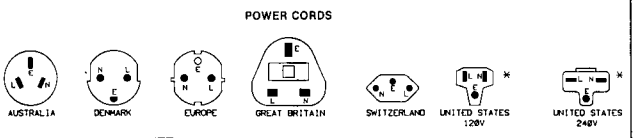
3437-B-4755

[1]SELECTED FOR 120V.

Figure 2-1. Line Voltage Selection.

2-7. Power Cords and Receptacles.

2-8. Figure 2-2 illustrates the various -hp- power cord configurations. If the appropriate power cord is not included with the instrument, notify the nearest -hp- Sales and Service Office and a replacement cord will be provided.



Country	Part Number	Opt.	Voltage
Australia	8120-1369	901	250V 6A
Denmark	8120-2956	912	250V 6A
Europe	8120-1689	902	250V 6A
Great Britain	8120-1351	900	250V 6A
Switzerland	8120-2104	906	250V 6A
*United States	8120-1378	903	120V 10A
*United States	8120-0698	904	240V 10A

Power cords supplied by HP have polarities matched to the power input socket on the instrument:
- L = Line or Active Conductor (also called "live" or "hot").
- N = Neutral or Identified Conductor
- E = Earth or Safety Ground

NOTE: Plugs are viewed from connector end. Shape of molded plug may vary within country.

* CSA certification includes only these Power Plugs

Figure 2-2. -hp- Power Cords.

2-9. Grounding Requirements.

2-10. To protect operating personnel, the National Electrical Manufacturers' Association (NEMA) recommends that the instrument panel and cabinet be grounded. The Model 3437A is equipped with a three-conductor power cable which, when plugged into an appropriate receptacle, grounds the instrument. The offset pin on the power cable is the ground wire.

2-11. To preserve the protection feature when operating from a two-contact outlet, use a three-prong to two-prong adapter and connect the green pigtail on the adapter to power line ground.

2-12. ENVIRONMENTAL REQUIREMENTS.

2-13. The 3437A should not be operated where the ambient temperature exceeds 0°C to 50°C or stored where the ambient temperature exceeds - 40°C to + 75°C.

2-14. Humidity.

2-15. The instrument may be operated in environments with relative humidity of up to 95%. However, the instrument must be protected from temperature extremes which cause condensation within the instrument.

2-16. Altitude.

2-17. The instrument may be operated at altitudes up to 4573 meters (15,000 feet).

WARNING

To prevent potential electrical or fire hazard, do not expose equipment to rain or moisture.

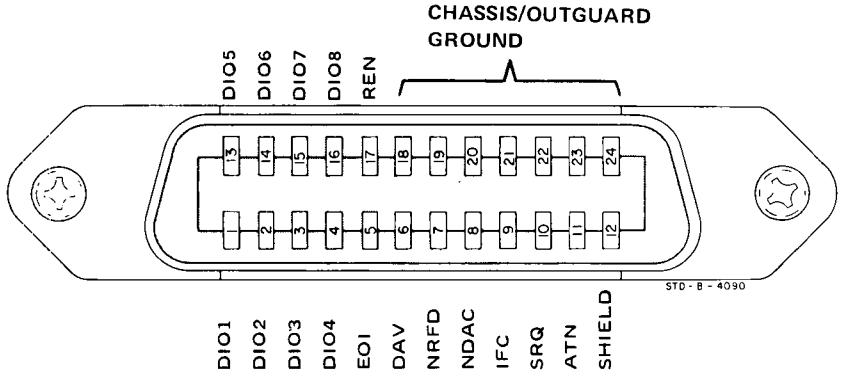
2-18. INSTRUMENT MOUNTING.

2-19. The Model 3437A is shipped with plastic feet and tilt stand in place, ready for use as a bench instrument. The front of the instrument may be elevated for convenience of operating and viewing by extending the tilt stand. The plastic feet are shaped to permit placing the instrument on top of other half-module Hewlett-Packard instruments.

2-20. Rack Mounting.

2-21. The Model 3437A is housed in a -hp- standard (½

HP-IB CONNECTOR J12



Mating Connector:

-hp- Part No. 1251-0293
Amphenol No. 57—30240

Mating Cables:

10631A	3 ft.
10631B	6 ft.
10631C	12 ft.

DIO 1-8 (Data Input/Output)
Mnemonic referring to the eight "Data Input/Output" lines. The DIO lines transfer messages in a byte-serial, bit parallel manner.

EOI (End or Identify)
Mnemonic referring to the "End or Identify" control line. EOI is used by a device to indicate the end of a multiple-byte transfer.

DAV (Data Valid)
Mnemonic referring to the "Data Valid" control line. DAV is used to coordinate the "handshake" sequence. The DAV line is controlled by the source (talker). When DAV is true, data on the DIO lines is considered valid.

NRFD (Not Ready For Data)
Mnemonic referring to the "Ready For Data" control line. NRFD is used to coordinate the "handshake" sequence. The NRFD line is controlled by the acceptor (listener). When NRFD is true, the acceptor indicates to the source that he is ready to accept data.

NDAC (Data Not Accepted)
Mnemonic referring to the "Data Accepted" control line. NDAC is used to coordinate the "handshake" sequence. The NDAC line is controlled by the acceptor (listener). When NDAC is true, the acceptor indicates to the source that the data on the DIO lines has been accepted.

IFC (Interface Clear)
Mnemonic referring to the "Interface Clear" control line. IFC is used to place the HP-IB system in a known quiescent state. The IFC line is controlled by the system controller.

SRQ (Service Request)
Mnemonic referring to the "Service Request" control line. SRQ is used (by any device having service request capability) to indicate to the system controller that the device requires service. The controller responds by polling the devices to determine which device requested service.

ATN (Attention)
Mnemonic referring to the "Attention" control line. The state of the ATN line determines whether the HP-IB is in the "Command mode" (ATN true) or the "Data mode" (ATN false). When ATN is true, all devices must listen to the data lines, and when ATN is false, only devices that have been addressed will actively transfer data.

REN (Remote Enable)
Mnemonic referring to the "Remote Enable" control line. REN is used in conjunction with listen addresses (DIO 1-8) to select either local or remote control of each device.

For further information concerning the HP-IB, refer to "Hewlett-Packard Interface, A Compendium of Technical Articles" -hp- publications No. 5952-2472.

Figure 2-3. Hewlett-Packard Interface Bus Connector.

module) System II enclosure. Refer to the -hp- catalog for rack mounting accessories.

2-22. Interface Connectors.

2-23. Input. The voltage to be measured is applied to either the front or rear panel mounted (parallel connected) triax connector labeled INPUT.

2-24. Ext Trig and Delay Out. A standard (negative edge) TTL input applied to the rear panel mounted BNC connector labeled EXT TRIG causes the instrument to initiate one or more measurements and provide one or more corresponding delayed triggers at the rear panel mounted BNC connector labeled DELAY OUT.

2-25. Hewlett-Packard Interface Bus (HP-IB). Figure 2-3 illustrates the rear panel HP-IB connector, along with a brief description of each signal line.

2-26. Interface Cable Length. The maximum accumulative length of an HP-IB cable in any system must not exceed more than 2 meters of cable per device (up to 15 devices) or 20 meters, which ever is less.

2-27. REPACKAGING FOR SHIPMENT.

2-28. The following is a general guide for repackaging the instrument for shipment. If the original container is available, place the instrument in the container with appropriate packing material and seal with strong tape or metal bands. If the original container is not available, proceed as follows:

a. Wrap the instrument in heavy paper or plastic before placing in an inner container.

b. Place packing material around all sides of the instrument and protect panel face with cardboard strips or plastic foam.

c. Place the instrument and inner container in a heavy carton and seal with strong tape or metal bands.

d. Mark shipping container "DELICATE INSTRUMENT." "FRAGILE." etc.

NOTE

If the instrument is to be shipped to Hewlett-Packard for service or repair, attach a tag to the instrument identifying the owner and indicating the service or repair to be accomplished. Include the model number and full serial number of the instrument. In any correspondence, identify the instrument by model number and full serial number. If you have any questions, contact your nearest -hp- Sales and Service Office.

SECTION III
OPERATING INSTRUCTIONS

3-1. INTRODUCTION.

3-2. This section contains complete operating instructions (both bench and system) for the Model 3437A Systems Voltmeter. Included is a description of the front and rear panel controls and indicators, programming instructions, and application examples.

3-3. Controls and Indicators.

3-4. Figure 3-1 identifies the 3437A displays, annunciators, controls, and connectors. The identification of each item is keyed to the drawing within the figure.

3-5. Front Panel Description.

3-6. KEYBOARD. The 3437A keyboard functions in two modes:

a. Key per function.

b. Numeric entry.

3-7. Key Per Function. The Key Per Function mode (each key representing instrument functions) occurs when the instrument is turned on.

3-8. Numeric Entry. The Numeric Entry mode (annunciated by blinking DELAY, NRDGS, or ENAB RQS annunciators) is a subset of the Key Per Function mode, and occurs when either the DELAY (7) N RDGS (8) ENAB RQS (9) keys are pressed while the keyboard is in the Key Per Function mode. Subsequent entries (displayed by the numeric entry display) correspond to the blue labeled numeric symbols 0-9 and decimal point . The Numeric Entry mode is terminated when STORE is pressed.

3-9. VOLTS DISPLAY. Displays the sign and magnitude of the sampled input voltage ("+" is implied). The overload indication is ± 99.99 (Decimal point position corresponds to voltage range selected).

3-10. NUMERIC ENTRY DISPLAY. The contents of the numeric entry display are annunciated directly below the display.

3-11. RQS STATUS. The RQS STATUS annunciators annunciate the instrument status.

3-12. Data Ready. The DATA READY annunciator notifies the operator that the sampled input voltage has been converted, displayed, and is ready to be output onto the HP-IB. The DATA READY annunciator remains on until the measurement data has been output onto the HP-IB, or until a new function is programmed.

3-13. Ignore Trig. The IGNORE TRIG annunciator notifies the operator that a second trigger occured prior to completion of the measurement sequence/data transfer initiated by the first trigger, and that the second trigger was ignored. The IGNORE TRIG annunciator remains on until a new function is programmed.

3-14. Invalid Prgm. The INVALID PRGM annunciator notifies the operator that an invalid program condition has occurred. The annunciator becomes illuminated during the Remote and Local modes of operation, for the following reasons:

LOCAL:

a. DELAY (0–.9999999). The first entry into the delay field must be a decimal point. Any entry other than a decimal point (leading zeros ignored) results in an invalid program condition. When this occurs, the last valid delay entry is stored and the numeric entry mode is terminated. The INVALID PGM annunciator remains on until the key causing the invalid entry is released.

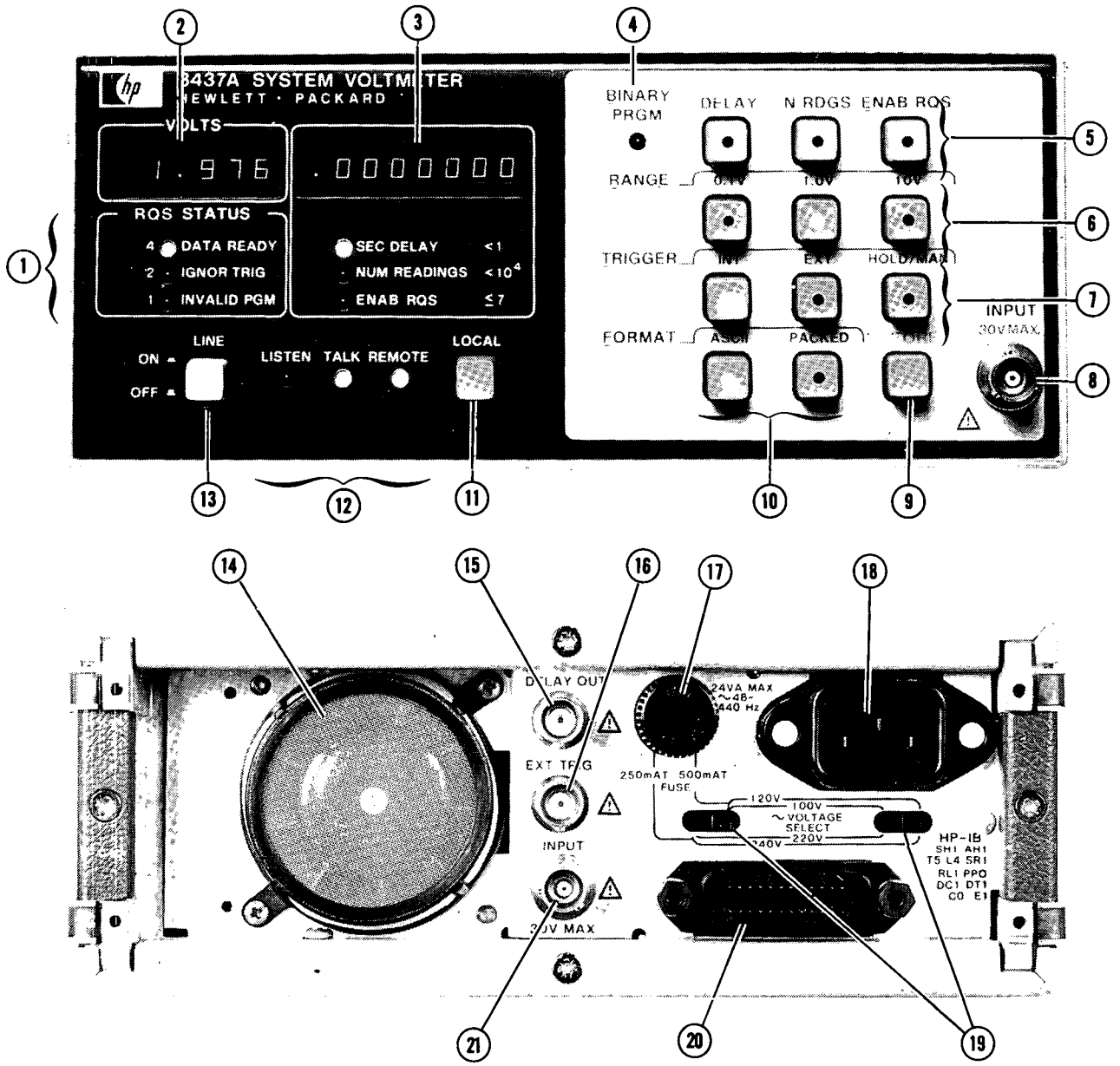
b. NRDGS (0–9999). A decimal point entry into the number of readings field results in an invalid program condition. When this occurs, the last valid NRDGS entry is stored and the numeric entry mode is terminated. The INVALID PGM annunciator remains on until the key causing the invalid entry is released.

c. ENAB RQS (0–7). Any entry other than 0–7 results in an invalid program condition. When this occurs, the last valid ENAB RQS entry is stored and the numeric entry mode is terminated. The INVALID PGM annunciator remains on until the key causing the invalid entry is released.

d. STORE. If the STORE key is pressed while the keyboard is not in the Numeric Entry mode, an invalid program condition occurs. The INVALID PGM annunciator remains on until the key causing the invalid entry is released.

REMOTE:

An invalid entry while in the Numeric Entry mode, or the use of an invalid program code, will result in an invalid



1 Annunciated instrument status (service request [SRQ] will be set if RQS STATUS and ENAB RQS [numeric entry display] correspond).

2 Volts display - Displays the sign and magnitude of the sampled input voltage.

3 Numeric entry display - Displays DELAY, NRDGS, and ENAB RQS entries.

4 Binary program mode annunciator.

5 Pre-entry keys for DELAY, NRDGS (Number of readings), and ENAB RQS (request service mask).

6 Voltage range select keys

7 Trigger mode select keys

8 Input connector

9 Numeric entry termination key (stores contents of the numeric entry display).

10 Output data format select keys

11 Keyboard return-to-local

12 Annunciated HP-IB status

13 Line switch

14 Fan

15 Delayed trigger output connector

16 External trigger input connector

17 Fuse

18 Line cord receptacle

19 Line voltage select switch

20 HP-IB connector

21 Input connector

Figure 3-1. 3437A Front and Rear Panel Description.

program condition to occur. The INVALID PGM annunciator remains on until the 3437A is readdressed to listen.

3-15. DELAY 7 [•]. The DELAY key (delay pre-entry) is used when entering either the delay between readings (NRDGS > 1) or the delay that occurs prior to sampling the input voltage after the 3437A is triggered (NRDGS=1).

EXAMPLE:

1. Press DELAY 7 [•]
   a. The Numeric Entry mode is annunciated by the (Flashing) DELAY annunciator.
   b. The numeric entry display (annunciated by SEC DELAY) displays the previously stored delay.
2. Press [•] (Any entry other than a decimal point (leading zeros ignored) results in an invalid program condition.
3. Enter up to 7 integers corresponding to the specified delay (additional inputs are ignored). A partial delay field can be set to zeros by pressing STORE [ ].
4. Terminate DELAY entry (Numeric Entry mode) by pressing STORE [ ].

3-16. N RDGS 8 [•] The NRDGS key (number of readings pre-entry) is used when entering the number of readings to be taken after the 3437A is triggered.

EXAMPLE:

1. Press N RDGS 8 [•]
   a. The Numeric Entry mode is annunciated by the (Flashing) NRDGS annunciator.
   b. The numeric entry display (annunciated by NUM READINGS) displays the previously stored number of readings.
2. Enter a 4 digit integer (0–9999) corresponding to the number of readings to be taken after the 3437A is triggered. (If a decimal point is entered into the number of readings field, an invalid program condition results.) Additional entries into a completed NRDGS field, cause previous entries to be shifted left.
3. Terminate NRDGS entry (Numeric Entry mode) by pressing STORE [ ]

3-17. ENAB RQS 9 [•]. The ENAB RQS key (enable request pre-entry) is used when entering the request service mask. (The request service mask is an octal number (0-7) identifying the conditions for which service request (SRQ) is initiated.) Table 3-1 shows the request service mask and corresponding conditions for which the 3437A will initiate a service request.

EXAMPLE:

1. Press ENAB RQS 9 [•]
   a. The Numeric Entry mode is annunciated by the (Flashing) ENAB RQS annunciator.
   b. The numeric entry display (annunciated by ENAB RQS) displays the previously stored request service mask.
2. Enter the request service mask (0-7). An invalid entry results in an invalid program condition to occur. (Additional entries override previous entries.)
3. Terminate ENAB RQS entry (numeric entry mode) by pressing STORE [ ]

Table 3-1. SRQ Conditions.

RQS Mask[1]		Conditions for Initiating SRQ
(4 2 1)	(Octal)	
0 0 0	0	No SRQ Capabilities
0 0 1	1	Invalid Program
0 1 0	2	Trigger Ignore
0 1 1	3	Trigger Ignore or Invalid Program
1 0 0	4	Data Ready
1 0 1	5	Data Ready or Invalid Program
1 1 0	6	Data Ready or Trigger Ignore
1 1 1	7	Data Ready or Trigger Ignore or Invalid Program

[1] a. Invalid PGM
b. Trig Ignore
c. Data Ready

3-18. RANGE 0.1V 4 [•] 1.0V 5 [•] 10V 6 [•] The three voltage ranges (annunciated by the range select keys) are selected by pressing either the 0.1V 4 [•] 1.0V 5 [•] 10V 6 [•] key. (Each range has 100% overrange capability.) The displayed decimal point position will not correspond to the selected voltage range until the 3437A has sampled the input voltage.

INT.

a. Local - With zero delay programmed, the sample rate is approximately 10 samples per second.

b. Remote - To generate an internal trigger while in remote, the following conditions must exist:

1. Remote
2. Internal Trigger
3. Addressed to Talk
4. Not in Binary Prgm Mode
5. Not in Serial Poll Mode
6. Not in Numeric Entry Mode

With these conditions satisfied, the 3437A will generate an internal trigger on the transition of ATN false.

EXT.

The 3437A will sample the input voltage when triggered (TTL negative edge) at the external trigger input connector.

CAUTION

External trigger inputs exceeding TTL levels (0 to 5 V) may cause damage to the 3437A's external trigger input circuitry. The Performance Test trigger interface (-hp- 34113A) is usefull for clamping bipolar triggers to within TTL levels. Refer to page 5-85 for more information on this interface.

HOLD/MAN. (LOCAL & REMOTE)

The first time the HOLD/MAN key is pressed, the 3437A holds the volts display of the last sampled voltage constant. The second time the HOLD/MAN key is pressed (and each time thereafter), a manual trigger is generated. Manual triggers can be generated in this manner until a new function is programmed.

GROUP EXECUTE TRIGGER.

(Addressed HP-IB Command.) Each time the 3437A receives group execute trigger (GET) while addressed to listen, it will generate a trigger (regardless of trigger mode selected).

3-20. FORMAT ASCII PACKED The output data format is selectable between an ASCII (8-byte) and PACKED (2-byte) format.

3-21. ASCII. Each data transfer is output as 6 ASCII characters, followed by a carriage return (CR) and line feed (LF) concurrent with EOI true.

EXAMPLES:

a. **Normal**

i.	.1 volt range	± .1998 (CR)	(LF and EOI)
ii.	1 volt range	± 1.998 (CR)	(LF and EOI)
iii.	10 volt range	± 19.98 (CR)	(LF and EOI)

b. **Overload**

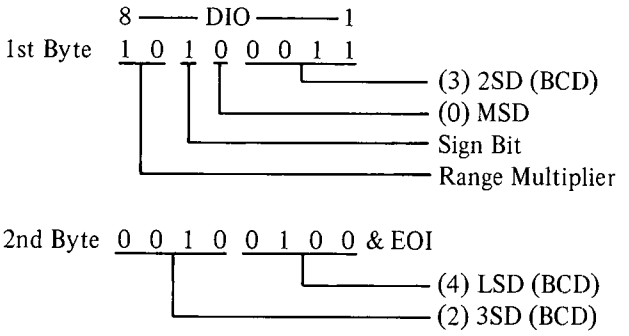
i.	.1 volt range	± .9999 (CR)	(LF and EOI)
ii.	1 volt range	± 9.999 (CR)	(LF and EOI)
iii.	10 volt range	± 99.99 (CR)	(LF and EOI)

For measurement data where NRDGS > 1, the (CR) and (LF and EOI) is suppressed (between the intermediate outputs) and the data is delimited by a comma.

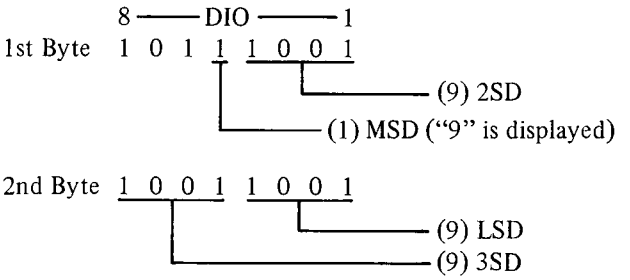
3-22. PACKED. Each data transfer is output as 2 binary bytes. The second byte is concurrent with EOI true.

EXAMPLES:

a. **Normal** (+ 3.24 volts, 10 volt range)



b. **Overload** (+25 volts, 10 volt range)



For measurement data where NRDGS > 1, EOI is suppressed (between intermediate outputs) and the data is not delimited. EOI true is sent concurrent with the second data-byte of the last data transfer. Table 3-2 shows the packed format designators.

3-23. LOCAL. When the 3437A is in remote (not local lockout), pressing LOCAL returns the 3437A keyboard from remote (HP-IB controlled) to local (front panel controlled).

3-24. Programming Instructions.

3-25. The 3437A is a systems instrument intended to be used with the HP-IB (IEEE STD 488-1975 or equivalent) system. The following paragraphs describe HP-IB operation.

Table 3-2. Packed Format Designators.

Byte	Function	DIO 8	7	6	5	4	3	2	1	Description
1st	Range Multiplier	0	1							1 Volt Range
		1	1							1 Volt Range
		1	0							10 Volt Range
	Sign bit			1						Positive
				0						Negative
	MSD				1					Numeric Value of Sampled Input Voltage
					0					
	2 SD					X	X	X	X	
2nd	3 SD	X	X	X	X					
	LSD					X	X	X	X	

3-26. The HP-IB transfers messages (data and commands) between the components of an instrumentation system on 16 signal lines. The interface functions for each system component are performed within the component so that only passive cabling is needed to connect the system. The cables connect all instruments, controllers, and other components of the system in parallel.

3-27. Eight of the lines (DIO 1-8) are reserved for the transfer of messages in a byte-serial, bit-parallel manner. Message transfer is asynchronous, coordinated by the three handshake lines (DAV, NRFD, and NDAC). The remaining five lines are for control of HP-IB activity.

3-28. Devices connected to the HP-IB may be talkers, listeners, or controllers. The controller dictates the roll of each of the other devices by setting the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO 1-8).

3-29. Addresses are set into each device at the time of system configuration. (The 3437A HP-IB address select switch is located on the Logic board.) While the ATN line is true, all devices must listen to the data lines. When ATN is false, only devices that have been addressed will actively send or receive data. All other devices ignore the data lines.

3-30. Several listeners can be active simultaneously but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers are automatically unaddressed.

3-31. Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than allowed by the slowest device presently addressed. This permits several devices to receive the same message byte concurrently.

3-32. The ATN line is one of the five control lines. When ATN is true, addresses and commands are transmitted on seven of the data lines using the ASCII code. When ATN is false, any code of 8 bits (or less) understood by both talker and listener(s) may be used.

3-33. The other control lines are IFC, REN, SRQ, and EOI. IFC (interface clear) places the interface system in a known quiescent state (the 3437A becomes unaddressed to listen, unaddressed to talk, and the serial poll mode (SPM) is cleared). REN (remote enable) is used in conjunction with listen addresses to select either local or remote control of each device. Any device having service request capability can set service request (SRQ) true. This indicates to the system controller that a device on the bus requires attention. EOI (end or identify) is used by a device to indicate the end of a multiple-byte transfer (the 3437A sets EOI true concurrent with the last data-byte of a multiple data-byte transfer). For further information concerning the HP-IB, refer to "Hewlett-Packard Interface. A Compendium of Technical Articles" -hp- publications No. 5952-2472.

3-34. HP-IB Address Selection. A seven-bit binary code forms the complete TALK or LISTEN address of the 3437A. The first five bits of the code (selected by A2S1) are referred to as the instrument address. The remaining two bits (DIO 6-7) are controller originated and define the address to be either TALK or LISTEN. The seven-bit code forms as ASCII character (Table 3-3) that uniquely defines the selected TALK or LISTEN address. Figure 3-2 illustrates the address select switch and address code designators.

3-35. Program Code Set. Program code (an alpha-numeric code representing various instrument functions) is used to control the front panel while the 3437A is in the remote mode of operation. To implement the program code set (Table 3-4), it is necessary for the 3437A to be in remote and addressed to listen.

3-36. The 3437A front panel is designed to imply the program code set. The underlined alpha characters represent the program code alpha symbol for the corresponding instrument function.

EXAMPLE:

The program code string:

D.0025S, N100S, E0S, R3, T2, F1 reads:

1.	DELAY	2.5 ms
2.	NRDGS	100
3.	ENAB RQS	0
4.	Range	10 Volts
5.	Trigger	External
6.	Format	ASCII

It is not necessary to reprogram all functions each time a programming change is made. (The order of program code, and the use of commas is optional.)

Table 3-3. Address Codes.

ASCII CODE CHARACTER		BINARY CODE							OCTAL CODE		5 BIT DECIMAL[3] EQUIVALENT
Listen Address	Talk Address	b_7[1]	b_6	A5 b_5	A4 b_4	A3 b_3	A2 b_2	A1 b_1	Listen	Talk	
SP	@			0	0	0	0	0	040	100	0
!	A			0	0	0	0	1	041	101	1
"	B			0	0	0	1	0	042	102	2
#	C			0	0	0	1	1	043	103	3
$	D			0	0	1	0	0	044	104	4
%	E			0	0	1	0	1	045	105	5
&	F			0	0	1	1	0	046	106	6
'	G			0	0	1	1	1	047	107	7
(	H			0	1	0	0	0	050	110	8
)	I			0	1	0	0	1	051	111	9
*	J			0	1	0	1	0	052	112	10
+	K			0	1	0	1	1	053	113	11
,	L			0	1	1	0	0	054	114	12
-	M			0	1	1	0	1	055	115	13
.	N			0	1	1	1	0	056	116	14
/	O			0	1	1	1	1	057	117	15
0	P			1	0	0	0	0	060	120	16
1	Q			1	0	0	0	1	061	121	17
2	R			1	0	0	1	0	062	122	18
3	S			1	0	0	1	1	063	123	19
4	T			1	0	1	0	0	064	124	20
5	U			1	0	1	0	1	065	125	21
6	V			1	0	1	1	0	066	126	22
7	W			1	0	1	1	1	067	127	23
8	X			1	1	0	0	0	070	130	24[2]
9	Y			1	1	0	0	1	071	131	25
:	Z			1	1	0	1	0	072	132	26
;	[			1	1	0	1	1	073	133	27
<	\			1	1	1	0	0	074	134	28
=	]			1	1	1	0	1	075	135	29
>	~			1	1	1	1	0	076	136	30

[1]Only the first five bits of the binary code are listed. These bits (set by A2S1) are the same for both the TALK and LISTEN address. The sixth and seventh bits (controller originated) determine whether the instrument is being addressed to TALK or LISTEN.

Function	Bit 7	Bit 6
Talk	1	0
Listen	0	1

[2]3437A factory preset address.

[3]Derived from the sum of the binary weighted value of the first five address bits.

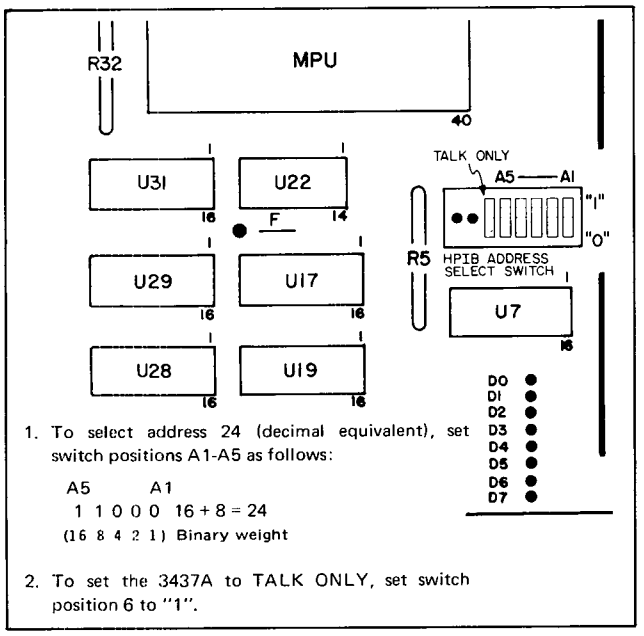


Figure 3-2. Address Select Switch and Address Code Designators.

Table 3-4. 3437A Program Code Summary.

PROGRAMMING CODES[1]		
Program Code (ASCII Character)	Description	Octal Code
D	Delay	104
N	NRDGS	116
E	ENAB RQS	105
S	Store	123
R	Range	122
1	.1 volt	061
2	1 volt	062
3	10 volts	063
T	Trigger	124
1	Internal	061
2	External	062
3	Hold/Man	063
F	Format	106
1	ASCII	061
2	Packed	062
B	Binary Prgm	102

[1]Program Code Handshake occurs with the 3437A in Remote, Addressed to Listen, and ATN false.

3-37. Message Set. Bi-directional traffic over the HP-IB (including program code) is described in terms of messages.

The controller originated messages (commands) are described in Table 3-5 and catagorized as follows:

1. Addressed (Directed to bus devices previously addressed to listen)
2. Universal (Directed to all bus devices capable of responding to the command)

EXAMPLE:

The system controller can configure the 3437A to its initial turn-on state by sending the universal command, Device Clear (DCL), or the addressed command, Selected Device Clear (SDC).

3-38. The 3437A originated messages allow the 3437A to communicate with the system controller, and to participate in the handshake process involved in the data-byte transfer process.

EXAMPLE:

The 3437A can advise the system controller that it requires service by sending the service request (SRQ) message.

Table 3-5. 3437A Message Set Summary Sheet.

Messag	Description	Class	Octal Code	R E N	I F C	Instrument Response
DCL	Device Clear	UC[2]	024	T		The 3437A configures to its initial turn-on state. Volts display (sampled input voltage) Numeric entry display (SEC DELAY) RQS STATUS (DATA READY) DELAY (0) NRDGS (1) ENAB RQS (0) RANGE (10 volts) TRIGGER (INT) FORMAT (ASCII)
SDC	Selected Device Clear	AC[3]	004			If addressed, the 3437A configures to its turn-on state.
GET	Group Execute Trigger	AC	010	T		Is triggered (regardless of trigger mode)
GTL	Go to Local	AC	001	T		Returns the 3437A from remote (HP-IB Controlled) to local (front panel controlled)
LLO	Local lockout	UC	021	T		Disables the Local Key From LLO to GTL to TREN = Remains in LLO From LLO to FREN to TREN = Exits LLO
MLA	My Listen Address	AC				Becomes addressed to listen.
MTA	My Talk Address	AC				Becomes addressed to talk.
UNL	Unlisten	AC	077			Becomes unaddressed to listen.
UNT	Untalk	AC	137			Becomes unaddressed to talk.
SPE	Serial Poll Enable	UC	030			Configures the 3437A into the serial poll mode.
SPD	Serial Poll Disable	UC	031			Exits serial poll mode.
IFC	Interface Clear	}	Single Line MSG		T	Unaddress the 3437A as a talker and as a listener and clears serial poll mode.
REN	Remote Enable	}		T		Programs the 3437A to remote (concurrent with MLA).
				F		Returns the 3437A to local.

[1]All multiline (DIO 1-8) messages are sent with ATN true.
[2]Universal command.
[3]Addressed command.

3-39. The capability of the 3437A as a systems instrument (in accordance with IEEE - 488-1975) is as follows:

SH1	Source	RL1	Remote/Local
AH1	Acceptor	PP0	Parallel Poll
T5	Talker	DC1	Device Clear
L4	Listener	DT1	Device Trigger
SR1	Service Request	C0	Controller

3-40. Binary Program.

3-41. Binary Programming, consisting of a learn mode (3437A to controller) and a program mode (controller to 3437A) provides the following programming capabilities.

3-42. Learn. The learn mode allows the system controller to determine (learn) the programmed state of the 3437A. When interrogated in the learn mode, the 3437A responds by handshaking 7 bytes (completely describing the programmed state of the instrument) onto the HP-IB. The controller, aware of the programmed state of the instrument, identifies the 7 bytes with this programmed state (Table 3-6).

3-43. Program. The program mode allows the system controller to program the 3437A using an abreviated program code (identical 7 bytes received in the learn mode). Since an abbreviated program code is used (compared to the normal ASCII string of up to 25 bytes to accomplish the same function), the 3437A can be reprogrammed in a minimum amount of time.

3-44. The following example illustrates Binary Program mode operation.

EXAMPLE:

1. The 3437A is preset as follows:

DELAY	500 μs
NRDGS	9999
ENAB RQS	2
RANGE	10 Volt
TRIGGER	External
FORMAT	ASCII

Table 3-6. Binary Program Code Designators.

Byte	Function	DIO 8	7	6	5	4	3	2	1	Description
1	Range							0	0	Invalid
								0	1	.1 Volt
								1	0	10 Volt
								1	1	1 Volt
	Trigger					0	0			Invalid
						0	1			Internal
						1	0			External
						1	1			Hold/Man
			(4	2	1)					
	ENAB RQS		0	0	0					Does not request service
			0	0	1					Invalid Prgm
			0	1	0					Ignore Trig
			0	1	1					Invalid Prgm/Ignore Trig
			1	0	0					Data Ready
			1	0	1					Data Ready/Invalid Prgm
			1	1	0					Data Ready/Ignore Trig
			1	1	1					Data Ready/Ignore Trig/Invalid Prgm
	Data Format	0								Packed
		1								ASCII
		(8	4	2	1)					
2	NRDGS	X	X	X	X					MSD
						X	X	X	X	2SD
3		X	X	X	X					3SD
						X	X	X	X	LSD
4	Delay	X	X	X	X					Not Used (May or may not be set)
						X	X	X	X	MSD
5	Delay	X	X	X	X					2SD
						X	X	X	X	3SD
6	Delay	X	X	X	X					4SD
						X	X	X	X	5SD
7	Delay	X	X	X	X					6SD
						X	X	X	X	LSD

2. The system controller programs the 3437A to the Binary Program mode.

   - The 3437A is addressed to listen.
   - The controller handshakes the ASCII character B (102_8) into the 3437A. The Binary Program annunciator is illuminated.

3. The system controller interrogates the 3437A, and the 3437A responds by handshaking 7 bytes (completely describing the programmed state of the instrument) onto the HP-IB (Table 3-7).

   - The 3437A is addressed to talk.
   - When ATN becomes false, the 3437A outputs the 7 bytes onto the HP-IB.
   - The 3437A terminates the Binary Program mode after the 7th byte is output onto the HP-IB.

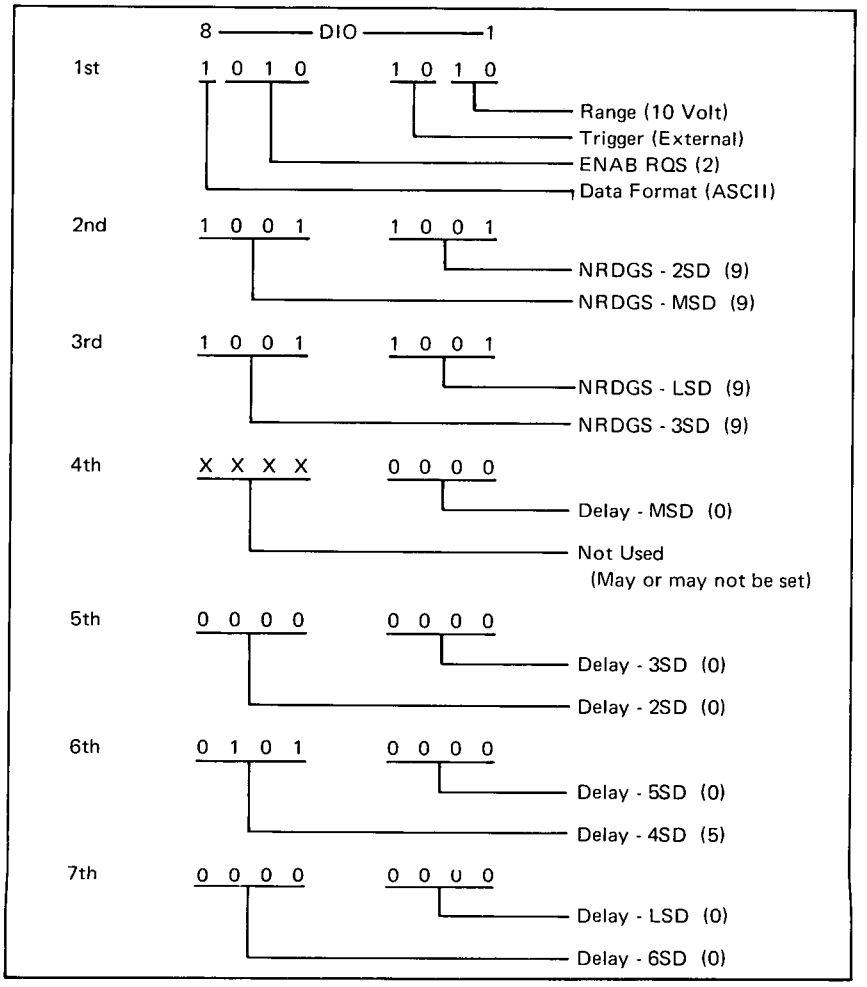
4. The controller stores the 7 bytes, then when required, reprograms the 3437A using the identical 7 bytes. The 3437A responds by reconfiguring to its previous state.

   - The 3437A is addressed to listen.
   - The controller handshakes the ASCII character B (102_8) into the 3437A. The Binary Program mode annunciator is illuminated.
   - The controller handshakes the 7 bytes into the 3437A, reconfiguring the instrument to its previous state.
   - The 3437A terminates the Binary Program mode after the 3437A handshakes the 7th byte.

3-45. Service Request.

3-46. The following events describe the process involving service request (SRQ), serial poll enable (SPE), and serial poll disable (SPD).

Table 3-7. Binary Program Byte Sequence (Example).



a. The 3437A operator defines and programs the service request mask (ENAB RQS).

b. The 3437A sets SRQ true when ENAB RQS (0 - 7) and RQS STATUS (0 - 7) correspond.

c. The controller, programmed to respond to a service request, sets SPE true and conducts a serial poll. When the 3437A is in the serial poll mode and is addressed to talk, the 3437A responds by writing a serial poll status byte onto the HP-IB (Table 3-8).

When the serial poll status byte is output onto the HP-IB, the 3437A clears SRQ.

d. The controller clears SPE by sending SPD.

Table 3-8. Serial Poll Status Byte.

Function	DIO 8	7	6	5	4	3	2	1	Description
ENAB RQS						X	X	X	Binary Code (0-7)[1]
RQS STATUS			X	X	X				Binary Code (0-7)
RQS Bit		X							Identifies the 3437A as the instrument that set SRQ True. (1 α True and 0 α False)
Not Used	X								Don't care.

[1]See Table 3-6.

3-47. APPLICATIONS.

3-48. Introduction.

3-49. The 3437A, although designed as a System DVM, is capable of performing numerous bench (stand-alone) as well as systems functions. The following paragraphs describe some 3437A bench applications.

3-50. Bench Measurements.

3-51. Variable Sample-Rate DVM.

a. The 3437A can be programmed to sample voltages at rates of 100 ms to 1 second. Program the 3437A keyboard as follows:

DELAY. . . . . 100 ms to .9999999 second
NRDGS. 1
RANGE. . . . . .As required
TRIGGER . . . . . .INT

b. The 3437A will sample (and display) the instantaneous value of the input voltage at a rate specified by the programmed delay.

3-52. Time-Selective DVM.

3-53. Oscilloscope Accuracy Enhancement. Oscilloscope measurement accuracy can be enhanced to equal the voltage and delay accuracy of the 3437A. The technique requires that the oscilloscope main gate output (corresponding to start of sweep) externally trigger the 3437A, and that the 3437A Delay out modulate the oscilloscope Z-axis (video) input. The voltage to be measured is connected to both the oscilloscope and 3437A inputs. Each time the oscilloscope is triggered, the oscilloscope main gate output triggers the 3437A, and depending upon the programmed delay, the 3437A samples the input voltage sometime between reoccuring sweeps. Each time the 3437A samples the input voltage, the Delay out (connected to the oscilloscope Z-axis input) is forced low and intensifies the oscilloscope display for the time required to perform the conversion sequence.

3-54. The user views the oscilloscope display, then programs the 3437A delay to intensify the point of interest. The amplitude of the waveform and the lapsed time (from start of sweep to the leading edge of the intensified section) is displayed by the 3437A Volts and Numeric entry displays.

Example:

a. Connect the equipment as illustrated in Figure 3-2.

b. Program the 3437A keyboard as follows:

DELAY. . . . . 3 ms
NRDGS. 1
RANGE. 10
TRIGGER . . . . . EXT

c. Set the 3310A controls as follows:

FUNCTION . . . . . .SQ
RANGE. 10
DIAL 25
DC OFFSET. . . . . OFF
OUTPUT LEVEL . . . . . .MIN

d. Set the oscilloscope controls as follows:

TIME/DIV . . . . . 1 ms
VOLTS/DIV. 1
TRIGGER . . . . . INTERNAL

e. Adjust the 3310A output level, and the oscilloscope trigger and intensity levels to obtain a waveform as illustrated in Figure 3-3.

f. Program the 3437A Delay so that the intensified section appears at the point of interest then read the corresponding magnitude and delay displayed by the Volts and Numeric entry display.

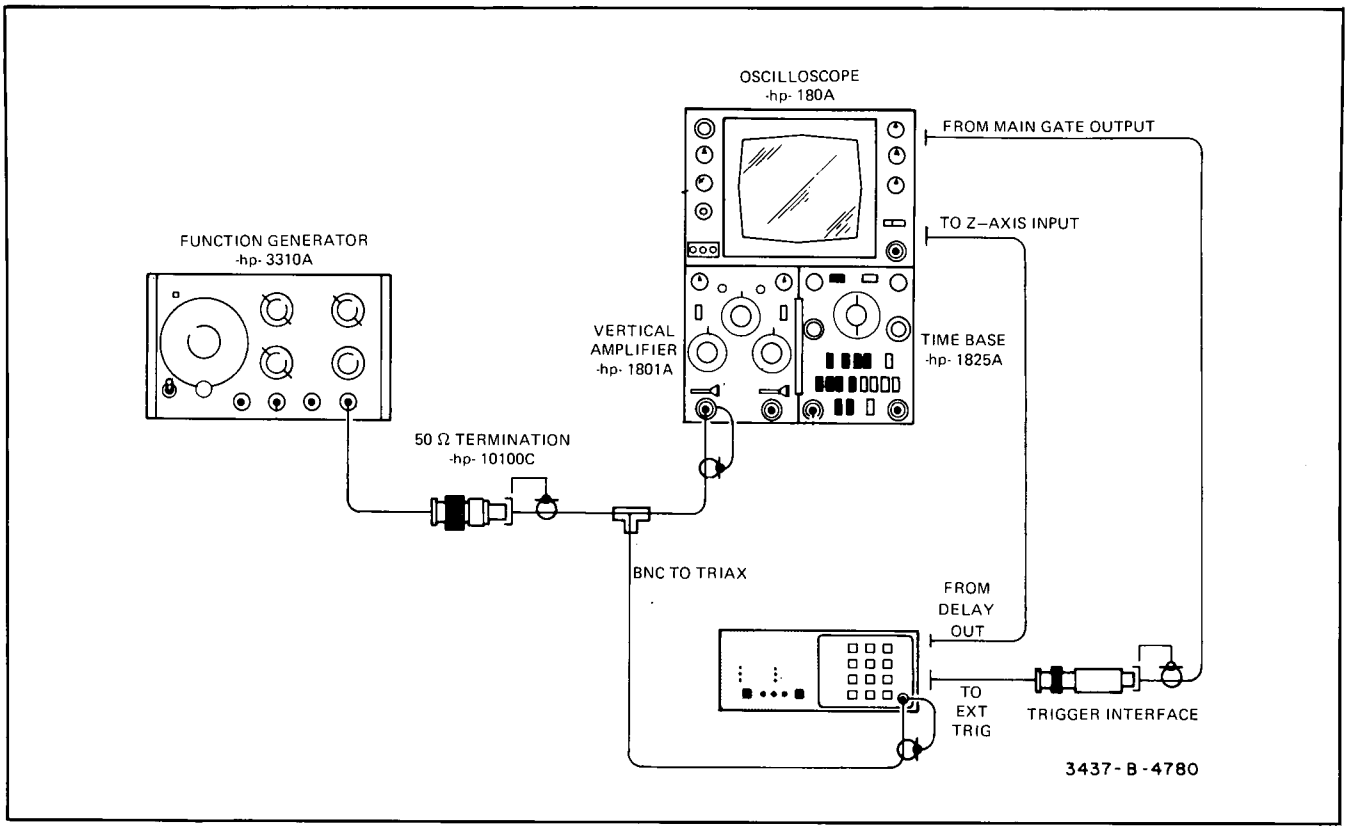


Figure 3-2. Oscilloscope Accuracy Enhancement.

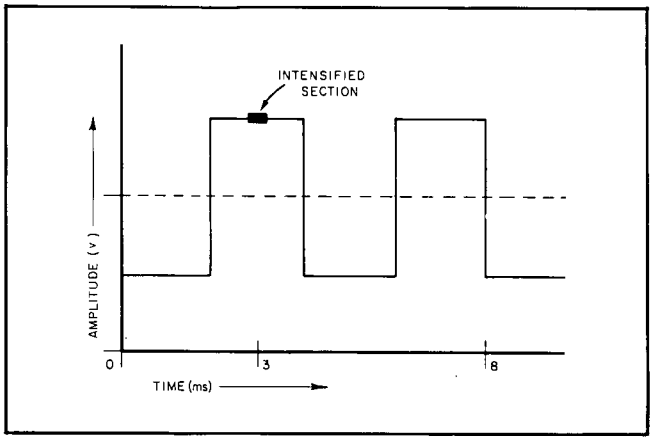


Figure 3-3. Intensified Waveform.

3-55. Delay Generator.

3-56. The 3437A can be programmed to delay an external trigger from 0 to .9999999 sec in 100 ns steps.

Example:

a. Connect the equipment as illustrated in Figure 3-4.

b. Program the 3437A keyboard as follows:

DELAY. . . . . 800 ns
NRDGS. 0
RANGE. . . . . –
TRIGGER . . . . . EXT

c. Set the 3310A controls as follows:

FUNCTION . . . . . .SQ
RANGE. 100
DIAL 10
DC OFFSET. . . . . OFF
OUTPUT
LEVEL. . . . . MINIMUM

d. Set the oscilloscope controls as follows:

TIME/DIV . . . . . 100 μs
VOLTS/DIV (A/B) 5/DC
TRIGGER . . . . . EXTERNAL

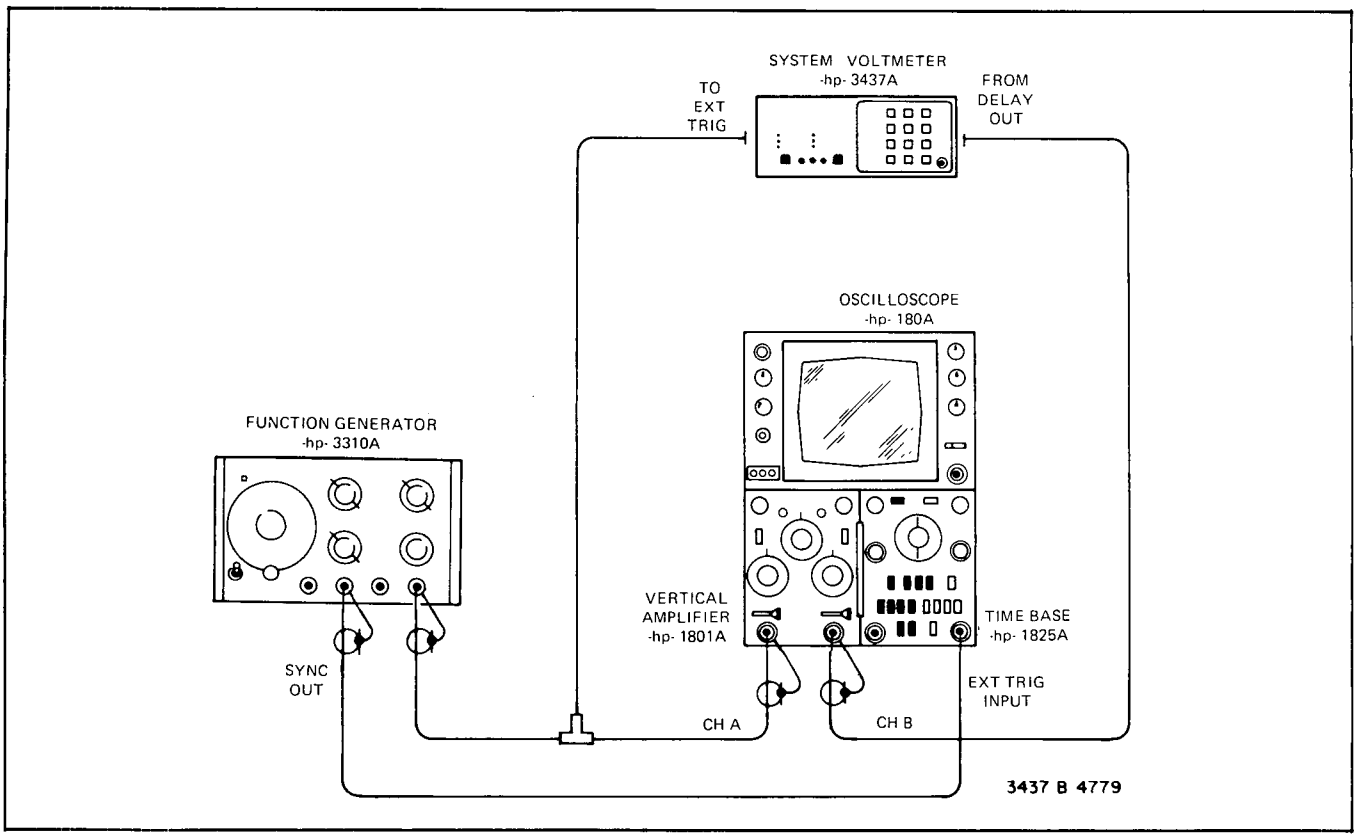


Figure 3-4. Delay Generator.

e. Adjust the 3310A output level and oscilloscope trigger level to obtain a display as illustrated in Figure 3-5. (Assure that the 3310A output is of sufficient amplitude to trigger the 3437A.)

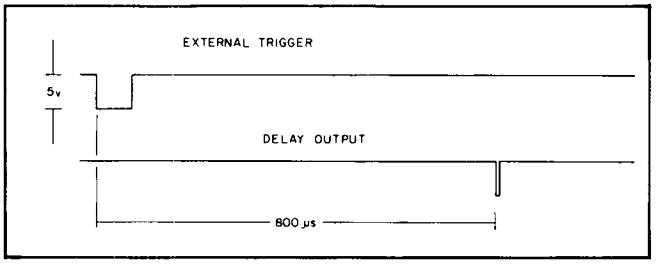


Figure 3-5. Delayed Output.

3-57. Trigger Generator.

3-58. The 3437A can be programmed to function as a trigger generator or as a burst trigger generator (up to 9999 triggers per burst).

3-59. Trigger Generator. Program the 3437A keyboard as follows:

DELAY. 0
NRDGS. 1
TRIGGER . . . . . .INT

a. The Delay out waveform is illustrated in Figure 3-6.

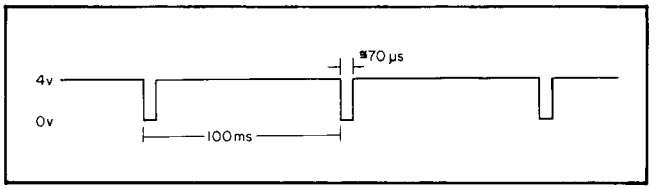


Figure 3-6. Delay Out Waveform.

b. The 3437A Delay can be programmed from 0 to .9999999 second (100 ns step) to provide continuous triggers at rates from 10 Hz to 1 Hz.

3-60. Burst Trigger Generator. Program the 3437A keyboard as follows:

DELAY. . . . . 500 µs
NRDGS. 5000
TRIGGER . . . . . EXT/INT

a. For each trigger received, the 3437A will generate a burst of triggers (5000) at a 2000 Hz (1/500 µs) rate (Figure 3-7). Maximum Rate = 9 kHz.

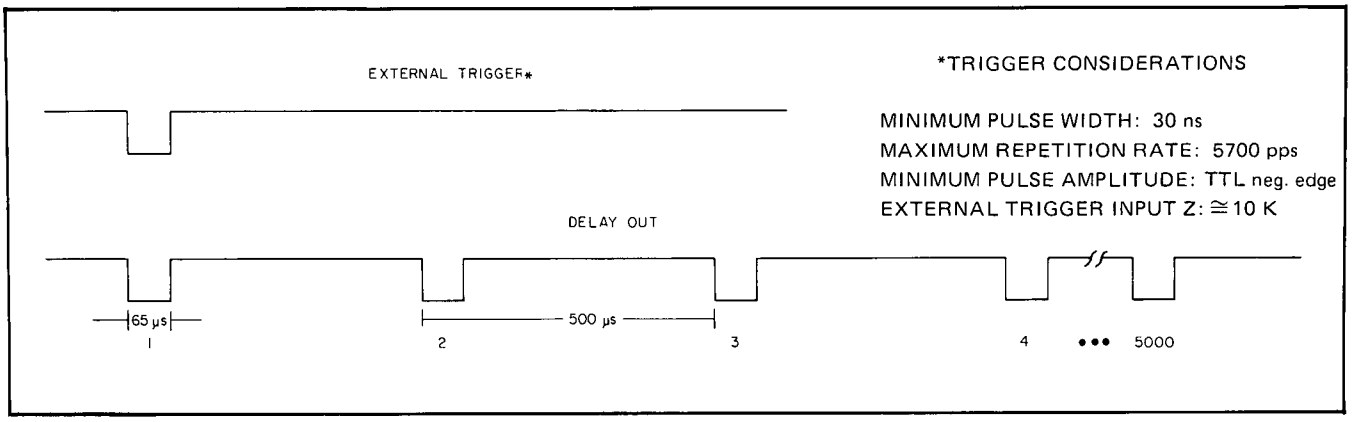


Figure 3-7. Burst Mode Delay Out.

3-61. System Measurements.

Systems Applications include:

- Waveform Analysis
  - Harmonic Content
  - Amplitude Characteristics
- Low Frequency True RMS Measurements
- Transient Characterization

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. The Model 3437A is a Microprocessor controlled, 3-1/2 digit, successive approximation system voltmeter, capable of sampling voltages at rates up to 5700 samples per second.

4-3. Chassis isolated input terminals, a wideband input amplifier, auto-zero, auto-polarity, sample and hold, and 100% overrange on each of the input voltage ranges (.1 volt, 1 volt, and 10 volt) provide floating measurement capability (± 20 V) over the frequency range of DC through 1.0 MHz.

4-4. Hewlett-Packard Interface Bus (HP-IB) capability is standard. All front panel functions are programmable. The output data format is selectable between an ASCII (8 byte) and Packed (2 byte) format.

4-5. The 3437A digital delay logic is capable of delaying an external trigger from 0 – 1 second (100 ns steps), and of generating up to 9999 triggers (for each trigger received) at rates of 1 Hz through 5700 Hz. The internally generated triggers provide a burst sampling capability (up to 9999 samples) at a maximum rate of 5700 samples per second.

4-6. The Binary Program mode provides a means of programming the 3437A using an abreviated program code. When interrogated in the Binary Program mode, the 3437A responds by writing 7 bytes (completely describing the programmed state of the instrument) onto the HP-IB. The controller can use these 7 bytes as an abreviated program code to reprogram the 3437A to its previous configuration.

4-7. Figure 4-1 illustrates the four functional sections of the 3437A. The following paragraphs describe these sections.

4-8. ANALOG SECTION.

4-9. The Analog Section, illustrated in Figure 4-30, accepts input voltages (± 20 volts) over the frequency range of DC through 1.0 MHz. The input voltage is either amplified or attenuated such that a voltage between ± 2 volts (full scale input) is applied to the sample and hold network. The sample and hold network (when put into hold) holds the A/D converter input voltage constant during the analog-to-digital conversion process.

4-10. Input Attenuator (Figure 4-30).

4-11. Depending upon the voltage range selected, the input attenuator provides 0 dB or 20 dB of attenuation. When the .1 volt or 1 volt range is selected, the input voltage is not attenuated. When the 10 volt range is selected (Q2 opens and U1A closes) the input voltage is applied to the amplifier through the resistive divider network and is attenuated by a factor of 10.

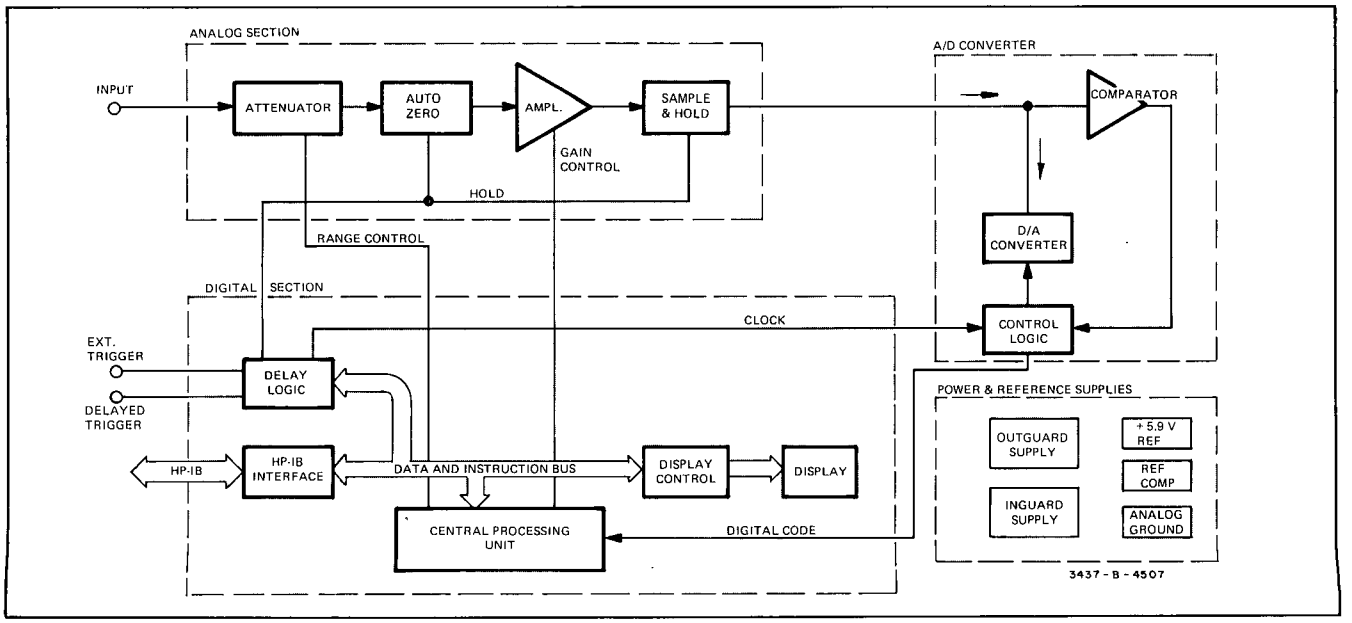


Figure 4-1. 3437A Block Diagram.

4-12. The unity-gain amplifier (U2) compensates for the on-resistance (R_{on}) of $U1_A$ by removing current (current sink) from the junction of $U1_A$ and the bottom of the divider network. The divider current that normally flows through $U1_A$ (10 volt range) is diverted into the U2 network, causing the current through $U1_A$ to be insignificant. The potential difference across $U1_A$ (also insignificant) results in the bottom of the divider being virtually grounded, while R_{on} of $U1_A$ has been effectively eliminated from the resistive divider network.

NOTE

R_{on} (U1A) is approximately 200 ohms, and if not compensated, would cause the attenuator ratio to be in error.

4-13. Auto Zero (Figure 4-30).

4-14. During the measurement cycle, U1 (C/D) isolates the input terminals of the instrument from the amplifier while grounding the amplifier input. The corresponding amplifier output (offset component) is applied through the auto zero path to the negative terminal of the comparator (U13). During this time, the sample and hold output (sum of the amplified input voltage and the offset component) is applied to the positive terminal of the comparator. Since the comparator is concerned with the differential voltage across its input terminals, the offset component (appearing at both terminals of the comparator) does not effect the comparator decision and is effectively removed from the amplified input voltage.

4-15. Input Amplifier (Figure 4-30).

4-16. The input amplifier is a cascode biased operational amplifier that provides voltage gains of approximately 2 or 20. The emitter follower output stage functions as an impedance transformer.

4-17 To protect the input amplifier from overvoltage transients, a protective diode network (CR2, CR38) limits the voltage excursions at the gate of Q3A to about ± 3 volts. The current source (CR6 and R19) sets the stage current of Q3 at an optimum level. Zener diode CR6 effectively maintains a constant voltage across R19 while transistor QA provides reference current for CR6 (Figure 4-2). Common-mode rejection is achieved by using the transistor QA as a high impedance common-mode resistor. The dynamic output resistance of QA absorbs the common-mode input signal.

4-18. Because Q4 and Q5 (cascode transistors) set the gate-drain voltage of Q3 at a fixed level, the signal voltage is developed across the cascode transistors rather than Q3. Keeping the gate-drain voltage of Q3 small (and independent of the input voltage) causes the output impedance to be very large (a necessary requirement to achieve the specified accuracy of the instrument).

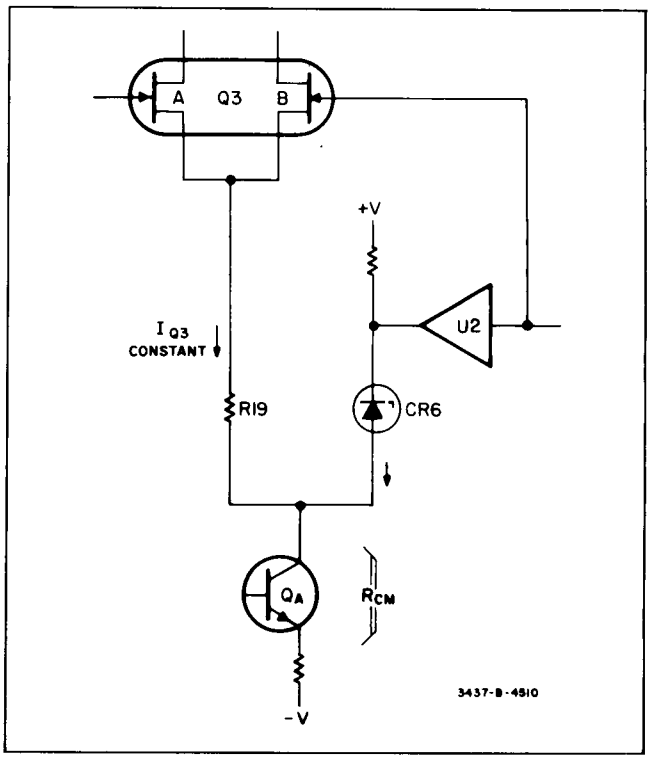


Figure 4-2. Q3 Current Source.

4-19. Voltage follower U3 and Q6 (current mirror) maintain equal potentials across resistors R14 and R15, resulting in balanced currents (minimum offset) through Q3.

4-20. The Amplifier output (level shifted through CR12) is applied to a dual (current-source-biased), emitter follower. The separate sample and hold gate-drive output is necessary to isolate the signal line from voltage transients that occur when the sample and hold network is put into hold. Selection of feedback resistors determines the amplifier gain to be approximately 2 or 20 (Figure 4-3). Small variations of gain, necessary to provide compensation for the reference diode (A1CR19) are accomplished by selecting (factory select) various combinations of binary weighted resistors in the feedback network.

4-21. The diode bridge (CR7 – CR11) limits the maximum feedback potential, assuring the output voltage excursions of the amplifier to be linear and the amplifier overload recovery to be adequate. The voltage across C11 (compensation capacitor) is dependent upon the differential input (Q3) and should not be allowed to become large enough so that the capacitor is not able to recover between sampling periods. (The RC time of C11 and R14 is significant compared to the highest specified operating frequency of the 3437A.)

4-22. Sample and Hold Network (Figure 4-30).

4-23. The Sample and Hold network provides 3-1/2 digit measurement capability over the frequency range of DC through 1.0 MHz (Figure 4-4). When the input voltage is being sampled, Q8 and Q9 are closed, and the sampling

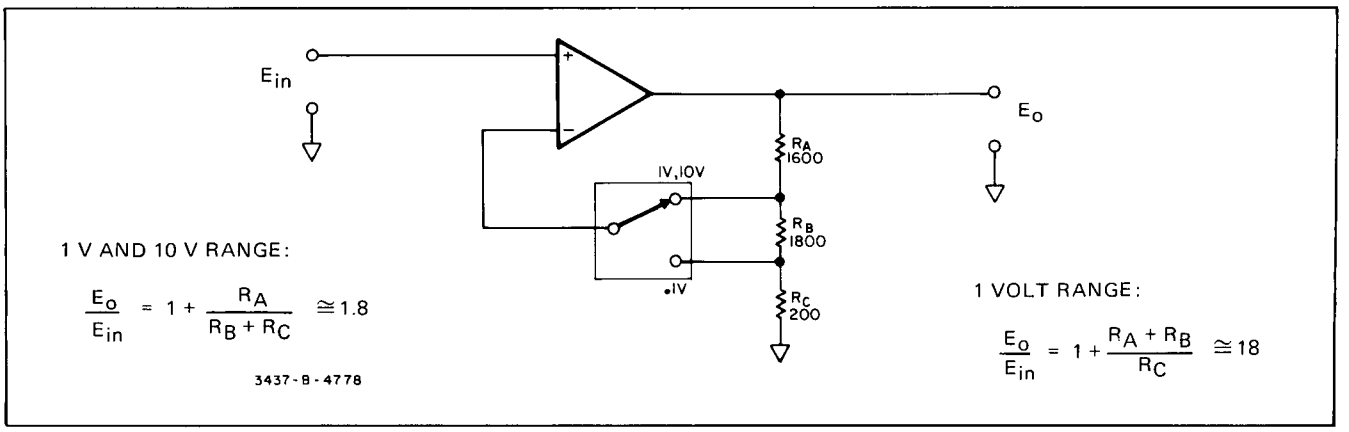


Figure 4-3. Input Amplifier Gain Selection.

capacitor continually tracks the input voltage. During the measurement cycle (Track/Hold line at - 15 volts) Q8 and Q9 open for the time required to digitize the voltage across the sampling capacitor. Although Q9 and C27 could accomplish the sample and hold function, Q8 and C24 provide additional series isolation between the input amplifier and the A/D converter when the sample and hold network is put into hold.

4-24. Charge Transfer Compensation. When the Sample and Hold network is put into hold, the Track/Hold line is gated to - 15 volts. The 15 volt step across the gate-drain junction of Q9 causes the internal gate-drain capacitance of Q9 to charge towards the - 15 volt potential and remove charge (charge transfer) from the sampling capacitor. However, as the Track/Hold line makes the transition between the input signal level and - 15 volts (the zener voltage of CR14 below the sampled input level), CR36 becomes forward biased and clamps the junction of R41 and CR13 at this potential. C25, previously uncharged (both terminals were at the same potential), charges through R42 and R43 towards the sampled input signal level. As the voltage across C25 begins to exceed the voltage at the junction of CR13 and R41, CR13 becomes forward biased, diverting the charging current of C25. The gate of Q9 then becomes clamped to the zener voltage of CR14 below the sampled input voltage.

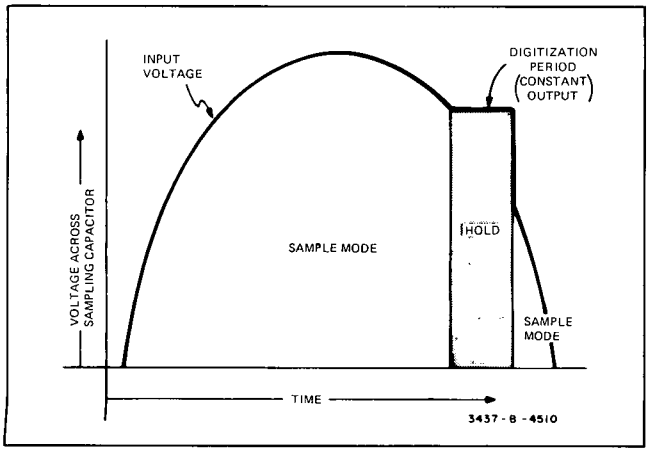


Figure 4-4. Sample and Hold Output Waveform with Sinewave Input.

4-25. Since the voltage across the gate-drain junction of Q9 (zener voltage of CR14) is constant, the charge transfer is also constant and is compensated by the offset adjust of the comparator.

4-26. Transistor Q11 functions as a current-dependent impedance providing a low impedance path for the gate-drive input while the instrument is sampling the input voltage; then during the measurement cycle (when Track/Hold is at line - 15 volts), Q11 provides a high impedance between the amplifier output and the Track/Hold line.

4-27. Analog-to-Digital Converter (Figure 4-30).

4-28. The Analog-to-Digital Converter (consisting of a successive approximation register, digital-to-analog converter, and a voltage comparator) generates a bipolar BCD code that approximates the sampled input voltage. The conversion process requires successive comparisons of internally generated BCD weighted voltage sets against the sampled input voltage (each voltage set is generated in an 8, 4, 2, 1 sequence and collectively represents a significant digit of the display). Since the 3437A is a 3-1/2 digit instrument with auto-polarity, a 14-bit code (14 comparisons) is required to define the sampled input voltage (Table 4-1).

4-29. When the conversion is initiated, the successive approximation register presets Q0 high and the remaining output (Q1 – Q13) low. Succeeding clock pulses cause Q1 – Q13 (in order of ascending bit weight) to be set high, resulting in the generation of BCD weighted voltages. Each weighted voltage is successively compared to the sample and hold output. The comparator (functioning as a null detector) determines which of the two inputs are greater, then outputs a corresponding "keep" or "reject" decision for the successive approximation register. A "keep" decision indicates that the converter voltage is equal to or less than the sampled input voltage, while a "reject" decision implies that the converter voltage is greater than

the sampled input voltage. Depending upon the output of the comparator, the corresponding Q outputs of the successive approximation register appear on the serial-data line as the digital code.

4-30. For conversion of a bipolar analog voltage into a digital code that contains sign information, an offset code is used. The code is offset 2000 counts (1/2 full scale) causing a code of 2000 to correspond to analog zero and a code of all zeros to correspond to negative full scale (Figure 4-5).

NOTE

The 3437A is a 3-1/2 digit (4000 count) instrument, the highest display being ± 1998 or approximately 4000 counts.

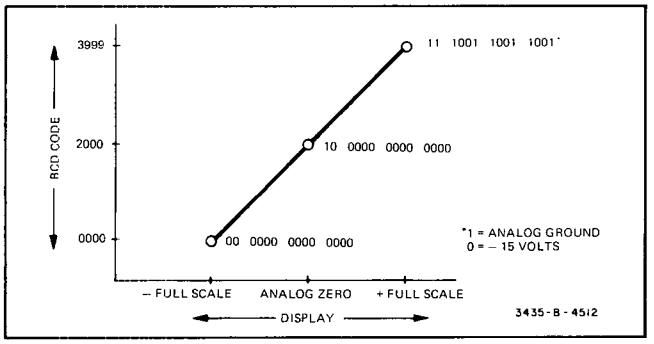


Figure 4-5. BCD Code Offset.

4-31. The conversion process that generates the first four bits of the BCD code (Figure 4-6) is explained in the following paragraphs.

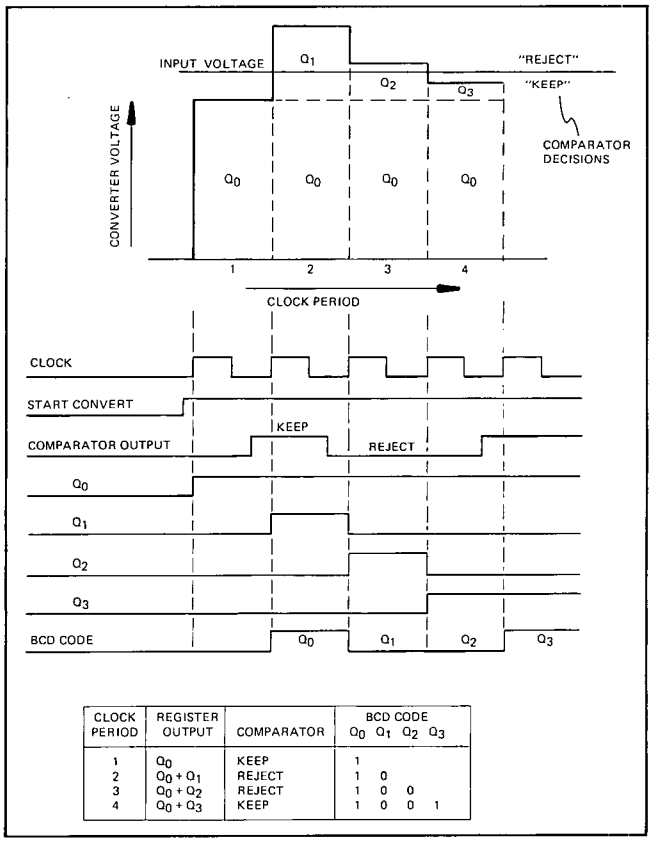
4-32. During the positive transition of the first clock period (after start convert has been initiated), the successive approximation register presets Q0 high and the remaining outputs (Q1 – Q13) low. Q0 set high causes the reference voltage to be switched to the first resistor in the weighted resistor array, resulting in a weighted voltage (-2000counts) being applied to the positive terminal of the comparator. Since the resulting voltage at the positive terminal of the comparator (the algebraic sum of the offset bias, Sample and Hold output, and D/A converter output) is more positive than the negative terminal of the comparator, the comparator outputs a "keep" decision for the successive approximation register.

NOTE

The comparator outputs a "keep" decision (0 volts) if the (+) terminal is more positive than the (-) terminal, and a "reject" decision (- 15 volts) if the (-) terminal is more positive than the (+) terminal.

The "keep" decision conditionally sets Q0 high for the remainder of the conversion sequence (allowing Q0 to make a contribution of - 2000 counts to subsequent comparisons) and causes a "1" to appear on the serial-data line (MSB) during the second clock period. During the positive transition of the second clock period, Q1 is set high. Q1 set high causes the reference voltage to be switched to the second resistor in the array, resulting in a weighted voltage (- 3000 counts) being applied to the positive terminal of the comparator. Since the resulting (+) terminal potential is more negative than the (-) terminal potential, the comparator outputs a "reject" decision for the successive approximation register. The "reject" decision conditionally resets Q1 low (for the remainder of the conversion sequence) and causes a "0" to appear on the serial-data line (2SB) during the third clock period.

4-33. During the positive transition of the third clock period, Q2 is set high. Q2 set high causes the reference voltage to be switched across the third resistor in the array, resulting in a weighted voltage (- 2800 counts) being applied to the positive terminal of the comparator. Since the resulting positive terminal potential is more negative than the negative terminal potential, the comparator outputs a second "reject" decision for the successive approximation register. The "reject" decision conditionally resets Q2 to zero (for the remainder of the conversion sequence) and causes a "0" to appear on the serial data line (3SB) during the fourth clock period. During the positive transition of the fourth clock period, Q3 is set high. Q3 set high causes the reference voltage to be switched to the fourth resistor in the array, resulting in a weighted voltage (- 2400 counts) being applied to the positive terminal of the com-



CLOCK PERIOD	REGISTER OUTPUT	COMPARATOR	BCD CODE Q_0 Q_1 Q_2 Q_3
1	Q_0	KEEP	1
2	$Q_0 + Q_1$	REJECT	1 0
3	$Q_0 + Q_2$	REJECT	1 0 0
4	$Q_0 + Q_3$	KEEP	1 0 0 1

Figure 4-6. BCD Code Generation.

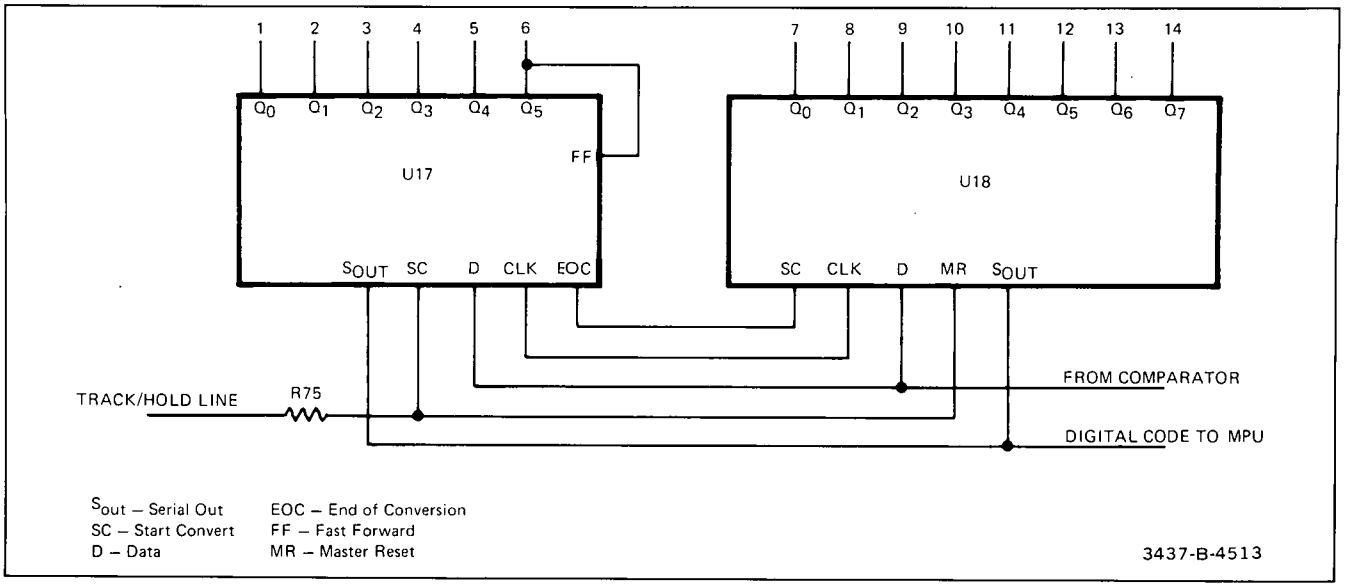


Figure 4-7. Successive Approximation Registers.

parator. Since the resulting positive terminal potential is more positive than the negative terminal potential, the comparator outputs a "keep" decision for the successive approximation register. The "keep" decision conditionally sets Q3 high for the remainder of the conversion sequence and causes a "1" to appear on the serial data line (4SB) during the fifth clock period. The remaining 10 successive approximations are performed in a similar manner. Since data appears on the serial-data line during the clock period following each comparator decision, the complete conversion sequence requires 15 clock periods. Table 4-1 describes the BCD-code designators.

Table 4-1. Code Bit Designators.

Bit Position		Bit Weight (Counts)	Function
1	U17 Q0	2000	Polarity
2	U17 Q1	1000	MSD
3	U17 Q2	800	2SD
4	U17 Q3	400	
5	U17 Q4	200	
6	U17 Q5	100	
7	U18 Q0	80	3SD
8	U18 Q1	40	
9	U18 Q2	20	
10	U18 Q3	10	
11	U18 Q4	8	LSD
12	U18 Q5	4	
13	U18 Q6	2	
14	U18 Q7	1	

4-34. Successive Approximation Register. The successive approximation register provides the digital control and storage necessary to implement the successive approximation conversion process. Two cascaded 8 bit registers, illustrated in Figure 4-7, provide the capability to generate the 14-bit code.

4-35. Digital-to-Analog Converter. The digital-to-analog converter, consisting of a series of SPDT switches and a BCD weighted resistor array, converts the digital output of the successive approximation register to BCD weighted voltage sets.

4-36. SPDT Switches. The converter switches illustrated in Figure 4-8 are used to switch either the reference voltage or ground to resistors in the weighted resistor array.

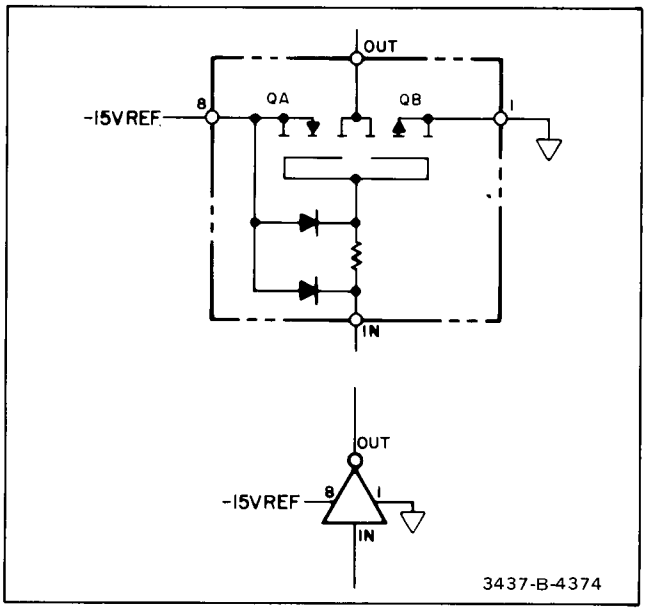


Figure 4-8. D/A Switch.

When the input is high (ground), QA switches the reference voltage to the output, and when the input is low (- 15 V), the output is grounded through QB.

4-37. To compensate for the channel on-resistance (R_{on}) of U14 switches (assuring that - V_{REF} is applied to the

weighted resistor array), U14A is placed in the feedback path of U11B (Figure 7-2) so that - V_{REF} is made more negative by an amount proportional to U14 R_{on}. This technique is effective because the devices in one package are well matched, and the U11B feedback resistors (P/O R58) are selected so that the current through U14A is the same as the current through U14B–F during the conversion sequence.

4-38. R57 and R58, illustrated in Figure 4-9, function as current sources to maintain equal currents through U14, insuring that the voltage across the on-resistances of each switch will be well matched. Since the ratio between the on-resistance of the switch and the corresponding resistor in the array become less significant as the magnitude of the currents become smaller, the compensated reference voltage is only used by the switches (U14) that generate the first four significant currents.

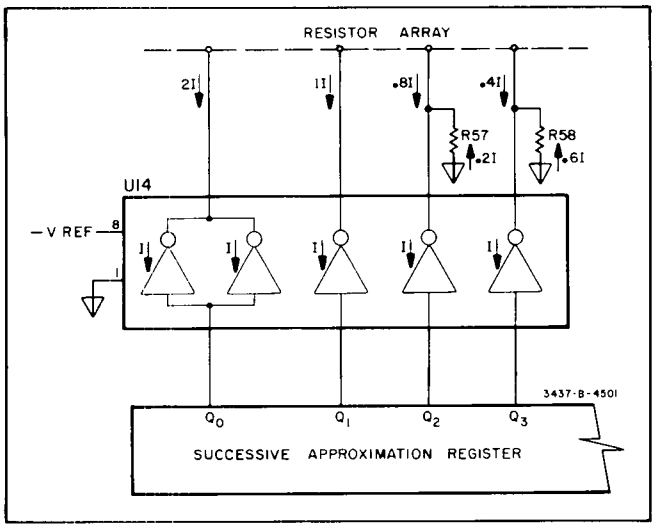


Figure 4-9. U14 Current Distribution.

4-39. Resistor Array. The weighted resistor array, illustrated in Figure 4-10, functions as a current-to-voltage converter by generating the BCD weighted voltage sets. As the successive approximation register causes the reference voltage to be switched to the resistors within the array, the resistance between the negative reference voltage and the positive terminal of the comparator decreases, causing that terminal to become more negative. The negative potential at the (+) terminal of the comparator increases in BCD weighted steps.

4-40. Comparator. The comparator, also illustrated in Figure 4-10, compares the sampled input voltage to the D/A output voltage. Depending upon the largest of the two inputs, the comparator outputs "keep" or "reject" decisions for the successive approximation register which result in the generation of the 14-bit digital code.

4-41. DIGITAL SECTION.

4-42. The Digital Section processes the BCD serial code, writes the code into the digit memory, then displays the contents of the digit memory.

4-43. If the serial code corresponds to a positive input (Polarity Bit "1"), the MPU discards the bit (-2000 counts) and displays the resulting code. If the code corresponds to a negative input (Polarity Bit "0"), the MPU writes a "–" into the digit register, then subtracts the code from 1999 (Figure 4-12).

4-44. If the 3437A is addressed to talk, the contents of the digit memory (sign and magnitude of the sampled input voltage), are written onto the HP-IB. Figure 7-1 illustrates the five functional blocks of the Digital Section. The following paragraphs describe these sections.

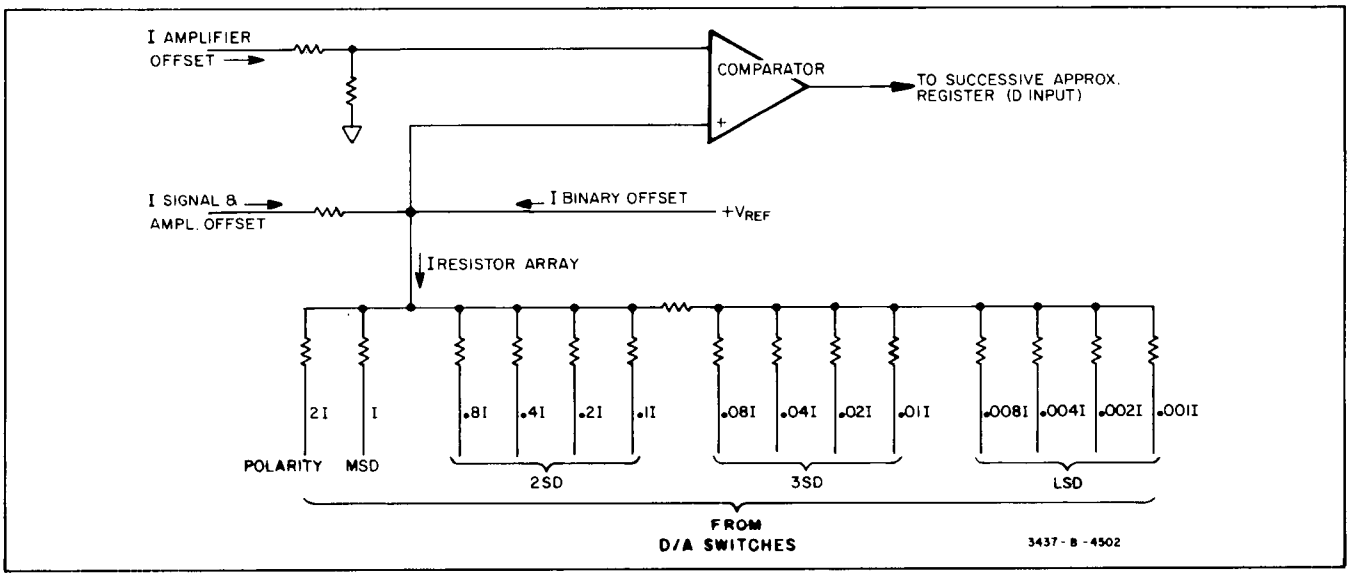


Figure 4-10. Resistor Array and Voltage Comparator.

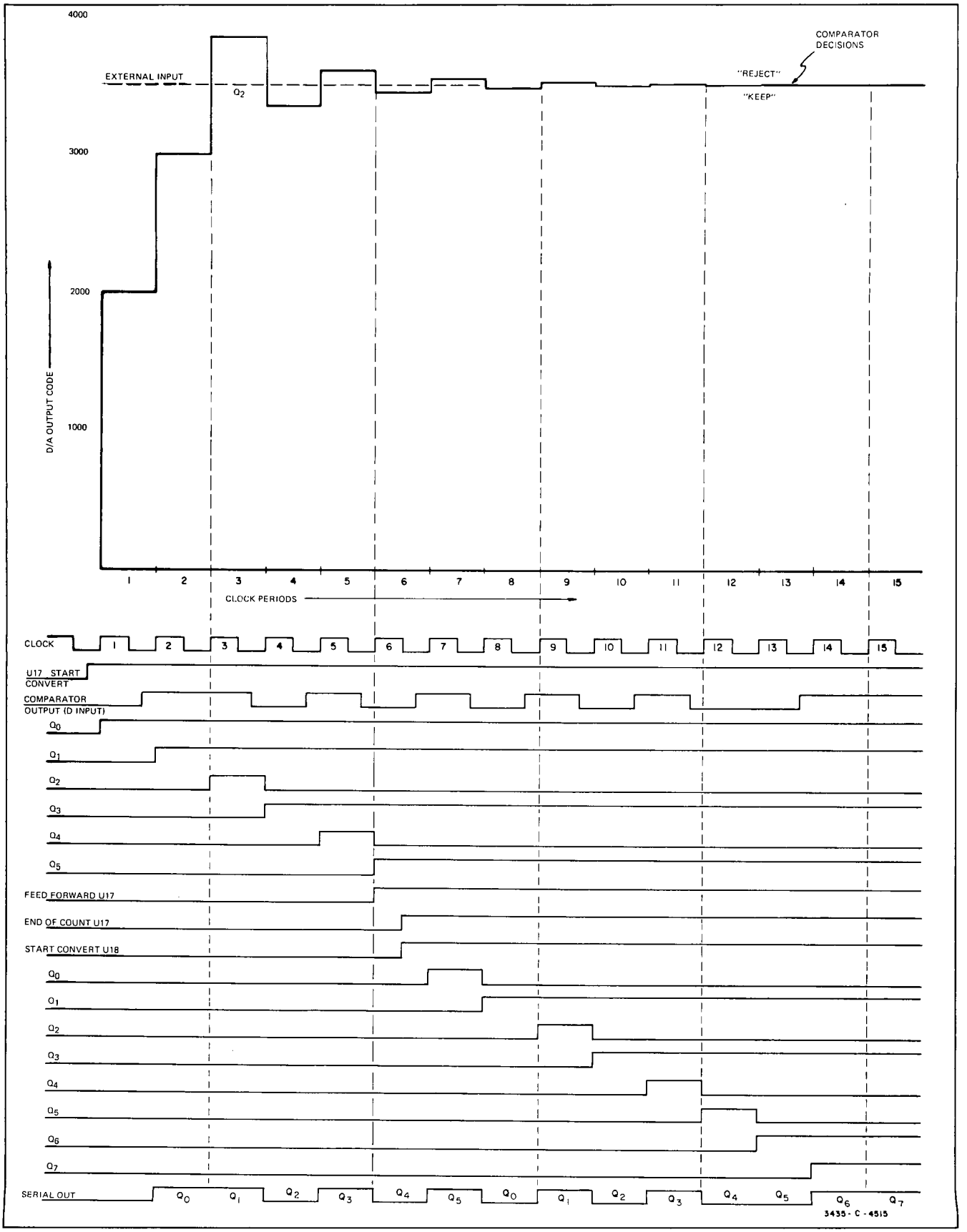
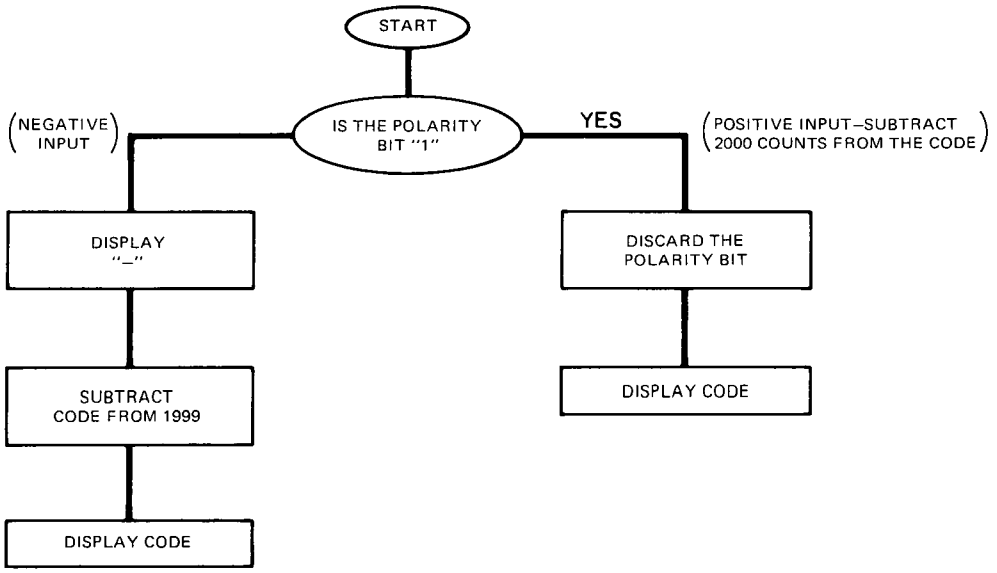


Figure 4-11. Generation of BCD Code Corresponding to an Input Voltage of + 1.533 Volts. (Refer to Table 4-2 for a description of the conversion Process.)

Table 4-2. Event of Conversion Process.

Clock Period	External Input[1] + Code Offset (Counts) A	Successive Approximation[2] Register Output (Counts) B	Comparator Output A ≥ B = Keep A > B = Reject	BCD
1	3553	2000 Q_0	Keep	0[3]
2	3553	3000 Q_0+Q_1	Keep	1
3	3553	3800 $Q_0+Q_1+Q_2$	Reject	11
4	3553	3400 $Q_0+Q_1+Q_3$	Keep	11 0
5	3553	3600 $Q_0+Q_1+Q_3+Q_4$	Reject	11 01
6	3553	3500 $Q_0+Q_1+Q_3+Q_5$	Keep	11 010
7	3553	3580 $Q_0+Q_1+Q_3+Q_5+Q_6$	Reject	11 0101
8	3553	3540 $Q_0+Q_1+Q_3+Q_5+Q_7$	Keep	11 0101 0
9	3553	3560 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_8$	Reject	11 0101 01
10	3553	3550 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_9$	Keep	11 0101 010
11	3553	3558 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_9+Q_{10}$	Reject	11 0101 0101
12	3553	3554 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_9+Q_{11}$	Reject	11 0101 0101 0
13	3553	3552 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_9+Q_{12}$	Keep	11 0101 0101 00
14	3553	3553 $Q_0+Q_1+Q_3+Q_5+Q_7+Q_9+Q_{12}+Q_{13}$	Keep	11 0101 0101 001
15	3553			11 0101 0101 0011[4]

1. An input voltage of + 1.533 volts (1533 counts), added to the 2000 count offset, results in a code value of 3553 counts.
2. All Q's not indicated are logic low.
3. Output inhibited during first clock period. Data appears at serial out during the clock period following each comparator decision.
4. The 2000 count offset is removed prior to display.



EXAMPLE:

INPUT VOLTAGE	SERIAL CODE	MPU ALGORITHM	VOLT DISPLAY
+ 1.532	3532	3532-2000	1.532
+ 0.000	2000	2000-2000	+ 0.000
- 0.000	1999	1999-1999	- 0.000
- 1.532	0467	1999-0467	- 1.532

3437-B-4804

Figure 4-12. MPU Serial-Code-Format Algorithm.

4-45. Central Processing Unit.

4-46. Microprocessor. The microprocessing unit (manufactured by the Loveland Instrument Division) has an internal architecture and instruction set that is optimized toward instrument control and interface.

4-47. MPU Architecture and Supporting Interface Logic. The MPU functional blocks (Figure 4-13) and supporting interface logic are described in the following paragraphs.

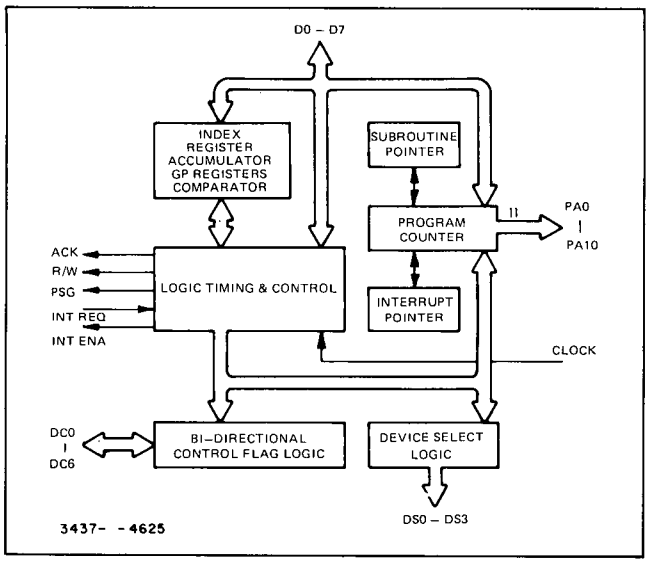


Figure 4-13. MPU Architecture.

4-48. Program Counter. The 11 bit program counter contains the location of the next instruction to be executed from program memory. The program address lines representing the 3 most significant bits (PA8 – PA10) are referred to as the page address, while the remaining 8 bits (PA0 – PA7) form the location of the program instruction within the page. The total 11 bits represent 8 pages of instructions, with each page containing up to 256 words of instructions. The program counter is incremented during each instruction cycle. Each entry into a subroutine or interrupt sequence causes either the subroutine or interrupt pointer to save the current program counter return address. (Two pointers are required in the event the MPU becomes interrupted during the execution of a subroutine.)

4-49. Program Control Memory. The program control memory field is organized as 2048 8-bit words. Individual ROM's are enabled by the program address bus and MPU program source gate (PSG).

NOTE

When PSG is true, the Data and Instruction – Bus Traffic is interpreted as instruction, and corresponds to the contents of the ROM memory location specified by the program counter.

Table 4-3 shows the program steps allocated to each ROM. (ROM enable requires CS1 = CS2 = 0 and CS3 = CS4 = 1).

Table 4-3. Memory Select.

Program Control ROM	Program Step	"1" CS4 #18	"1" CS3 #19	"0" CS2 #20	"0" CS1 #21
U41	0-511	PSG	+ 5 V	PA9	PA10
U42	512-1023	+ 5 V	PA9	PA10	PSG
U43	1024-1536	+ 5 V	PA10	PA9	PSG
U44	1537-2048	PA10	PA9	GND	PSG

Table 4-3 Example: During program steps 1024-1536, Program Control ROM U43 pins number 18 and 19 = logic "1", and pins number 20 and 21 = logic "0". Since the chip select requirement is satisfied, U43 is enabled and the contents of the memory location specified by the program counter, appear on the data and instruction bus during these program steps.

4-50. Control Flags. The seven (bi-directional) MPU control flags are used to:

a. Read the coded serial data (Converter output)
b. Encode interrupt requests
c. Provide the HP-IB/3437A interface

4-51. MPU I/O Capability. The device select output lines (DS0 – DS3) allow the MPU to control various logic devices throughout the instrument. The majority of the device select outputs function as data and instruction-bus traffic controllers, allowing the MPU to read from a device (read the contents of the annunciator memory) or write into a device (write a BCD digit into the digit memory). The device select logic is implemented to provide control of 6 read devices, 8 write devices, and 8 non-read/write devices. Table 4-4 describes the device select functions.

4-52. Table 4-5 shows logic states of the device select outputs.

4-53. MPU Interrupt Capability. The MPU interrupt logic provides the capability of interrupting mainline program execution (when requested) and accessing a service subroutine that provides the required MPU service. An interrupt request is an asynchronous logic state representing combinations of events that result in the need for MPU service. (The valid trigger interrupt request occurs when the 3437A is triggered. Since the 3437A samples the input voltage when triggered, the valid trigger interrupt request calls the service subroutine that controls the A/D conversion sequence.) Since interrupt requests vary in urgency, they are assigned an order of priority. Interrupt requests are read into the MPU over the 8 bit data and instruction bus. The 8 bit format (providing the capability of implementing 256 interrupt requests) sets the program counter to the corresponding subroutine address in program control memory. The 3437A uses seven interrupt request; five are assigned to the HP-IB interface logic, and two are assigned to the delay logic. An eighth interrupt request (invalid interrupt) is provided in the MPU software. The invalid interrupt request is a precautionary measure to guard against an interrupt request that becomes false prior to

Table 4-4. Device Select Functions.

Device Select	Description
DSR1	Read HP-IB Address U7(1)
DSR2	Read Keyboard Data (U21(1)
DSR3	Read Annunciator Memory U38(1)
DSR5	Set Secondary Trigger FF U124A(4)
DSR6	Clear Primary and Secondary Trigger Ignore FF U118A(1)/U124B(14)
DSR7	Read Digit Memory U36(15)
DSW0	Write Data-Byte onto HP-IB U5(11)
DSW1	Write HP-IB Status into Interrupt Encode Logic U6(9)
DSW2	Write Programmed Delay into Preset Registers U101-14
DSW3	Write Digit into Digit Packing Register U37(9)
DSW4	Write Range Bits to Analog Section (Inguard) U100(9) and Trigger Enable to Delay Logic
DSW5	Write Annunciator Memory U39 (3)
DSW6	Write Digit Memory U35(3)
DSW7	Preset Keyboard, Digit, and Annunciator Address U32 (11)
DS10	Increment Keyboard, Digit, and Annunciator Address U32(5)
DS11	Decrement Keyboard, Digit, and Annunciator Address U32(4)
DS12	Clear Primary Trigger FF U119B (9) and Preset Matched Delay FF U121A (4)
DS13	Set Primary Trigger FF U118B (11)
DS14	Clear Secondary Trigger FF U124A(15)
DS15	Clock Successive Approximation Register A2 (R127 and C113)
DS16	Read Data-Byte from HP-IB U3(15)
DS17	Blank Annunciator and Digit Displays A3U1 (14) and U45
	Select READ/WRITE or SCAN address U34(1)

being acknowledged (would only occur during improper HP-IB operation). The interrupt request are shown (in order of assigned priority) in Table 4-6.

4-54. System Clock. The ECL gate (U52A) functions as a linear positive-feedback amplifier, sustaining 10 MHz oscillations by providing positive feedback (non-inverting output) through the 10 MHz crystal. The 10 MHz output is level converted (ECL to TTL) then divided by three. The divider network introduces asymmetry such that the clock period is high for 100 ns and low for 200 ns (Figure 4-14). Transistor Q3 (active pull-up) level translates the 3.33 MHz clock so that clock transitions occur between 0 and + 5 volts.

4-55. Bi-directional Buffers. The bi-directional buffers (controlled by U23) control the direction of the data and instruction-bus traffic, as well as reduce the capacitive loading of the MPU data lines. Table 4-7 shows the buffer control-inputs and corresponding direction of bus traffic.

4-56. Delay Logic.

4-57. The 3437A delay logic, illustrated in Figure 7-1, is capable of delaying an external trigger from 0–1 second (100 ns steps), and of generating up to 9999 triggers (when triggered) at rates of 1 Hz through 5700 Hz. The internally generated triggers provide a burst sampling capability (up to 9999 samples) at a maximum rate of 5700 samples per second.

4-58. The specified delay is preset into down-counters that begin counting towards zero when triggered. When the counters reach a pre-determined count, the delay logic

Table 4-5. Device Select Decoders.

Device Select Control Lines					Device Select Outputs		
DS3	DS2	DS1	DSØ	(Octal)	Read (U26)	Write (U27)	Non I/O (U25)
0	0	0	0	00	– – –	DSW0	HIGH
0	0	0	1	01	DSR1	DSW1	HIGH
0	0	1	0	02	DSR2	DSW2	HIGH
0	0	1	1	03	DSR3	DSW3	HIGH
0	1	0	0	04	– – –	DSW4	HIGH
0	1	0	1	05	DSR5	DSW5	HIGH
0	1	1	0	06	DSR6	DSW6	HIGH
0	1	1	1	07	DSR7	DSW7	HIGH
1	0	0	0	10	HIGH	HIGH	DS10
1	0	0	1	11	HIGH	HIGH	DS11
1	0	1	0	12	HIGH	HIGH	DS12
1	0	1	1	13	HIGH	HIGH	DS13
1	1	0	0	14	HIGH	HIGH	DS14
1	1	0	1	15	HIGH	HIGH	DS15
1	1	1	0	16	HIGH	HIGH	DS16
1	1	1	1	17	HIGH	HIGH	DS17[2]

1. Low True.
2. The quiescent state of DSØ – DS3 and the Read/Write control line is 17_8 and logic "1" respectively (DS17 Enable). Since no read/write functions occur during this time, DS17 is used to unblank the digit and annunciator displays. While read/write functions are in process (DSØ – DS3 $\neq 17_8$), DS17 blanks the digit and annunciator displays to prevent display ghosting.

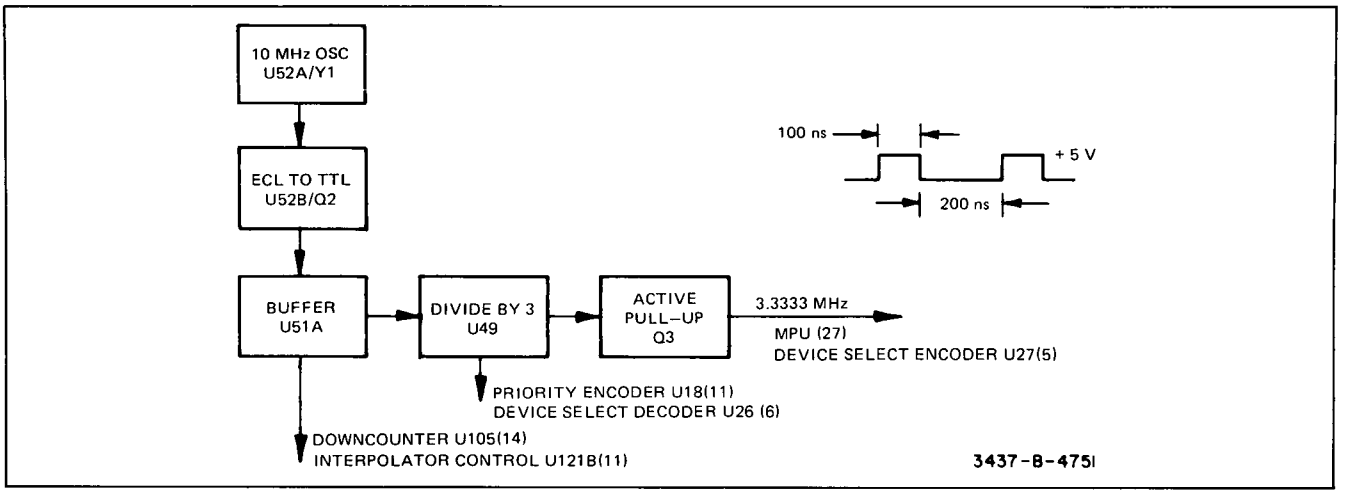


Figure 4-14. 10 MHz System Clock.

Table 4-6. Interrupt Requests.

Interrupt Requests
1. Interface Clear
2. Remote Enable False
3. Valid Trigger
4. Attention
5. Source Handshake
6. Acceptor Handshake
7. Primary or Secondary Ignored Trigger

provides a delayed-trigger to the delayed trigger output connector, sample and hold network, and analog-to-digital converter. If more than one reading is programmed, the downcounters are reset to the original delay, and the process is repeated. When the specified number of readings have been taken, DS12 clears the primary trigger flip-flop, stopping the process. To provide delays (100 ns resolution) for triggers asynchronous to the 10 MHz system clock (100 ns period), an analog interpolator is used. The following paragraphs describe the operation of the delay logic.

4-59. Downcounters. Seven downcounters are cascaded (ripple-carry) to provide delay intervals of 100 ns to 1 second (100 ns steps). U112 counts 100's of ms, and U105 counts 100's of ns. Preset control (p/o U115) controls the state of the downcounters preset line, and U121B controls the state of the downcounter (U105) enable line. When preset is enabled (low true), the contents of the preset registers are written into the downcounters. When preset is released and the enable line is true, the downcounters count toward zero during the 10 MHz clock cycles. The following examples illustrate the downcounter preset and enable functions.

Table 4-7. Bi-directional Buffer Control.

Control Inputs			
R/W	PSG	INT ACK	Bus Traffic
0	0	0	Read[1]
0	0	1	Read
0	1	0	Read
0	1	1	Read
1	0	0	Write[2]
1	0	1	Read
1	1	0	Read
1	1	1	Read

[1]Read into MPU
[2]Write from MPU

4-60. NRDGS = 1 and DELAY > 100 ns. The programmed delay is written into the downcounters prior to receiving the external trigger. Preset-release occurs when the received trigger sets U118B, and downcounter-enable occurs when the subsequent 10 MHz system clock clears U121B. The downcounters then count toward zero on subsequent 10 MHz clock cycles.

4-61. NRDGS > 1 and DELAY ⩾ 175.4 μs. The programmed delay is written into the downcounters prior to receiving the external trigger. The 10 MHz system clock (following the external trigger) clears U121B (enable true and preset false) enabling the downcounters to count towards zero during subsequent 10 MHz clock cycles.

4-62. A counter state of 200 ns forces the detector output high, causing U121B to be set during the positive transition of the subsequent 10 MHz clock cycle (enable false and preset true). The contents of the preset registers are rewritten into the downcounters, and the U121B detector input forces the detector output low. The subsequent 10 MHz system clock clears U121B (enable true and preset false) enabling the downcounters to count toward zero during the 10 MHz clock cycles. A counter state of 200 ns (detector output-high) causes U121B to be set, and the process is repeated.

4-63. Detector. The detector sets the "D" input of U121B to logic "1" (causing U121B to be set during the positive transition of the subsequent 10 MHz clock cycle) for the following conditions:

a. Downcounter state of 100 ns. When a delay of 100 ns is programmed (counters preset to 100 ns), the analog inter-

polator (when triggered) ramps continuously for 100 ns. The detector assures that U121B remains set during the subsequent 10 MHz system clock cycles, so as not to interrupt the ramp mode.

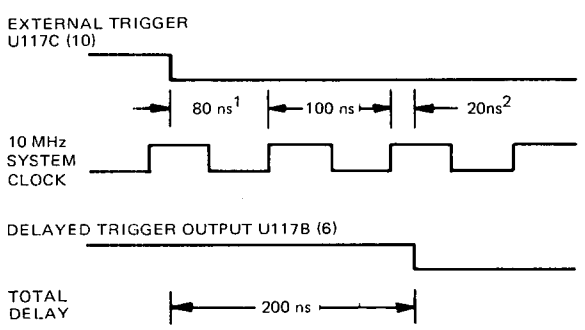
b. Downcounter state of 200 ns and U121B clear.

1. NRDGS = 1 and Delay > 100 ns – Sets U121B to terminate the hold state (CR103 reverse biased).

2. NRDGS > 1 and Delay ⩾ 175.4 μs – Sets U121B to preset the counter chain as well as apply a logic "1" to the (-) terminal of the "OR" comparator to generate a delayed output trigger.

c. NRDGS > 1 and DELAY ⩽ 100 ns – (Invalid Program Condition. Since the programmed delay is less than the time required to complete the measurement sequence.) The detector, along with U114B, toggles the "D" input of U121B on successive 10 MHz system clock cycles. The first time U121B becomes set, the corresponding output of the secondary ignored trigger FF (previously armed by the initial output trigger) generates an ignored-trigger interrupt request, illuminating the ignored-trigger front panel LED.

4-64. Analog Interpolator. The analog interpolator eliminates the potential time quantization error (100 ns) that is inherent between the 10 MHz system clock and external trigger input. Figure 4-15 illustrates the quantization error that occurs when a delay of 200 ns is programmed, and the external trigger is not synchronous to the 10 MHz system clock.



[1] 80 ns (interpolated time) is stored.
[2] 20 ns (100 ns – 80 ns) is added to the stored interpolator time (80 ns) plus the 100 ns clock period.

3437-B-4625

Figure 4-15. Analog Interpolation.

4-65. Refer to Figure 4-14. The time between the external trigger and positive transition of the system clock (quantization error) is measured and stored. The delay logic then begins to count clock periods. After one clock period has lapsed (100 ns), the interpolated time (80 ns) is added to the lapsed clock period plus an additional interpolated time of 20 ns, resulting in a total delay of 200 ns.

4-66. Ramp Comparator. The interpolated interval of 100 ns is determined by the time required for an RC network to charge to a comparison voltage. A comparator senses when the RC network voltage (V ramp) begins to exceed the comparison voltage (V compare) and outputs a negative transition that results in a delayed trigger output. Figure 4-16 illustrates the case where NRDGS = 1 and the specified delay = 100 ns.

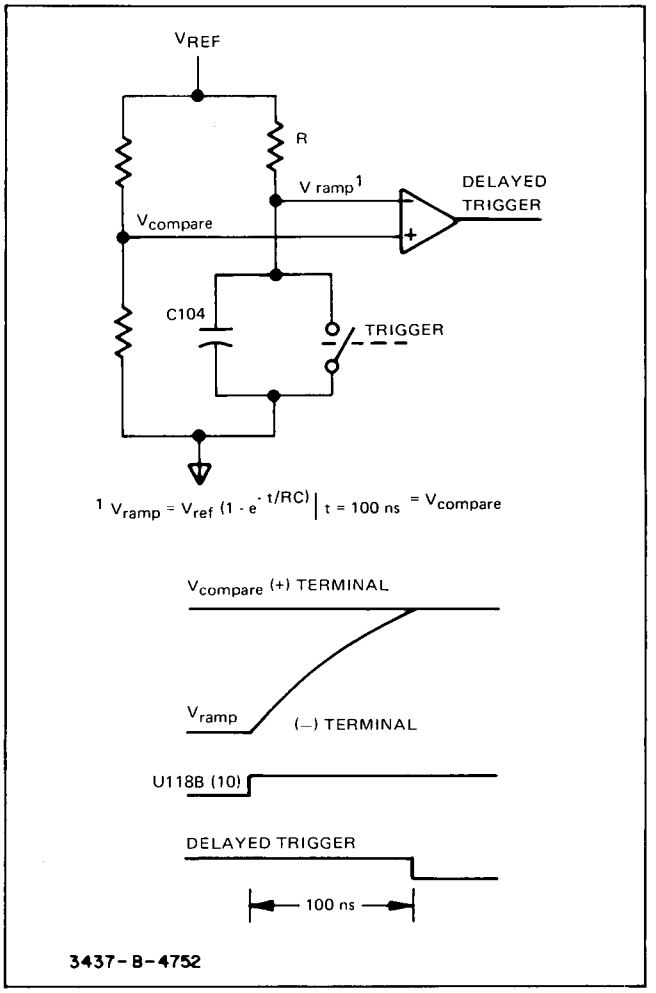


Figure 4-16. NRDGS = 1 and Delay = 100 ns.

4-67. When triggered, C104 begins charging towards V reference. When V ramp begins to exceed V compare (100 ns) the comparator (sensing the voltage change at its input terminals) changes state and outputs a negative transition. (The comparator output polarity corresponds to the polarity of the input terminal that is at the highest potential.)

4-68. If more than 100 ns of delay is programmed, the 100 ns ramp (initiated by the external trigger) is interrupted by the system clock subsequent to the trigger, causing the interpolator go into a hold state. When N-1 clock periods (where N = specified delay in clock periods) have elapsed, the ramp mode is resumed, and C104 continues charging towards V reference. When V ramp begins to exceed V compare, the comparator outputs a negative

transition. Since the ramp takes 100 ns (one clock period) to complete, and the hold state occurs over N-1 clock periods, the total delay (trigger-in to trigger-out) equals an integer number of clock periods. Figure 4-17 illustrates the case where NRDGS = 1 and the specified delay is 300 ns.

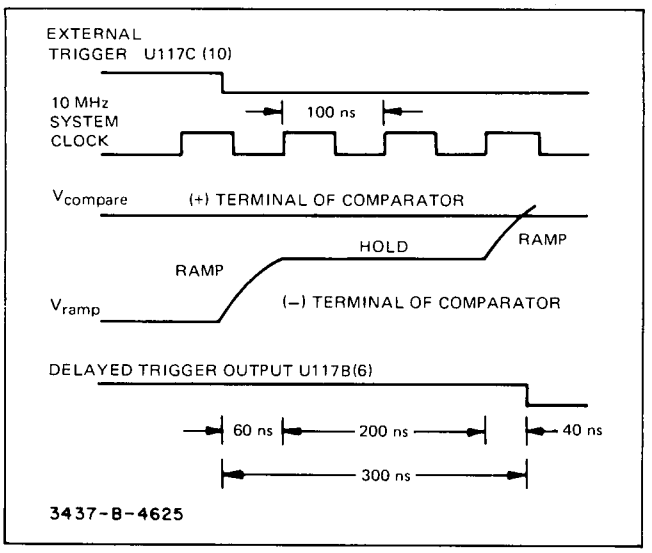


Figure 4-17. NRDGS = 1 Delay = 300 ns.

4-69. When triggered, C104 begins charging toward V reference. The system clock (subsequent to the external trigger) interrupts the charging current (I_{C104}) and initiates a hold state. Since the external trigger preceded the system clock by 60 ns, the voltage across C104 equals 60% of V compare. (Although the voltage across C104 rises exponentially, the section of the ramp used by the interpolator is considered linear.) The hold state is maintained until 2 clock periods (N-1) have elapsed. At the beginning of the third clock period, the hold state is terminated and C104 continues charging towards V reference. Since the voltage across C104 is 60% of $V_{compare}$, an additional 40 ns of charge time is required until V_{ramp} begins to exceed $V_{compare}$. When this occurs, the comparator, sensing the voltage change across its input terminals, outputs a negative transition. The total delay (sum of the incremental delays) equals 300 ns.

4-70. "OR" Comparator. When NRDGS > 1, or zero delay is specified, the analog interpolator/ramp comparator is not used. To assure that the zero delay output is 100 ns less than the 100 ns delay output, an alternate signal path ("OR" comparator) is provided. The "OR" comparator (functioning as an OR gate between U121A/B) provides a signal delay equal to the ramp comparator. The following examples illustrate the function of the "OR" comparator.

4-71. NRDGS = 1 and DELAY = 0. The input trigger (internal, external, or manual) clears U121A, causing the potential at the (+) terminal of the "OR" comparator to change from 5 V to approximately 1.3 V. The potential at the (-) terminal is logic "1" (U121B set). Since the potential at the (-) terminal of the comparator is the highest of the two inputs, the comparator output is forced low (0 delay output). The normally high output state of the monostable (U119A) enables the "OR" comparator output to be applied to the level translator (Q102).

4-72. NRDGS > 1 and DELAY ⩾ 175.4 μs. The monostable (enabled by U100–4 and U118B) fires (for a period of 100 ns) forcing the wired-or output of U123 low (first trigger out). When the downcounters (preset to the programmed delay) reach a pre-determined state (200 ns). U121B becomes set, applying a logic "1" to the (-) terminal of the "OR" comparator forcing a negative transition at the comparator output (2nd trigger out). The downcounters are then preset, clearing U121B ("OR" comparator (-) terminal = logic "0") and the process is repeated. U121B continues to toggle the "OR" comparator output until the specified number of readings have been taken. DS12 then clears U118B (forcing U121B to remain clear) inhibiting additional outputs.

4-73. Analog Interpolator Control Network. The interpolator control network (U121A/B) controls the three operational states of the analog interpolator. Table 4-8 describes the three states.

Table 4-8. Analog Interpolator States.

Interpolator State	Mode
DUMP	Idle – U121A/B Set
RAMP	Active – U121 Set and U121 Clear
HOLD	Static – U121A/B Clear

DUMP – The voltage across C104 is minimal. U121A(Q) functions as a current sink for I dump and I compare.[1]

RAMP – C104 charges towards V reference. I dump = 0. U121A(Q) functions as a current sink for I compare. CR101 and CR102 prevent excessive voltage build-up at U121B(Q).

HOLD – C104 becomes open-circuited. Ramp interrupt gate (CR103) diverts I ramp (I hold = I_{CR103}). U121A(Q) functions as a current sink for I compare.

[1] Diodes DA and DB function as an "OR" gate and provide a path for I compare whether U121A is set or clear. Resistors R108 and R109 set the impedance at U121A(Q) so that I compare remains constant as U121A changes between set and clear.

4-74. Figure 4-31 illustrates the sequence of events occurring during various operating modes of the delay logic.

4-75. Trigger Encode Logic (Interrupt Requests).

4-76. The primary and secondary ignored-trigger flip-flops (U118A and U124B) are used to detect a second trigger (external or internal) occuring prior to completion of the measurement sequence initiated by the first trigger. (The 3437A ignores the second trigger since the measurement sequence initiated by the first trigger is still in progress.)

4-77. When NRDGS > 1 is programmed, the primary ignored-trigger interrupt source (U118A) detects external triggers occuring within a period less than the specified minimum delay, and the secondary ignored-trigger interrupt source (U124B) detects internally generated triggers occuring within a period less than the specified minimum delay. If a second trigger is detected prior to completion of the measurement sequence, an ignored trigger interrupt request is generated. The request calls a subroutine that illuminates the IGNOR TRIG annunciator, and if SRQ is programmed to respond to an ignored-trigger condition, the MPU sets SRQ true.

4-78. The output of U124A (Hold/Start Convert) is also used as the Valid Trigger interrupt request. The subroutine called by this request, controls the measurement sequence. The following paragraphs describe the Ignore and Valid Trigger interrupt-request logic.

4-79. Primary Ignored Trigger Interrupt Request. The external trigger sets the primary trigger flip-flop (U118B) and arms the primary ignored-trigger flip-flop (U118A). If a second trigger occurs prior to completion of the measurement sequence that is initiated by the first trigger, U118A is set and outputs a negative transition (ignored-trigger interrupt request) to the interrupt priority encoder U18(4). (DS12 clears U118B (disarming U118A) at the end of each measurement sequence.)

4-80. Secondary Ignored Trigger Interrupt Request. The delayed trigger that initiates the analog measurement sequence (1st trigger out), sets the secondary trigger flip-flop (U124A) and arms the secondary ignored-trigger flip-flop (U124B). If a second delayed trigger occurs prior to completion of the measurement sequence (initiated by the first trigger) U124B is set and outputs a negative transition (secondary ignored-trigger interrupt request) to the preset (low true) of the primary ignored trigger flip-flop. U118A is then set and outputs a negative transition (ignored-trigger interrupt request) to the interrupt priority encoder U18(4). (DS14 clears U124A (disarming U124B) at the end of each measurement sequence.)

4-81. Valid Trigger Interrupt Request. The valid trigger interrupt request calls the subroutine that controls the analog measurement sequence. The negative output transition of U123 (first trigger out) sets the secondary trigger flip-flop (U124A), causing a negative transition (Valid trigger interrupt request) to be applied to interrupt priority encoder U18 (7).

4-82. HP-IB INTERFACE.

4-83. The HP-IB Interface logic, illustrated in Figure 7-1, consists primarily of interrupt encode logic that monitors the HP-IB Management and Control lines, HP-IB status register, and MPU control flags for combinations of logical states that result in the detection of interrupt requests.

4-84. When a interrupt request is detected, the interrupt encode logic forces one of the five interrupt request lines low. During the subsequent clock period, the interrupt synchronizer latches the interrupt request into the priority encoder. The output of the priority encoder is a three-bit code signifying the highest priority interrupt request currently active. The interrupt acknowledge line (if enabled) reads the interrupt vector (8-bit priority encoder/buffer output) onto the data and instruction bus and into the MPU, resulting in the execution of a corresponding interrupt subroutine (Figure 4-18).

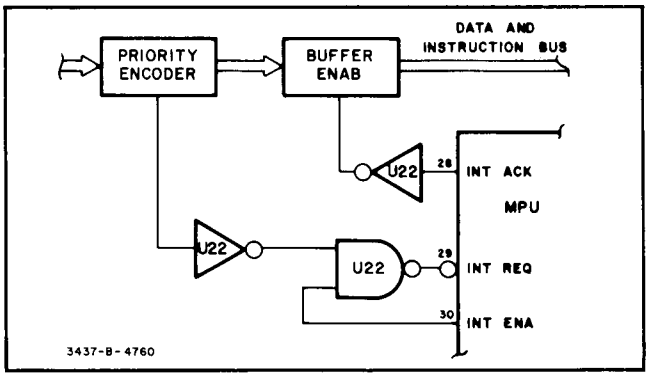


Figure 4-18. Interrupt Enable and Acknowledge.

4-85. HP-IB Interrupt Encode Logic.

4-86. The interrupt encode logic monitors the HP-IB Management and Control lines, HP-IB status register, and MPU control flags for combinations of logical states that indicate a need for MPU service. These MPU service requests (interrupts) are described in the following paragraphs.

4-87. Interface Clear Interrupt Request (LIFC). The interrupt subroutine that is called by the interface clear interrupt request, configures the 3437A to a predefined state (Table 3-5). The logic state of the LIFC interrupt request is:

$$TIFC \times (TATL + TATT + TSPM)$$

Which reads: Interface Clear is true (TIFC) AND the MPU is Addressed to Listen (TATL) OR Addressed to Talk (TATT) OR in the Serial Poll mode (TSPM). Figure 4-19 illustrates the logic implimentation of the interface clear interrupt request.

4-88. Remote Enable False Interrupt Request (LREF). The interrupt subroutine that is called by the remote enable false interrupt request, changes the 3437A from the remote (HP-IB controlled) to local (front panel controlled) mode of operation. The logic state of the LREF interrupt request is:

$$FREN \times (TREM + TLOT)$$

Which reads: Remote Enable is false (FREN) AND the MPU is in Remote (TREM) OR Local Lockout (TLOT). Figure 4-20 illustrates the logic implementation of the remote enable false interrupt.

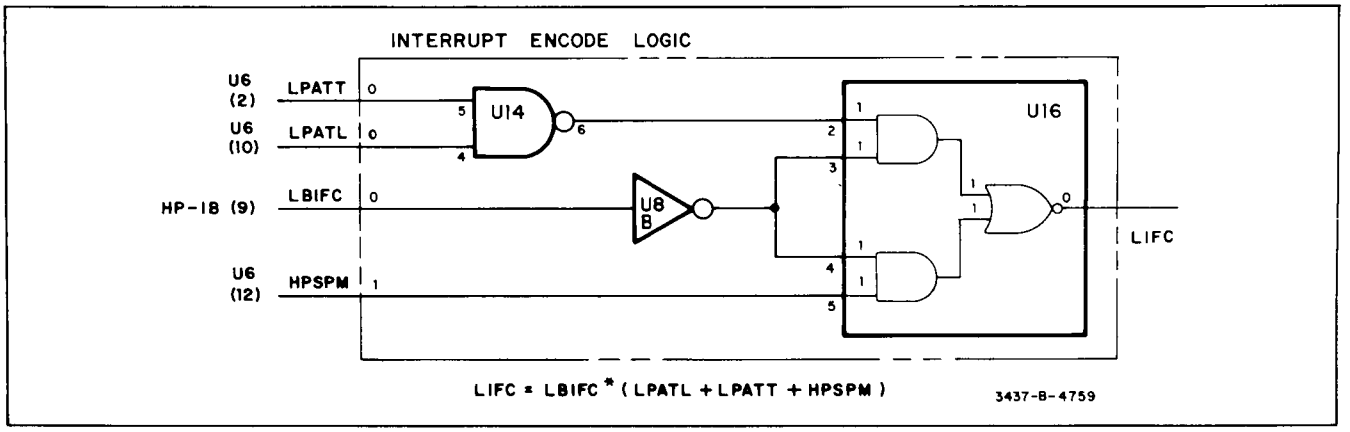


Figure 4-19. LIFC Interrupt Request Logic Implementation.

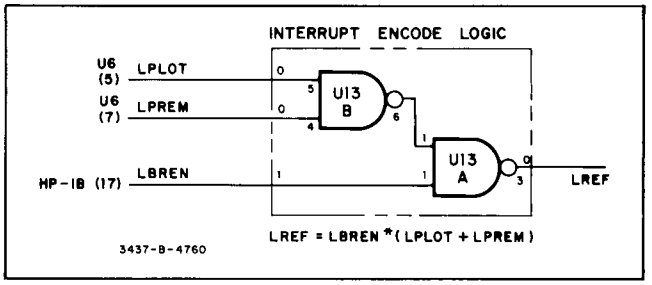


Figure 4-20. LREF Interrupt Request Logic Implementation.

4-89. Attention Interrupt Request (LATN). The logic states of the LATN interrupt are:

1. TATN x TEAI

Which reads: Attention is true (TATN) AND Enable Attention Interrupt is true (TEAI).

2. FATN x FEAI

Which reads: Attention is false (FATN) AND Enable Attention Interrupt is false (FEAI).

NOTE

Since the HP-IB Attention line determines how data on the HP-IB signal lines is to be interpreted, two states are required.

The function of the interrupt subroutine that is called by the attention interrupt request depends upon the interrupt request state.

1. TATN x TEAI (HP-IB Command Mode)

   a. Clears interrupt source (Complements HPEAI).
   b. Configures the 3437A as an HP-IB acceptor.

2. FATN x FEAI (HP-IB Data Mode)

   a. Clears interrupt source (Complements HPEAI).
   b. If addressed to talk, configures the 3437A to talk.

Figures 4-21 and 4-22 illustrate the logic implementation of the attention interrupt requests. (The interrupt encode logic performs an Exclusive OR function on the LBATN and HPEAI signal lines.)

4-90. Source Handshake Interrupt Request (LSHS). The interrupt subroutine that is called by the source handshake interrupt request, controls an interlocked handshake sequence that guarantees the successful transfer of a data-byte from the 3437A (source) to HP-IB acceptor devices. The logic states of the LSHS interrupt request are:

1. TNBA x TRFD x TATT x FATN

Which reads: The MPU has a New Data-Byte Available TNBA) AND all HP-IB acceptors are Ready For Data TRFD) AND the MPU is Addressed to Talk (TATT) AND Attention is false (FATN).

2. TDAC x TDAV x TATT x FATN

Which reads: All HP-IB acceptors have Accepted the Data-byte (TDAC) AND the MPU's Data-byte is Valid (TDAV) AND the MPU is Addressed to Talk (TATT) AND Attention is false (FATN). Figures 4-23 and 4-24 illustrate the logic implementation of the source handshake interrupt requests.

NOTE

Since the source handshake interrupt subroutine involves active participation between the source of the data-byte (3437A), and the acceptor of the data-byte (HP-IB Device), two states are required—the HP-IB controller initiates state 1, then state 2 results from the response of HP-IB devices.

4-91. Acceptor Handshake Interrupt Request (LAHS). The interrupt subroutine that is called by the acceptor handshake interrupt request, controls an interlocked handshake sequence that guarantees the successful transfer of a data-byte from a source (HP-IB device) to the 3437A (acceptor). The logic states of the LAHS interrupt requests are:

1. TDAV x TRFD x (TATL + TATN)

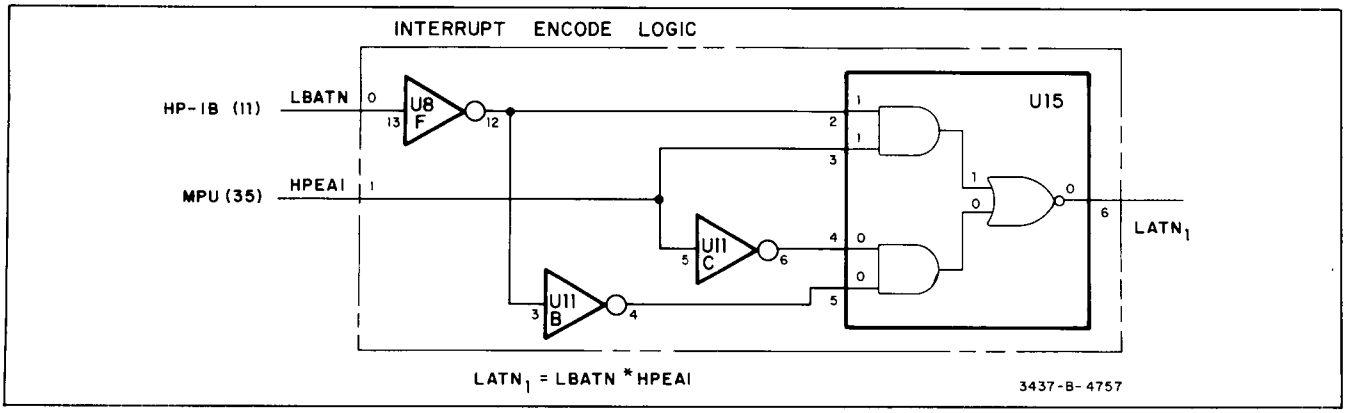


Figure 4-21. $LATN_1$ Interrupt Request Logic Implementation.

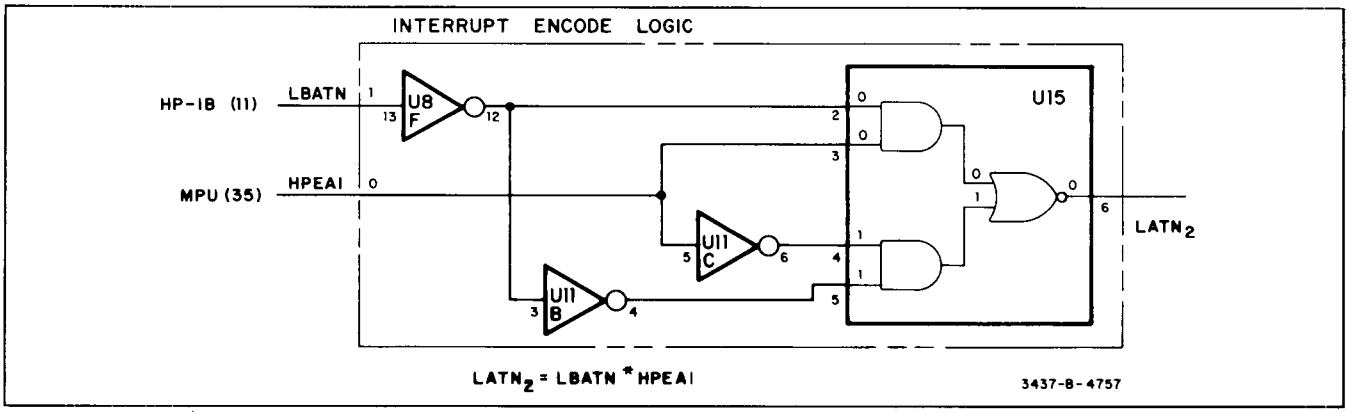


Figure 4-22. $LATN_2$ Interrupt Request Logic Implementation.

Which reads: The HP-IB source indicates the Data-byte on the HP-IB is Valid (TDAV) AND the MPU (acceptor) is Ready For Data (TRFD) AND the MPU is Addressed to Listen (TATL) OR Attention is true (TATN).

2. FDAV x TDAC x (TATL + TATN)

Which reads: The HP-IB source indicates the Data-byte on the HP-IB is not Valid (FDAV) AND the MPU has Accepted the Data-byte (TDAC) AND the MPU is Addressed to Listen (TATL) OR Attention is true (TATN). Figures 4-25 and 4-26 illustrate the logic implementation of the LAHS interrupt requests.

NOTE

Since the acceptor handshake interrupt subroutine involves active participation between the acceptor of the data-byte (3437A) and the source of the data-byte (HP-IB Device), two states are required – the HP-IB controller initiates state 1, then state 2 results from the response of HP-IB devices.

4-92. Bus Transceivers.

4-93. The bus transceivers provide the interface between the HP-IB and 3437A. Transceiver talk-enable (Low True)

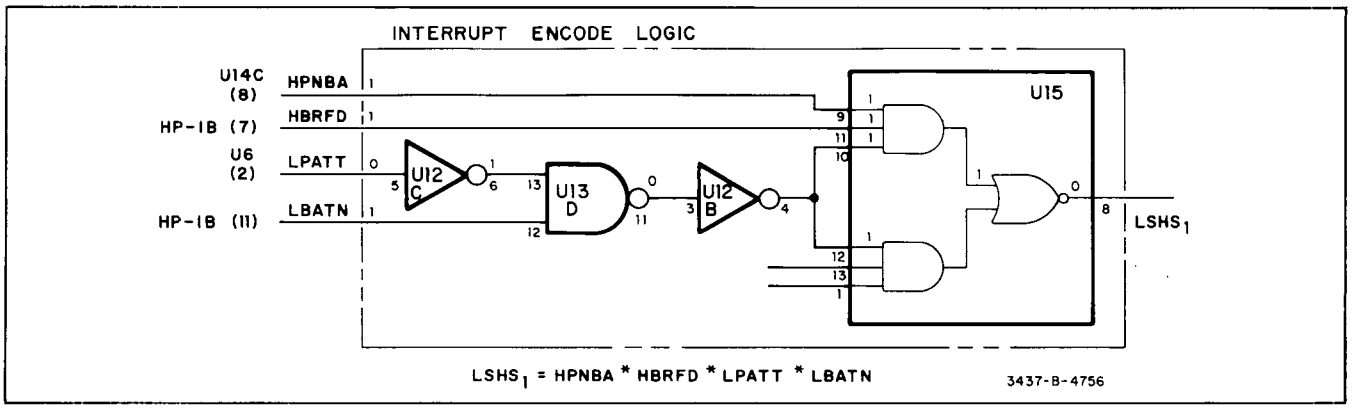


Figure 4-23. $LSHS_1$ Interrupt Request Logic Implementation.

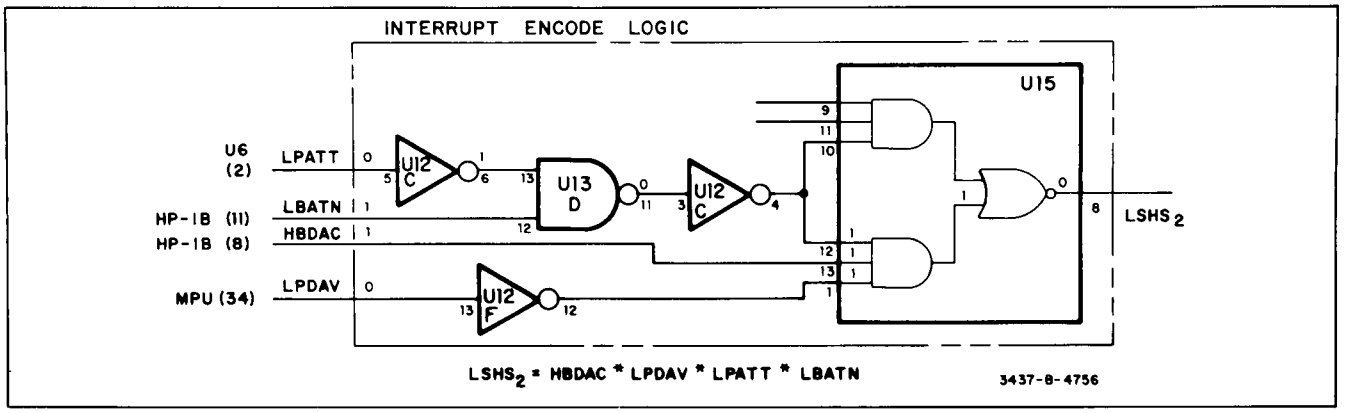


Figure 4-24. LSHS2 Interrupt Request Logic Implementation.

occurs during the logic state (FATN x TATT) which reads: HP-IB is in the Data mode (FATN) AND the 3437A is Addressed toTalk (TATT).

4-94. HP-IB Address Switch.

4-95. The procedure by which the 3437A determines if it has been addressed is as follows. When the system controller sets the ATN interface line true, the resulting 3437A interrupt request (LATN) forces the MPU program counter to access a routine stored in the program control memory that causes the MPU to perform the following sequence of events:

a. Read the DIO1–8 interface lines (DS16), internally storing the results.

b. Read the A2S1 switch setting (through the address buffer A2U7), internally storing the results.

c. Look at DIO5–7 to determine if a listen or talk address group code is present. If so, a comparison of DIO1–5 and A2S1 is performed to determine if the 3437A has been addressed.

4-96. Display and Keyboard Control.

4-97. The Display and Keyboard Control, illustrated in Figure 7-1, uses a scanning technique to enable the front panel annunciators and digit LEDs to display the contents of the annunciator and digit memories. The annunciator and digit memories, and the front panel digit LEDs are simultaneously scanned so that the contents of the memory

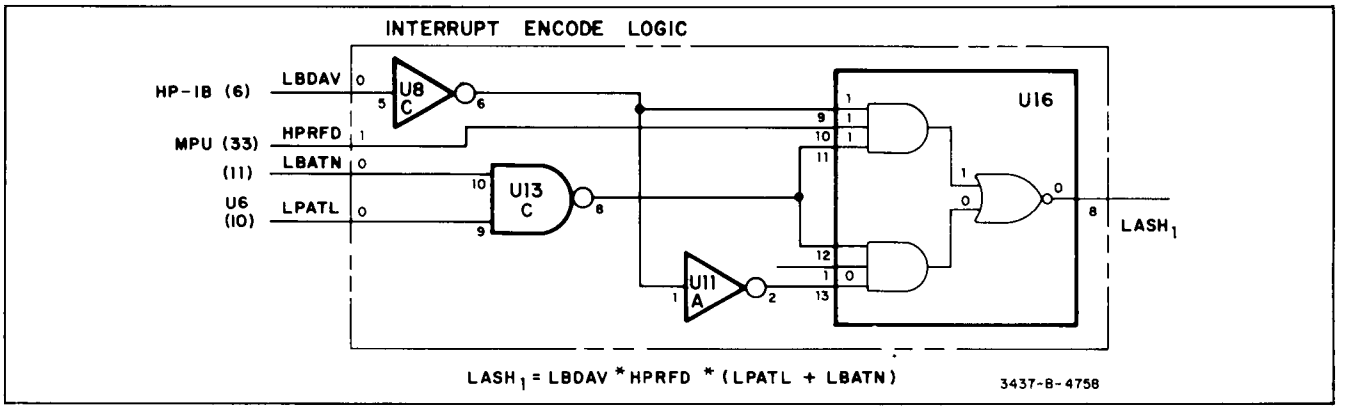


Figure 4-25. LASH1 Interrupt Request Logic Implementation.

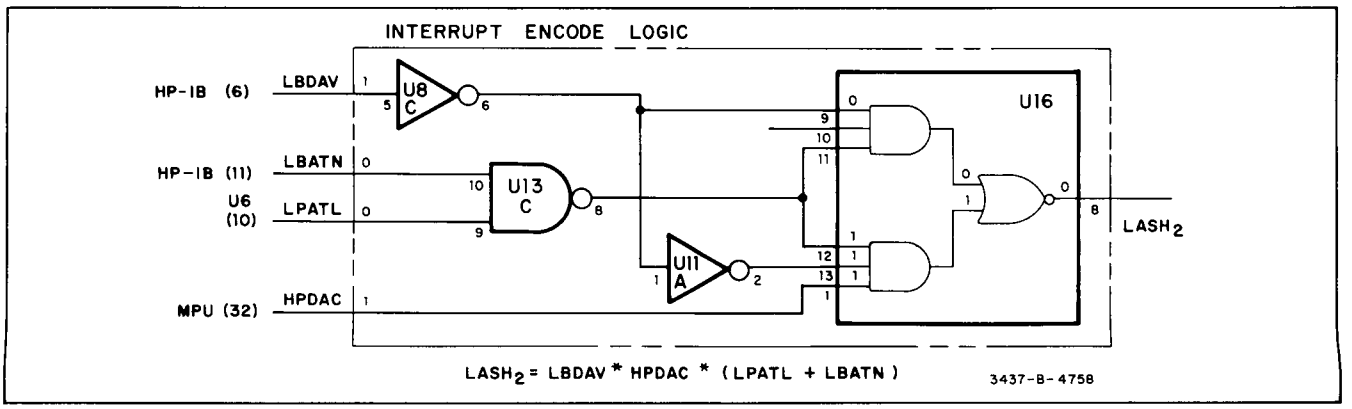


Figure 4-26. LASH2 Interrupt Request Logic Implementation.

locations specified by the scan address are displayed by the front panel annunciator and digit LEDs with addresses identical to the scanned memories. The operational modes (Display, Read, Write) of the Display and Keyboard Control are described in the following paragraphs.

4-98. Display (Annunciator and Digit). The scan clock is a free running multivibrator (1.5 to 2.0 kHz) used to clock the scan counter (a 4-bit counter configured to provide a continuous 14-1 downcount sequence). Since the annunciator and digit memory fields are organized as 14 4-bit words, the 4-bit binary output of the scan counter provides the capability of accessing all words written into the annunciator and digit memories. The scan counter output (designated as the scan address and annunciator and digit scan) is applied to address select (U34) and 4-16 decoder (A3U3) respectively.

4-99. To display the contents of the annunciator and digit memories, address select (U34) applies the scan address to the RAM address select bus, causing the contents of the memory locations specified by the scan address to appear on the annunciator and digit data bus (DS17). The annunciator and digit scan (same source as memory scan) scans front panel annunciator and digit display LEDs, enabling them to display annunciator and digit data.

4-100. Read (Annunciator). When the MPU requires the status of a front panel annunciator, the address counter (U32) is preset to that annunciators memory address (DSW7, DS10, or DS11). The annunciator and digit displays are blanked, and address select (U34) applies the annunciator address to the RAM address select bus (DS17). The annunciator input port (U38) then reads the annunciator word (4-bits) into the MPU (DSR3).

4-101. Read (Digit). When the MPU requires the status of a digit LED, the same sequence as annunciator read is performed. In addition, the MPU writes the first digit word (read from digit memory) onto the packed digit bus DSW3). The address counter is then preset to the second digit memory address, and the digit input port (U36 and p/o U38) reads the first and second digit words (8 bits) into the MPU (DSR7).

4-102. Write (Annunciator and Digit). To change the annunciator LED or digit LED status, the address counter (U32) is preset to the address of the annunciator or digit LED to be changed (DSW7, DS10, or DS11). The annunciator and digit displays are blanked, and address select (U34) applies the annunciator or digit address to the RAM address select bus (DS17). The MPU then writes the new annunciator or digit word into the annunciator or digit memory (DSW5 or DSW6).

4-103. POWER AND REFERENCE SUPPLIES.

4-104. The 3437A uses two independent power supplies (Figure 7-1). The Inguard supply is used by the Analog Measurement circuitry, and the Outguard supply is used by the Digital Logic and Display circuitry. The three reference supplies (located on the Analog board) provide:

a. + 5.9 volt reference.

b. Chassis-isolated analog ground.

c. Compensated U14 (- 14 V) reference.

4-105. Reference Supplies (Figure 4-32).

4-106. The Inguard Power supply uses an active ground. When power is applied to the instrument, the positive and negative output voltages come-up as illustrated in Figure 4-27(a). (The output voltages overlap since Analog ground and the −14 volt output are initially at the same potential.)

4-107. The ground supply (U11A) senses this condition and begins to source current into the analog ground node, causing that node to become more positive. The ground supply continues sourcing current into the ground node until the potential difference between the - 14 volt output and analog ground node is 14 volts (Figure 4-27(b)).

4-108. Refer to the Inguard Power and Reference Supplies Simplified Circuit Diagram (Figure 4-32) for the following discussion.

4-109. Feedback forces the (-) terminals of U12 and U11B to Analog Ground (V_{in} (-)). Since the output of U12 is the sum of V_{in} (-) and V_Z, the current through R_A is directly proportional to the zener voltage of the reference diode CR19 (IR_A = VZ/RA). Since no current flows into the (-) terminals of U11B, $IR_A = IR_B$. The voltage across R_B (VZ/RA*RB volts below V_{in} (-)) is applied to the (-) terminal of U11A. The negative terminal of the bridge (CR205 – CR208) establishes a base potential (V_2) at the (+) terminal of U11A. Negative feedback forces the output of U11A (defined as Analog ground) to a value such that the potential difference across the U11A input becomes zero. This causes Analog ground to be established VZ/RA*RB volts above the base potential applied to the (+) terminal of U11A. (Although VRB is constant, the relative potential between the inputs of the U11 is dependent upon Analog ground since VRB is referenced to analog ground.)

4-110. To compensate for the on-resistance (R_{on}) of the CMOS switches that provide the weighted currents within the D/A converter, the switch reference voltage is increased (made more negative) by an amount proportional to the switch on-resistance. The output of U11B (compensated reference voltage for U14) is level shifted (more negative) from V_2 by an amount proportional to I_{sw} x R_{on} of U14A. Since the ratio between R_{on} of the switch and the corresponding resistor in the weighted resistor array (R58) becomes less significant as the magnitude of the currents become smaller, the compensated reference voltage (- V_{REF}) is only used by switches (U14) that generate the first four significant currents.

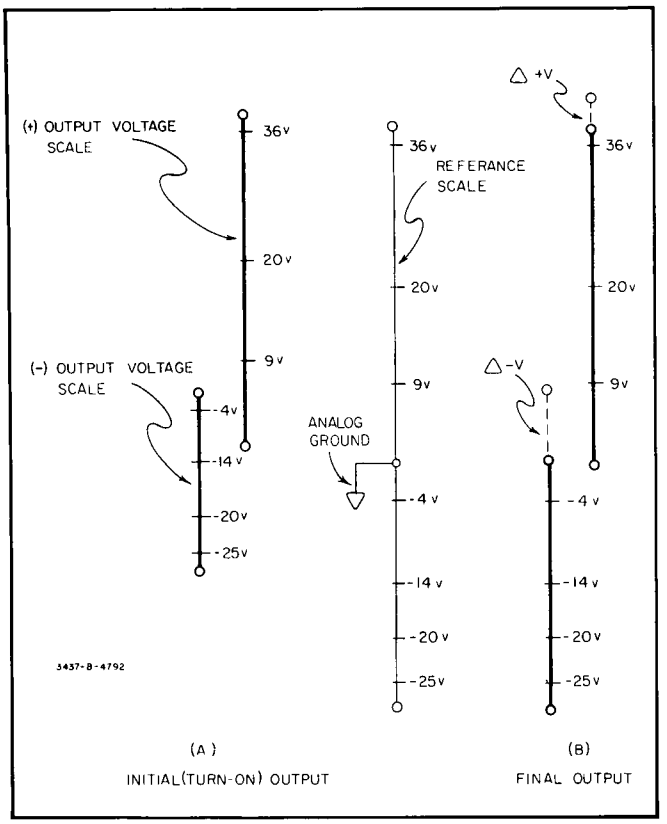


Figure 4-27. Inguard Supply Voltage (Initial/Final).

4-111. Power Supplies.

4-112. Inguard (Figure 4-32).

4-113. (+9 V, - 5 V, - 15 V) Analog ground is established approximately 15 volts above the negative terminal of the diode bridge (CR205 – CR208) making that terminal - 15 volts. Voltage regulation of the 9 volt output is provided by the series pass regulator Q201 and zener diode CR212. The base potential of Q201, held constant at the zener voltage of CR212 above the + 5.9 volt reference, regulates Q201 so that the + 9 volt output is maintained within the specified voltage range. Overcurrent protection is provided by Q202 along with the resistive network R201–R204. During normal power supply operation, the base-emitter voltage of Q201 is divided across R203 and R204, causing Q201 to be biased at + .3 volts. As the load current increases to where the voltage across R201/R202 begins to exceed .3 volts, Q202 becomes forward biased and diverts base current from Q201. Since the supply is current limited at this point, a further decrease in load resistance will cause the + 9 volt output to decrease. The - 5 volt output is provided by zener diode CR217.

4-114. (+ 21 V, + 36 V) Zener diode CR213 level shifts the low terminal of U201 (a three terminal 15 volt regulator) 12 volts above the + 9 volt output. The regulator, providing an output voltage 15 volts above its low terminal potential, provides an output of + 36 volts.

4-115. (- 21 V, - 26 V) The voltage doubler network provides a voltage across C205, enabling zener diodes CR218 and CR219 to provide output voltages of - 21 volts and - 26 volts respectively.

4-116. Outguard.

4-117. (+ 5 V) Operational amplifier U203B provides overvoltage protection for the + 5 volt output (Figure 4-28). The series pass elements and U203B function as a voltage follower, causing the potential at the negative terminal of U203B to appear at the + 5 volt output. Resistor R211 is selected (factory select) so that the (-) terminal of U203B is at + 4.9 ± .11 volts. If the + 5 volt output begins to exceed this voltage, U203B will sense the change on its input terminals. The corresponding U203B output (forward biasing CR206) decreases the base currents of the series pass elements, causing the output voltage to decrease.

4-118. Operational amplifier U203A provides overcurrent protection for the +5 volt output (Figure 4-28). During normal power supply operation, the offset potential across the input of U203A is approximately 100 mV. As the load current increases to where the voltage across the current sense element (L201) begins to exceed the voltage across R235, U203A will sense the change on its input terminals. The corresponding U203A output, (forward biasing CR207) decreases the base currents of the series pass elements, causing the output voltage to decrease.

4-119. (Switched +12 volts) To insure the MPU is initialized (program execution begins at program step zero) when the instrument is turned on, the MPU supply voltages must be applied in a particular sequence. The sequence, illustrated in Figure 4-29, shows that the +5 volt and - 3 volt outputs must be on prior to the + 12 volt output. (The rise time of the + 12 volt output is also specified to be less than 1 μs.) To insure that this sequence is followed, the MPU + 12 volt supply is made dependent upon the + 5 volt output.

4-120. When power is applied to the instrument, a reference voltage (+ 5 volts) generated within U202, is applied to the (-) terminal of the U202 comparator (Figure 4-28). As the + 5 volt output, following the exponential rise of C205 comes within 200 mV of the + 5 volt reference, the comparator begins to change state (negative to positive), enabling the switch and causing + 12 volts to be applied to the MPU.

4-121. As the switched 12 volt output begins to exceed + 5 volts, the potential at the junction of R231 and R232 increases, causing the comparator to change states within a period of time such that the switched 12 volt output has a rise time of less than 1 μs.

4-122. Fan Control.

4-123. The fan control network is a three-stage ring-counter producing a rotating magnetic field about the rotor of the fan motor. The CEMF developed across each

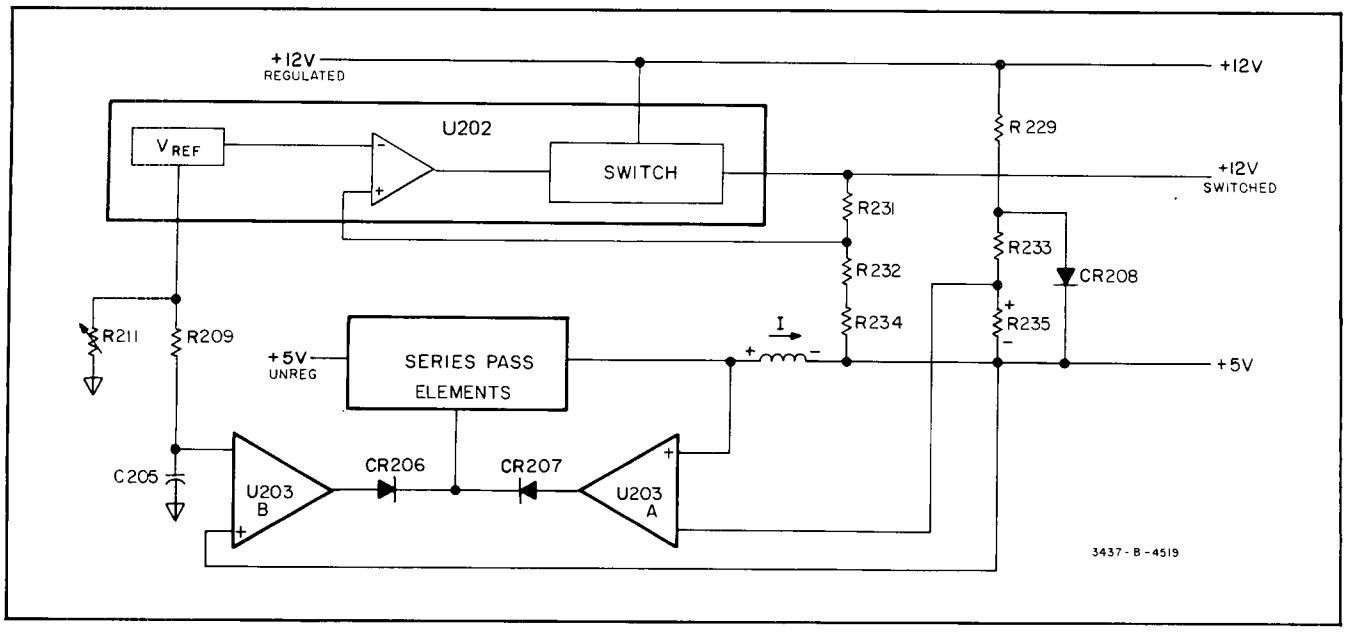


Figure 4-28. Overvoltage and Overcurrent Protection of the +5 Volt Output.

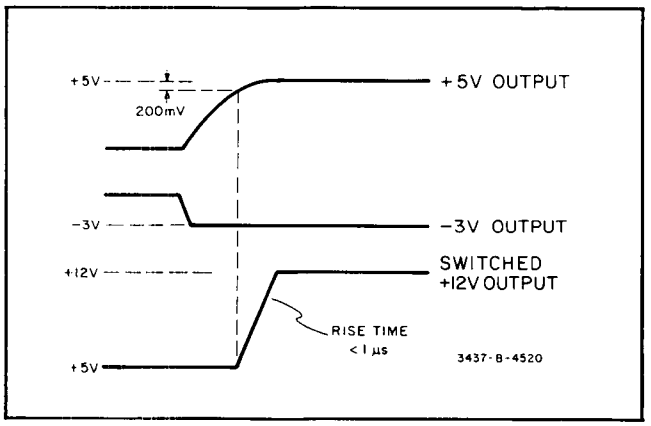
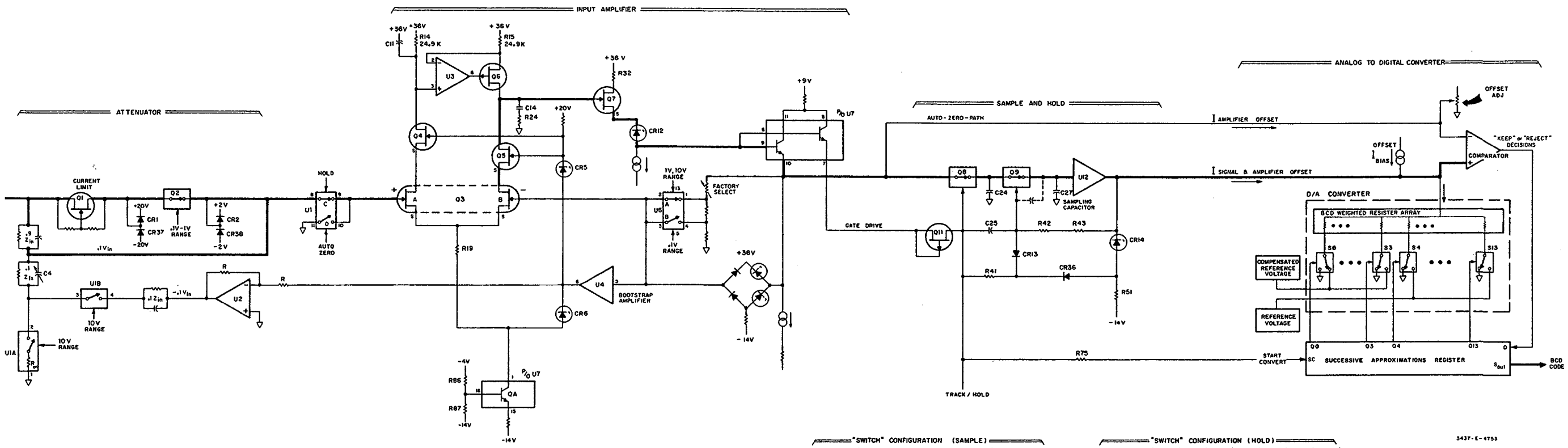


Figure 4-29. MPU Power-On Sequence.

field winding as the rotor aligns itself with the rotating field, stabilizes the counter frequency at about 88 Hz, resulting in a motor speed of about 5300 RPM. Since the power to the fan is unregulated, its speed increases with increasing line voltage.



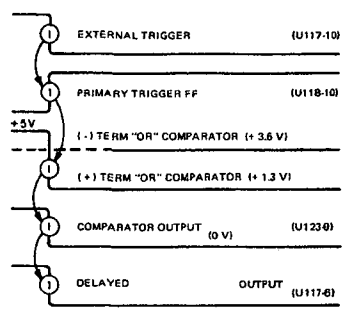
			"SWITCH" CONFIGURATION (SAMPLE)									"SWITCH" CONFIGURATION (HOLD)								
RANGE	ATTEN	GAIN	U1A	U1B	Q2	U1C	U1D	U6A	U6B	Q8	Q9	U1A	U1B	Q2	U1C	U1D	U6A	U6B	Q8	Q9
0.1	1	20	0	0	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0
1.0	1	2	0	0	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	0
10.0	10	2	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1	0	0	0

Figure 4-30. Analog Measurement Circuitry Block Diagram.

CASE I

NRDGS = 1
DELAY = 0

"OR" comparator provides output. Downcounters and Analog interpolator/ramp comparator are not used.



SEQUENCE OF EVENTS:

1. Primary trigger FF (U118B) is set.
   - Dump control FF (U121A) is reset.
   - The (+) terminal of the "OR" comparator changes from +5 V to +1.3 V.
   - Ramp control FF (U121B) remains set and applies +3.6V to the (-) terminal of the "OR" comparator.
   - The "OR" comparator (U123) output is forced low.
   - The comparator output (pulled down by Q102) sets U124A, Q103 switches +5 V to the successive approximation clock-transformer. U124A also forces the output of U117B low, resulting in a delayed trigger out.

[1]External trigger is asynchronous to system clock. In this example the external trigger leads the positive transition of the system clock by 75 ns.

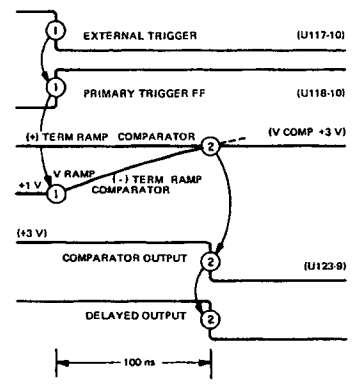
[2]This illustration (an ignore trig condition) is for instruction only.

[3]The comparator output (pulled down by Q103) set U124A, Q103 switches +5 V to the successive approximation clock - transformer. U124 also forces the output of U117B low - resulting in a delayed trigger out.

CASE II

NRDGS = 1
DELAY = 100 ns

Analog interpolator/ramp comparator provides 100 ns delay. Downcounters and "OR" comparator are not used.



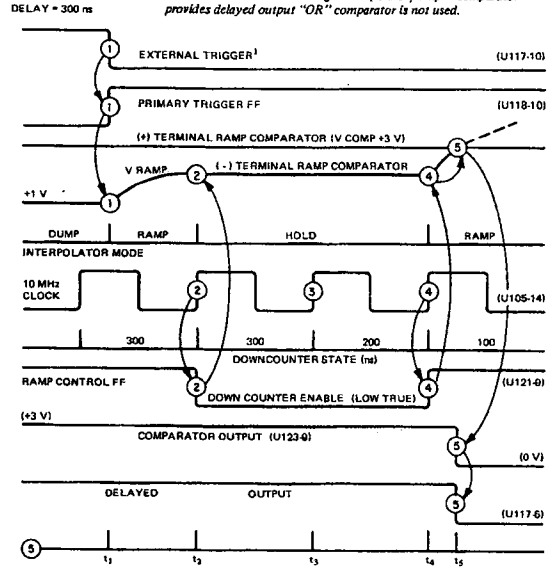
SEQUENCE OF EVENTS:

1. Primary trigger FF (U118B) is set.
   - Dump control FF (U124A) is reset. Dump mode terminates.
   - C104 begins charging towards +12 V.
   - Ramp control (U124B) remains set. (Detector output (U114-10) is high.)
   - Ramp comparator output remains enabled by U115 (6).
2. When V ramp begins to exceed V comp, the comparator output is forced low. (The "OR" comparator output was forced low when U121A was reset. However, the wired - or output (U123-9) remained high since the ramp comparator output, (V compare) was high.
   - The comparator output (pulled down by Q103) sets U124A. Q103 switches +5 V to the successive approximation clock - transformer. U124A also forces the output of U117B low resulting in a delayed trigger out.

CASE III

NRDGS = 1
DELAY = 300 ns

Downcounters and Analog interpolator/ramp comparator provides delayed output "OR" comparator is not used.



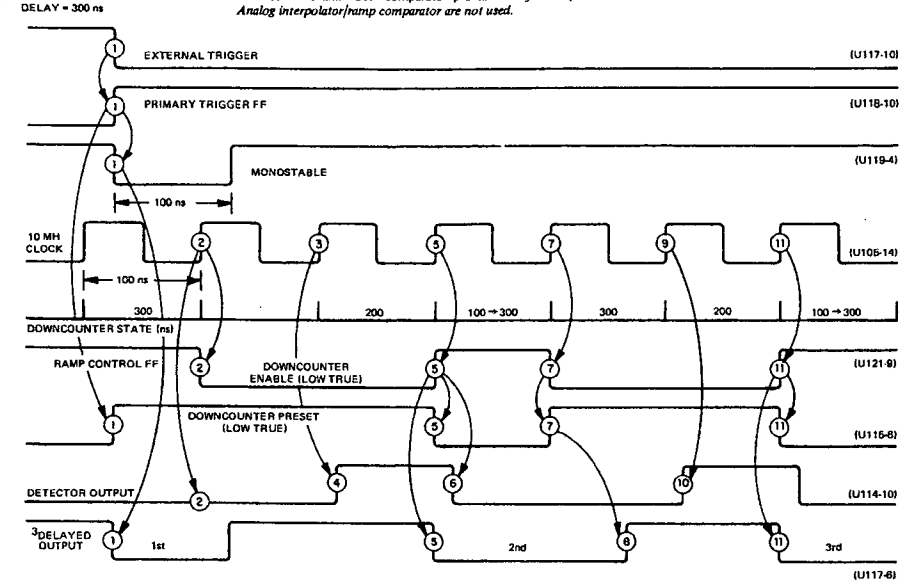
SEQUENCE OF EVENTS:

1. Primary trigger FF (U118B) is set.
   - Downcounter preset is released (U115-8). Downcounters were preset to specified delay prior to external trigger input.
   - Dump control FF (U121A) is reset. Dump mode is terminated.
   - C104 begins charging (through R113) towards +12 V.
   - $t_1 - t_2$ C104 charges towards +12 V.
2. Ramp control FF (U121B) is reset.
   - Downcounters are enabled.
   - Interpolator hold state is initiated.
3. Down counter state = 200 ns.
   - Detector output is forced high.
4. Ramp control FF (U121B) is set. Downcounter enable is false.
   - The interpolator ramp mode is initiated.
   - $t_4 - t_5$ C104 charges towards +12 V.
5. $t_1 - t_2 = 75$ ns $t_4 - t_3 = 200$ ns
   $t_2 - t_4 = 25$ ns $t_5 - t_1 = 300$ ns
   - When V ramp begins to exceed V compare, the comparator output is forced low (the "OR" comparator output was forced low when U121A was reset. However, the wired - or output (U123-9) remained high since the ramp comparator output (V compare) was high.
   - The comparator output (pulled down by Q103) sets U124A, Q103 switches +5 V to the successive approximation clock - transformer. U124 also forces the output of U117B low resulting in a delayed trigger out.

CASE IV[2]

NRDGS > 1
DELAY = 300 ns

Downcounters and "OR" comparator provides delayed output. Analog interpolator/ramp comparator are not used.



SEQUENCE OF EVENTS:

1. Primary trigger FF (U118B) is set. Initial trigger.
   - Monostable (U119A) fires for 100 ns.
   - The "OR" comparator output is forced low (the ramp comparator output was forced low when NRDGS > 1 inhibit (U115-6) was forced low. However, the wired - or output (U123-9) remained high since the "OR" comparator output was high - U121A set).
   - Downcounter preset is released (U115-8). Downcounters were preset to specified delay prior to external trigger input.
2. Ramp control FF (U121B) is reset. Downcounters are enabled (U106-4).
3. Downcounters count towards zero.
4. Downcounter state - 200 ns.
   - Detector output is forced high.
5. Ramp control FF (U121B) is set. Downcounter enable is false.
   - The "OR" comparator is forced low (2nd trigger).[3]
   - Downcounter preset is enabled. The counters are preset to the original delay.
6. Ramp control FF (U121B) input to the detector, forces the detector output low.
7. Ramp control FF (U121B) is reset.
   - Downcounters are enabled.
   - Downcounter preset line is released.
8. MPU clears the secondary trigger FF U124A (DS14).
9. Downcounters count towards zero.
10. Downcounter state = 200 ns.
    - Detector output is forced high.
11. Ramp control FF (U121B) is set. Downcounter enable is false.
    - The "OR" comparator output is forced low (3rd output).[3]
    - Downcounter preset is enabled. The counters are preset to the original delay.

— The process is repeated until the specified number of readings are performed. At this time, DS12 clears the primary trigger FF (U113B), inhibiting additional output.

Figure 4-31. Delay Logic Modes.

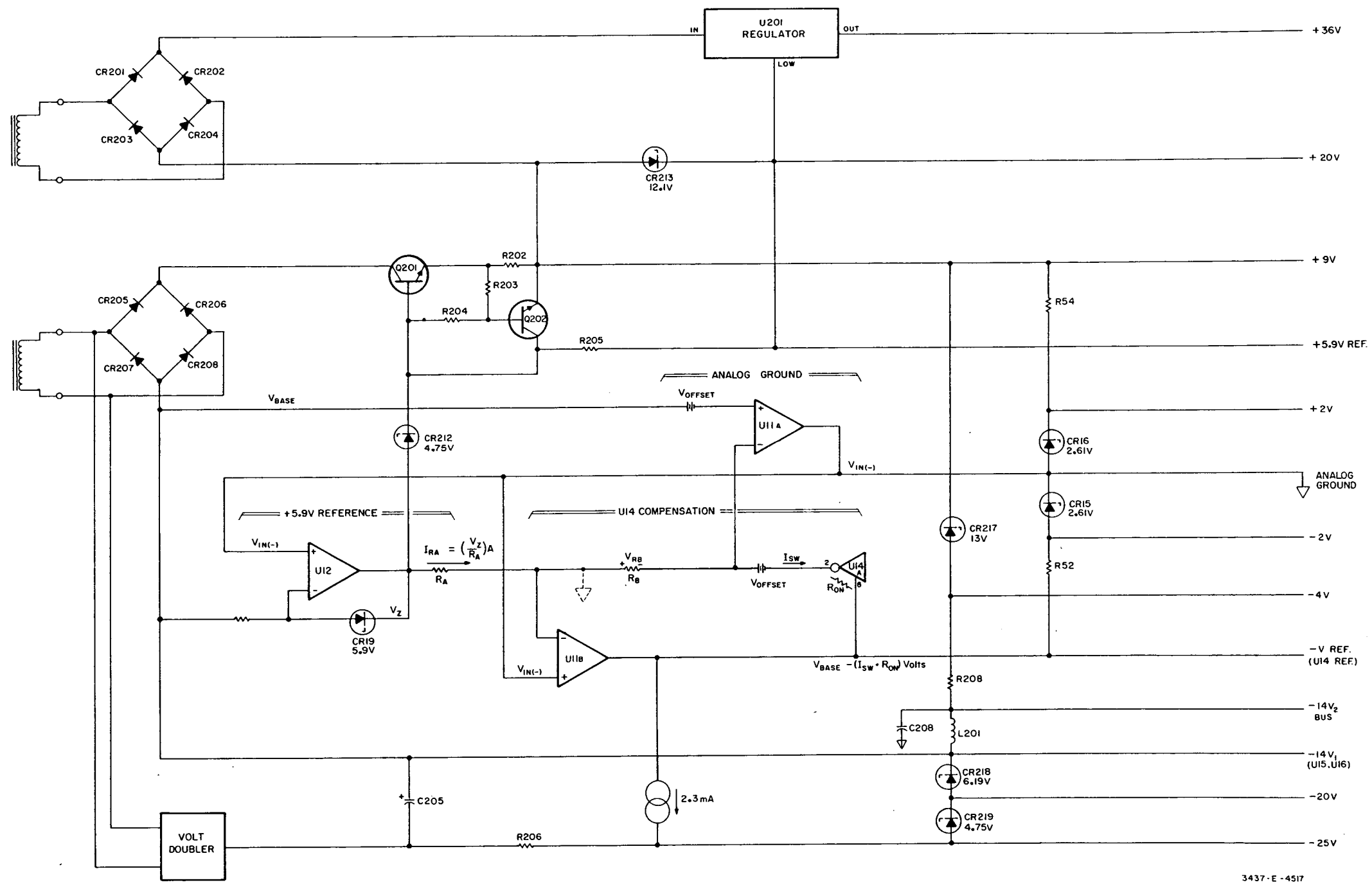


Figure 4-32. Inguard Power Supply Functional Block Diagram.

WARNING

These servicing instructions are for use by trained service personnel only. To avoid electrical shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains information necessary to maintain the 3437A within its specified performance limits. Included are performance tests, adjustment procedures, select component algorithms, and troubleshooting procedures.

5-3. Service-Guide Flowchart.

5-4. The service-guide flowchart (Figure 5-24) illustrates the sequence of events that should be performed whenever the 3437A requires service.

5-5. PERFORMANCE TESTS.

5-6. The performance tests verify the 3437A is performing within the specified limits indicated in Table 1-1 of this manual. A performance test card (located at the end of this section) is provided to record the results of the performance tests. If successful results are not obtained, refer to the service-guide flowchart.

NOTE

Read Section III (Operating and Programming) before starting Performance Tests.

5-7. Recommended Test Equipment.

5-8. The test equipment that is recommended to accomplish the performance tests, is listed in Table 5-1. If the recommended model is not available, use an instrument that has specifications equal to or better than those listed.

NOTE

The performance tests described in the following paragraphs can be performed in any order. However, the sequence described for each performance test must be followed since test results depend upon equipment configuration specified in previous steps.

5-9. Static Accuracy.

a. Connect the equipment as illustrated in Figure 5-1.

b. Program the 3437A keyboard as follows:

DELAY	0
NRDGS	1
RANGE	.1 V
TRIGGER	INT

Table 5-1. Required Test Equipment.

Instrument Type	Required Specifications	Recommended Model
Digital Voltmeter	± 20 V Range 5 Digit Resolution	-hp- Model 3490A
Thermal Converter	Bandwidth ⩾ 1.1 MHz	-hp- Model 11049C
Frequency Counter	Time Interval Measurements 2 ns Resolution	-hp- Model 5345A
Oscilloscope	Main Gate Output Z - Axis Input	-hp- 180A
Bus System Analyzer		-hp- 59401 Bus System Analyzer
Function Generator	Function: Sine/Sq Wave Output Power: ⩾15V p-p into 50 Ω Frequency: Up to 1.5 MHz	-hp- 3310A
High Resolution DC Source	± 15 Vdc: RMS-Noise Voltage Magnitude of ⩽ .2 Counts of the Range being calibrated.[1]	As illustrated in Figure 5-1
Logic Tracer[2]		-hp- 5004A
DSA Test ROM		-hp- 34115A
Power Supply	± 25 Vdc	-hp- 6218A
Performance Test Source Interface		-hp- 34114A
Performance Test Trigger Interface		-hp- 34113A
Triax Test Cable		-hp- 03437 - 61613

[1] Refer to Page 5-85 for noise measurement procedure.
[2] Contact your nearest -hp- Sales & Service Office for information concerning the -hp- 5004A Logic Tracer.

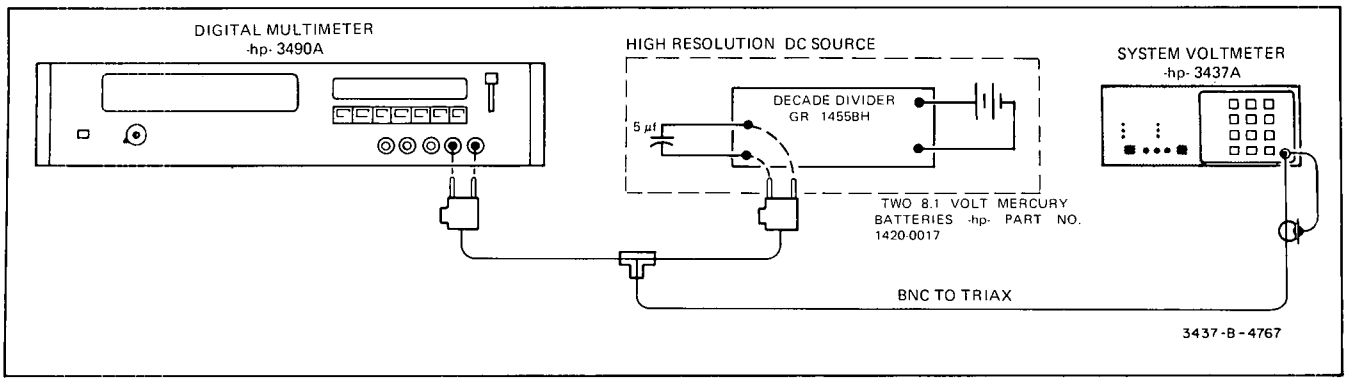


Figure 5-1. Static Accuracy Test Set-Up.

c. Set the 3490A controls as follows:

RANGE	Auto
FUNCTION	DC
SAMPLE/ HOLD	OFF

d. Adjust the dc source output to the values listed in Table 5-2 (3490A Display). Verify that the 3437A volts display indicates within the specified limits. (Program the 3437A to the 1 volt and 10 volt range where indicated.)

Table 5-2. Static Accuracy Test Limits.

Range	3490A Display	3437A Volts Display
.1 Volt	+ 0.04	.0398 to .0402
	- 0.04	- .0402 to - .03982
	- 0.08	- .0802 to - .0798
	+ 0.08	.0798 to .0802
	+ 0.12	.1198 to .1202
	- 0.12	- .1202 to - .1198
	- 0.16	.1598 to .1602
	+ 0.16	- .1602 to - .1598
1 Volt	+ 0.4	.398 to .402
	- 0.4	- .402 to - .398
	- 0.8	- .802 to - .798
	+ 0.8	.798 to .802
	+ 1.2	1.198 to 1.202
	- 1.2	- 1.202 to - 1.198
	- 1.6	- 1.602 to - 1.598
	+ 1.6	1.598 to 1.602
10 Volts	+ 4.0	3.98 to 4.02
	- 4.0	- 4.02 to - 3.98
	- 8.0	- 8.02 to - 7.98
	+ 8.0	7.98 to 8.02
	+ 12.0	11.98 to 12.02
	- 12.0	- 12.02 to - 11.98
	- 16.0	- 16.03 to - 15.97
	+ 16.0	15.97 to 16.03

5-10. Dynamic Accuracy.

5-11. 10 Volt Range.

a. Connect the equipment as illustrated in Figure 5-2.

b. Program the 3437A keyboard as follows:

DELAY	800 µs
NRDGS	1
TRIGGER	EXT
RANGE	10 V

c. Set the 3310A controls as follows:

RANGE	100
DIAL	10
DC OFFSET	OFF
FUNCTION	SQ
OUTPUT LEVEL	MINIMUM

d. Set the oscilloscope controls as follows:

VOLTS/DIV	5/DC
TIME/DIV	.1 ms
TRIGGER	EXTERNAL

e. Adjust the 3310A output level, oscilloscope trigger and intensity levels, to obtain a display as illustrated in Figure 5-3.

NOTE

Since the 3437A is using the main-gate output of the oscilloscope as an external trigger, the 3437A will not sample the waveform at the correct time if the oscilloscope is not properly triggered.

f. Adjust the output level (3310A) to obtain a 3437A volts display of 10.00 (± 5 counts).

g. Program the 3437A delay to 100 µs. Note the value of the 3437A volts display. (This is the final value of the input waveform, and will be used in determining the step response.)

h. Program the 3437A delay to 700 ns. Verify that the 3437A volts display indicates between ± 200 mV of the final value noted in Paragraph g. (The volts display can be held constant by pressing the 10 V key.)

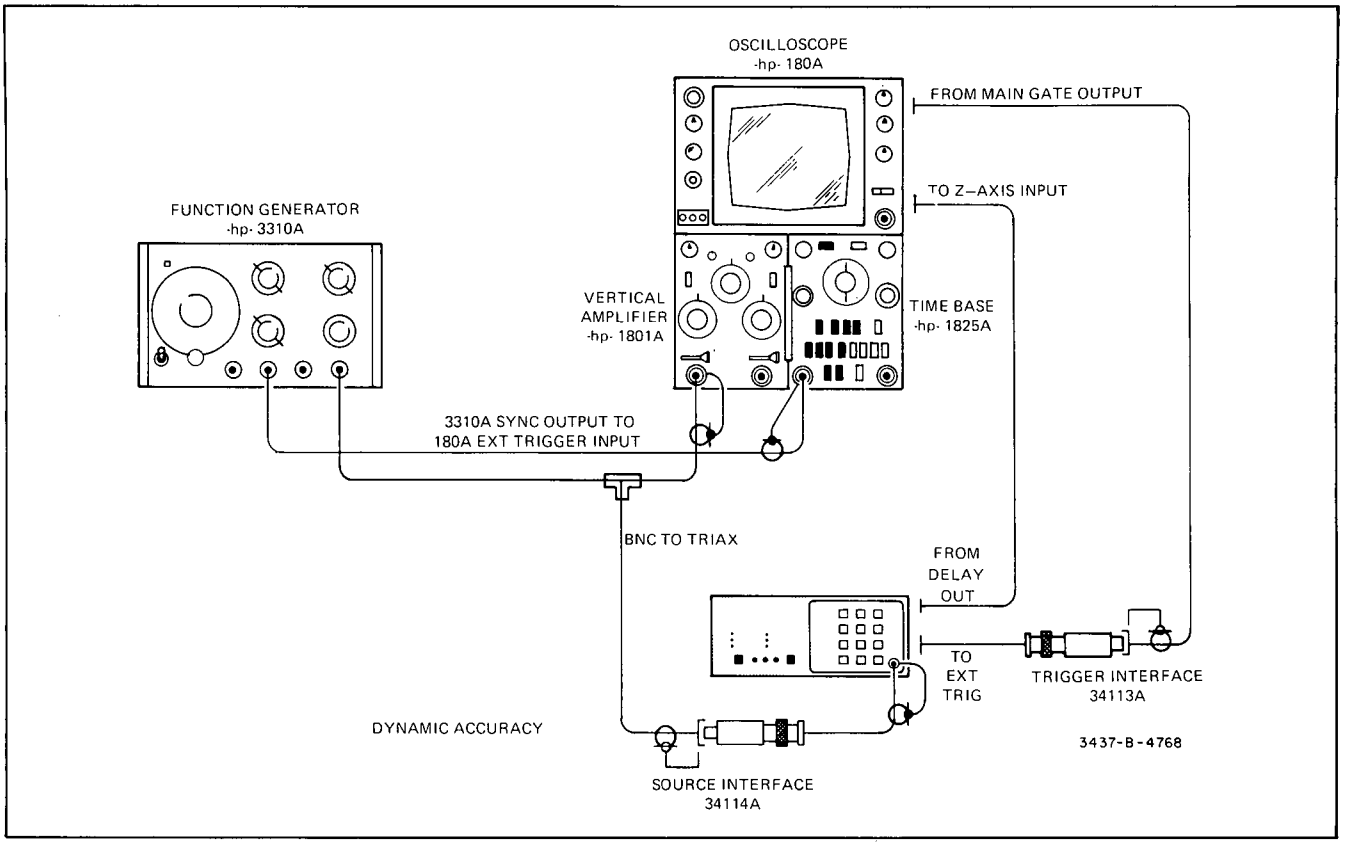


Figure 5-2. Dynamic Accuracy Test Set-Up.

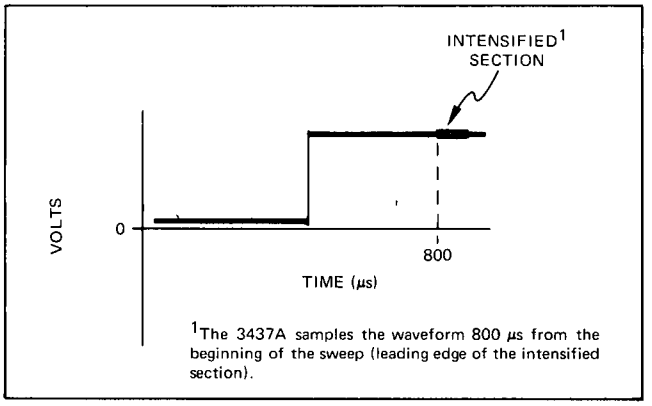


Figure 5-3. Intensified Waveform.

i. Program the 3437A delay to 7.5 μs. Verify the 3437A volts display indicates between ± 30 mV of the final value noted in Paragraph g.

j. Program the 3437A delay to 800 μs.

k. Adjust the output level (3310A) to obtain a 3437A volts display of approximately 01.00.

5-12. 1 Volt Range.

a. Program the 3437A Range to 1 V.

b. Set the oscilloscope Volts/Div to 1.

c. Adjust the 3310A output level, oscilloscope trigger and intensity levels, to obtain a waveform as illustrated in Figure 5-3.

d. Adjust the output level (3310A) to obtain a 3437A volts display of 1.000 (± 10 counts). The volts display can be held constant by pressing the 1.0 V key.

e. Program the 3437A delay to 100 μs. Note the value of the 3437A volts display. (This is the final value of the input waveform, and will be used in determining the step response.)

f. Program the 3437A delay to 700 ns. Verify that the 3437A volts display indicates between ± 20 mV of the final value noted in Paragraph e. (Repeat this procedure for a delay of 1.5 μs and a volts display of ± 3 mV.)

g. Program the 3437A delay to 800 μs.

h. Adjust the output level (3310A) to obtain a 3437A volts display of approximately 0.100.

5-13. .1 Volt Range.

a. Program the 3437A Range to .1 V.

b. Set the oscilloscope Volts/Div to .1.

c. Adjust the 3310A output level, oscilloscope trigger and intensity levels, to obtain a waveform as illustrated in Figure 5-3.

d. Adjust the output level (3310A) to obtain a 3437A volts display of .1000 (± 10 counts). The volts display can be held constant by pressing the .1 V key.

e. Program the 3437A delay to 400 μs. Note the value of the 3437A volts display. (This is the final value of the input waveform, and will be used in determining the step response.)

f. Program the 3437A delay to 25 μs. Verify that the 3437A volts display indicates between ± 200 μV of the final value noted in Paragraph e.

5-15. Bandwidth.

5-16. .1 Volt Range.

a. Connect the equipment as illustrated in Figure 5-4.

b. Program the 3437A keyboard as follows:

DELAY	0
NRDGS	1
TRIGGER	EXT
RANGE	.1 V

c. Set the 3310A controls as follows:

RANGE	100
DIAL	10
DC OFFSET	0
FUNCTION	SINE
OUTPUT LEVEL	MINIMUM

d. Set the oscilloscope controls as follows:

VOLTS/DIV	.1/DC
TIME/DIV	200 μs
TRIGGER	EXTERNAL

e. Set the 3490A controls as follows:

RANGE	AUTO
FUNCTION	DC
SAMPLE/HOLD	OFF

f. Adjust the oscilloscope trigger level so that the oscilloscope is triggered when the input waveform is at its most positive value. Adjust the intensity level to obtain a display as illustrated in Figure 5-5.

NOTE

Since the 3437A is using the main-gate output of the oscilloscope as an internal trigger, the 3437A will not sample the waveform at the correct time if the oscilloscope is not properly triggered.

g. Adjust the output level (3310A) to obtain a 3437A volts display of approximately.1500. The volts display can be held constant by pressing the .1 V key. (Note the volts display as V_A.)

h. Set the 3310A output frequency to 40 kHz (monitor the 3310A output level with the 3490A to assure it remains constant).

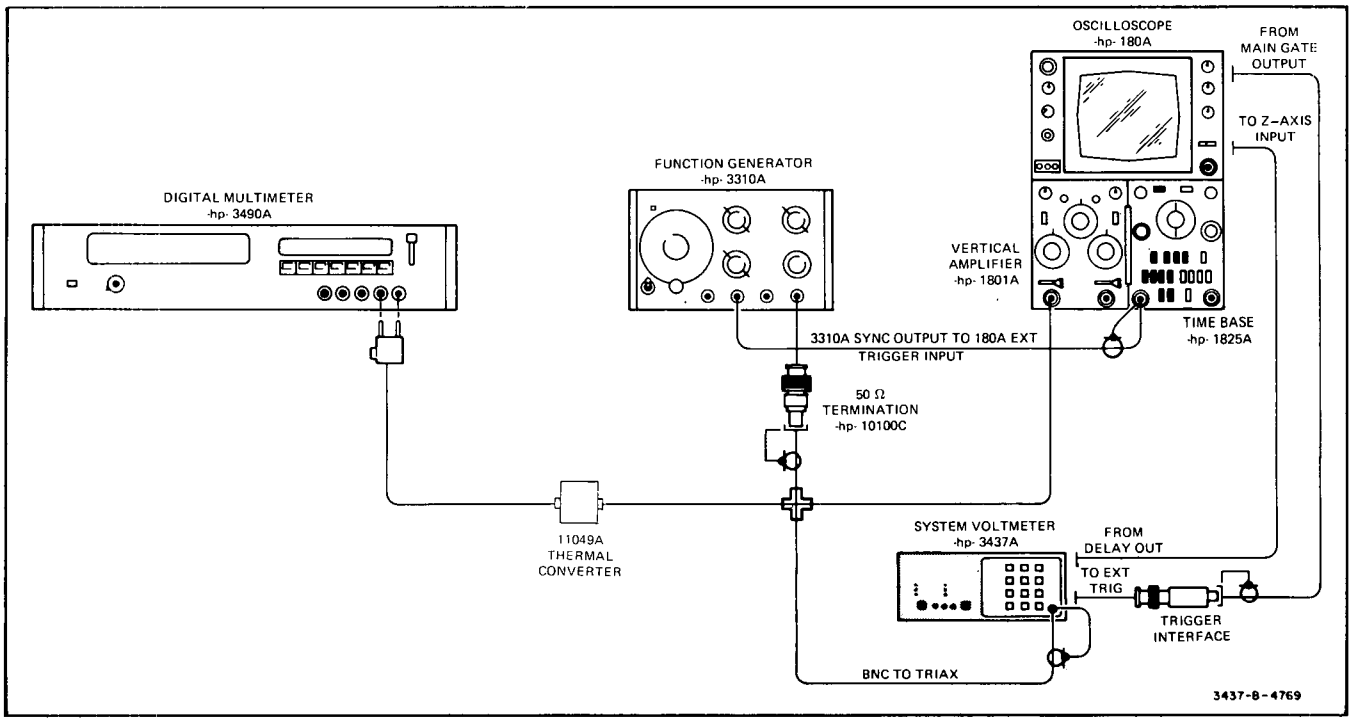


Figure 5-4. Bandwidth Test Set-Up.

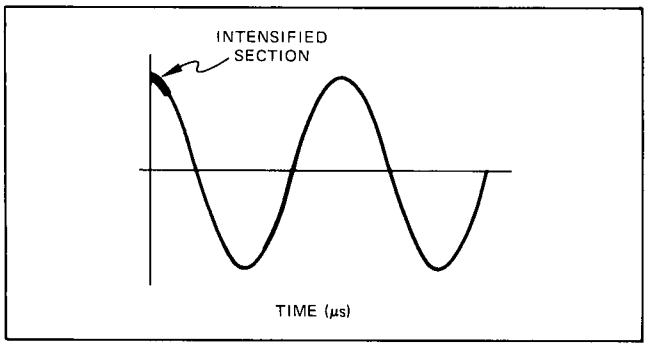


Figure 5-5. Reference Waveform.

i. Remove the cable connected to the oscilloscope EXT INPUT and set the Time/Div switch to 50 ms.

j. Verify that the maximum indication observed on the 3437A volts display is $\geqslant 1/\sqrt{2}$ VA.

NOTE

Since the 3437A external trigger and input waveforms are not synchronous, several samples need to be observed to verify a maximum indication.

5-17. 1 Volt Range.

a. Program the 3437A RANGE to 1 volt.

b. Set the 3310A as follows:

RANGE	100
DIAL	10
OUTPUT LEVEL	MINIMUM

c. Set the oscilloscope as follows:

VOLTS/DIV	1
TIME/DIV	200 μs

(Reconnect the oscilloscope EXT INPUT cable.)

d. Adjust the oscilloscope trigger level so that the oscilloscope is triggered when the input waveform is at its most positive value. Adjust the intensity level to obtain a display as illustrated in Figure 5-5.

e. Set the oscilloscope Volts/Div to 1 and adjust the output level (3310A) to obtain a 3437A volts display of approximately 1.500. The volts display can be held constant by pressing the 1.0 V key. (Note the volts display as V_B.)

f. Set the 3310A output frequency to 1.1 MHz. (Monitor the 3310A output level with the 3490A to assure it remains constant.)

g. Remove the cable connected to the oscilloscope EXT INPUT and set the Time/Div switch to 50 ms.

h. Verify that the maximum indication observed on the 3437A volts display is $\geqslant 1/\sqrt{2}\, V_B$.

NOTE

Since the 3437A external trigger and input waveforms are not synchronous, several samples need to be observed to verify a maximum indication.

5-18. 10 Volt Range.

a. Program the 3437A Range to 10 volts.

b. Set the 3310A as follows:

RANGE	100
DIAL	10
OUTPUT LEVEL	MINIMUM

c. Set the oscilloscope as follows:

VOLTS/DIV	.1
TIME/DIV	200 μs

(Reconnect the oscilloscope EXT INPUT cable.)

d. Adjust the oscilloscope trigger level so that the oscilloscope is triggered when the input waveform is at its most positive value. Adjust the intensity level to obtain a display as illustrated in Figure 5-5.

e. Set the oscilloscope Volts/Div to 1 and adjust the output level (3310A) to obtain a 3437A volts display of approximately 2.50. The volts display can be held constant by pressing the 10 V key. (Note the volts display as V_C.)

f. Set the 3310A output frequency to 1.0 MHz. (Monitor the 3310A output level with the 3490A to assure it remains constant.)

g. Remove the cable connected to the oscilloscope EXT INPUT and set the Time/Div switch to 50 ms.

h. Verify that the maximum indication observed on the 3437A volts display is $\geqslant 1/\sqrt{2}\, V_C$.

NOTE

Since the 3437A external trigger and input waveforms are not synchronous, several samples need to be observed to verify a maximum indication.

5-19. Delay Accuracy/Jitter.

a. Connect the equipment as illustrated in Figure 5-6.

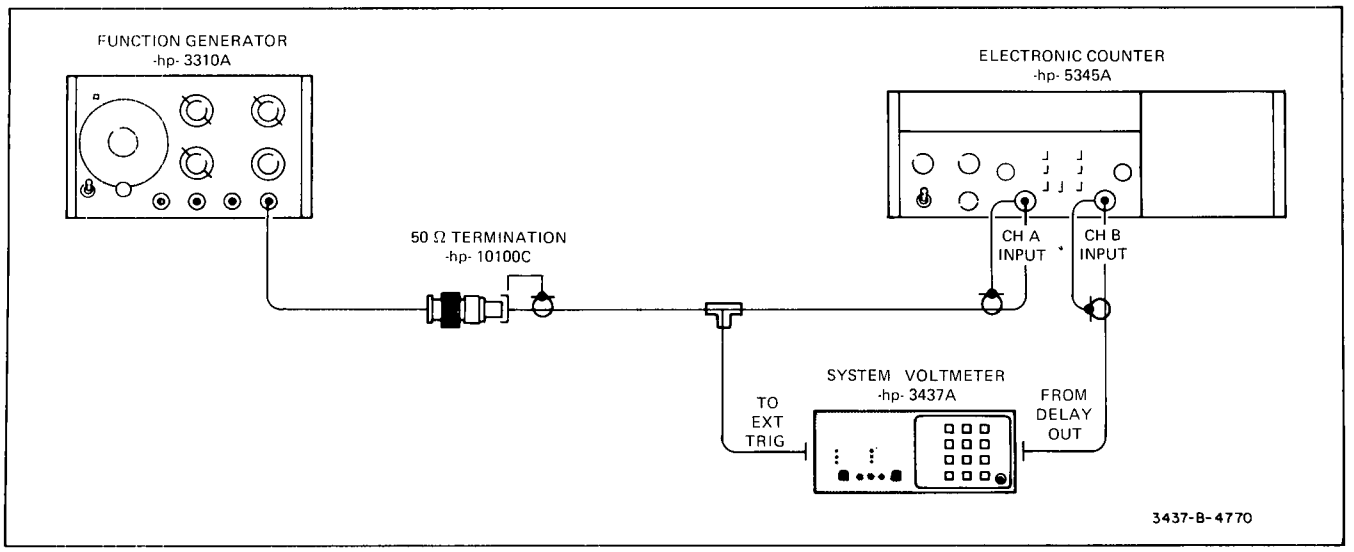


Figure 5-6. Delay Accuracy/Jitter Test Set-Up.

b. Program the 3437A keyboard as follows:

DELAY	0
NRDGS	1
TRIGGER	EXTERNAL

c. Set the 3310A as follows:

RANGE	0.1
FREQUENCY DIAL	10
DC OFFSET	0
FUNCTION	SQ
OUTPUT LEVEL	MINIMUM

d. Set the 5345A as follows:

FUNCTION	TIME INT A TO B
GATE TIME	MIN
DISPLAY POSITION	AUTO
CHANNEL A	
LEVEL	PRESET
SLOPE	–
ATTEN	1 MΩ/x 1
AC/DC	DC
CHANNEL B	SAME AS CHANNEL A
CHECK/COM A/ SEP	SEP

e. Adjust the output level (3310A) until the 3437A becomes externally triggered (sampling LED begins to blink).

f. Referring to Table 5-3, verify that the frequency counter display is within the specified limits for 0 delay. Also verify that the jitter (Δ Display) is within the specified limits.

g. Program the 3437A delay to the values indicated in Table 5-3, verifying that the delay and jitter are within the specified limits.

Table 5-3. Delay Accuracy/Jitter.

Delay	Accuracy	Jitter
0	75 ns to 125 ns	≤2 ns
100 ns	175 ns to 225 ns	≤2 ns
500 ns	575 ns to 625 ns	≤10 ns
1 μs	1.075 μs to 1.1250 μs	≤10 ns
500 μs	499.960 μs to 500.1650 μs	≤11 ns
1 ms	.999920 ms to 1.0002050 ms	≤12 ns
500 ms	499.960 ms to 500.040125 ms	≤110 ns
.9999999 sec	.999919990 sec to 1.000080030 sec	≤110 ns

5-20. Number of Readings.

a. Connect the equipment as illustrated in Figure 5-7.

b. Program the 3437A keyboard as follows:

DELAY	0
NRDGS	10
TRIGGER	HOLD/MANUAL

c. Set the 5345A controls as follows:

FUNCTION	START
GATE TIME	MIN
DISPLAY POSITION	AUTO
CHANNEL A	
LEVEL	PRESET
SLOPE	–
ATTEN	1 MΩ/x 20
AC/DC	DC
CHECK/COM A/ SEP	SEP

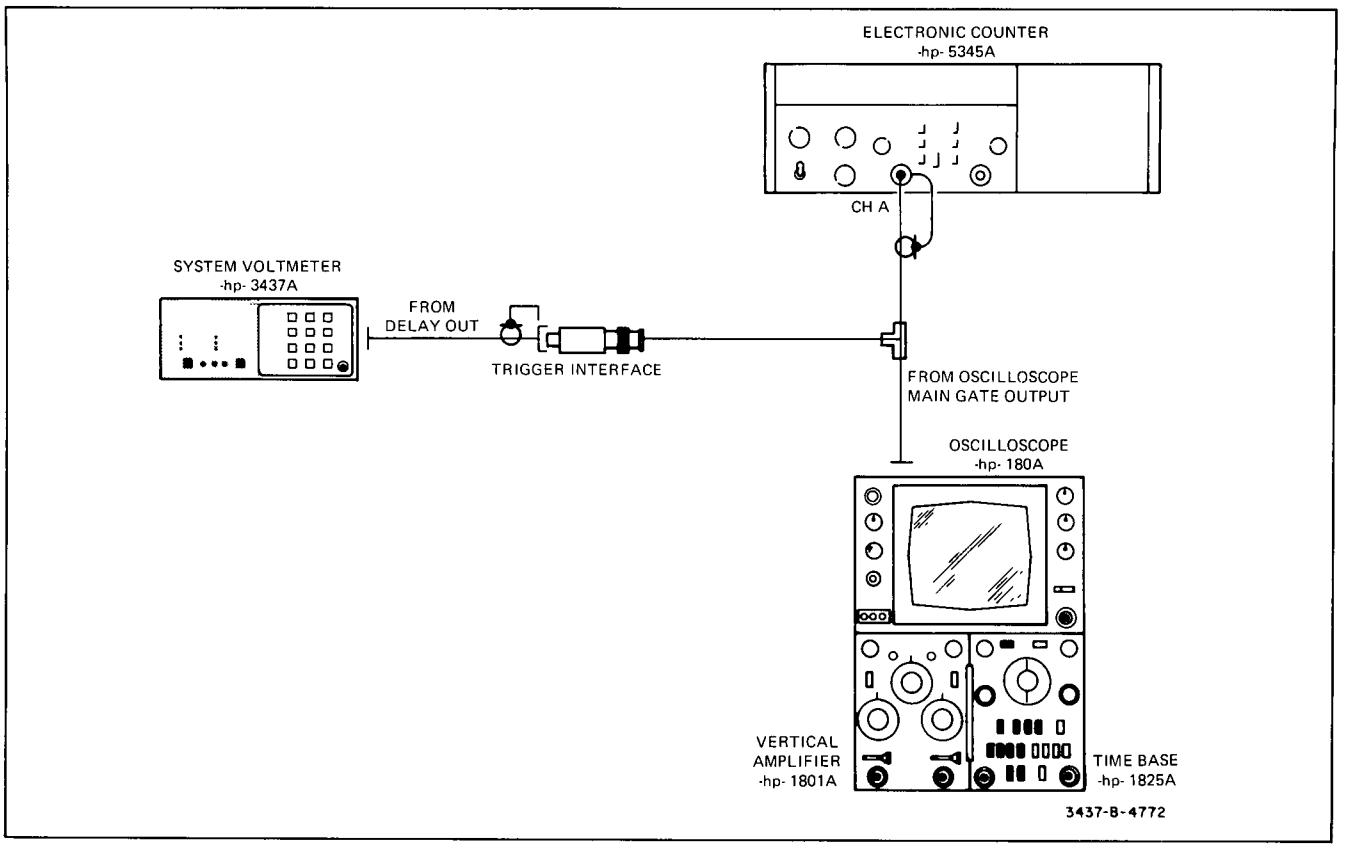


Figure 5-7. NRDGS Test Set-Up.

d. Set the oscilloscope to single sweep.

e. Reset the 5345A. (Gate the 5345A by pressing the oscilloscope reset key.)

f. Press the 3437A Hold/Man key (initiates 10 readings). Verify that the 5345A display indicates 10.

g. Program NRDGS (3437A) to the values listed in Table 5-4. Using the procedure described, (Steps e - f) verify that the 5345A indicates the number of readings programmed.

Table 5-4. NRDGS Test Values.

NRDGS	5345A Display
10	10
50	50
100	100
500	500
1000	1000
5000	5000
9999	9999

5-21. Common Mode Rejection Ratio (CMRR).

a. Connect the equipment as illustrated in Figure 5-8. (Remove the line cord from the 3437A.)

b. Set the oscilloscope controls as follows:

CH A Volts/Div	5
CH B Volts/Div	.1
Int/Ext	Int
Auto/Norm	Auto

c. Verify that with the 10 V p-p calibrator output applied between the 3437A chassis and LO input (through C_X) that there is $\leqslant$ 450 mV p-p across C_X (CH B input).

NOTE

A CMRR of $\geqslant$ 75 dB is achieved by maintaining a Lo to chassis capacitance of $\leqslant$ 471 pF. The CMRR test measures this capacitance.

5-22. Overload Display.

a. Connect the equipment as illustrated in Figure 5-9.

b. Set the power supply output to minimum.

c. Program the 3437A keyboard as follows:

DELAY	.250 SEC
NRDGS	1
RANGE	.1 V
TRIGGER	INT

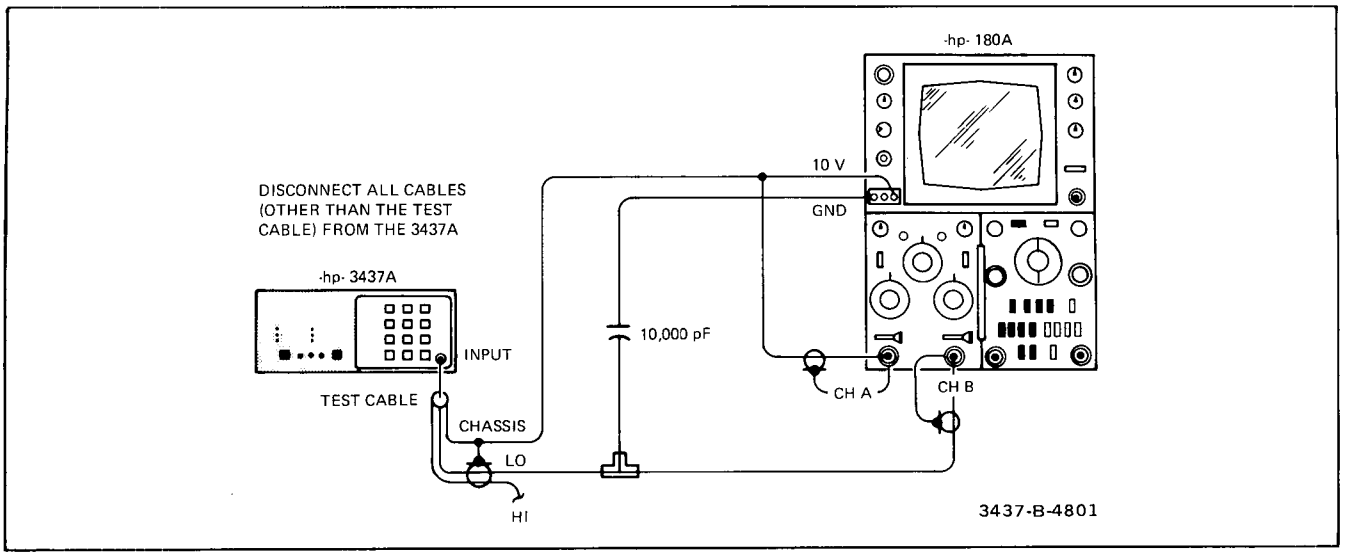


Figure 5-8. CMRR Test Set-Up.

d. Set the 3490A controls as follows:

RANGE	AUTO
FUNCTION	DC
SAMPLE/ HOLD	OFF

e. Adjust the power supply output for a 3490A volts display of 0.20. Verify that the 3437A volts display indicates .9999.

f. Program the 3437A Range to 1 V.

g. Adjust the power supply output for a 3490A volts display of 2.0. Verify that the 3437A volts display indicates 9.999.

h. Program the 3437A Range to 10 volts.

i. Adjust the power supply output for a 3490A volts display of 20.00. Verify that the 3437A volts display indicates 99.99.

5-23. HP-IB INTERFACE.

5-24. The Bus Analyzer (-hp- 59401A) is used as the 3437A controller during the HP-IB performance tests. Whenever the 59401A is required to send either MLA (My Listen Address) or MTA (My Talk Address) refer to Table 5-5 for DIO 1-8 switch settings.

NOTE

Set HP-IB address switch positions 1-8 to zero.

5-25. Connect the equipment as illustrated in Figure 5-10.

Table 5-5. MLA and MTA DIO 1-8 Switch Settings.

	DIO								
Message	8	7	6	5	4	3	2	1	ATN
MLA	X	0	1	0	0	0	0	0	1
MTA	X	1	0	0	0	0	0	0	1

NOTE

To clear an invalid program condition: (Re-address the 3437A to listen.)

Set DIO 1-8 to "MLA"
Set ATN to 1, REN to ON
Press EXECUTE

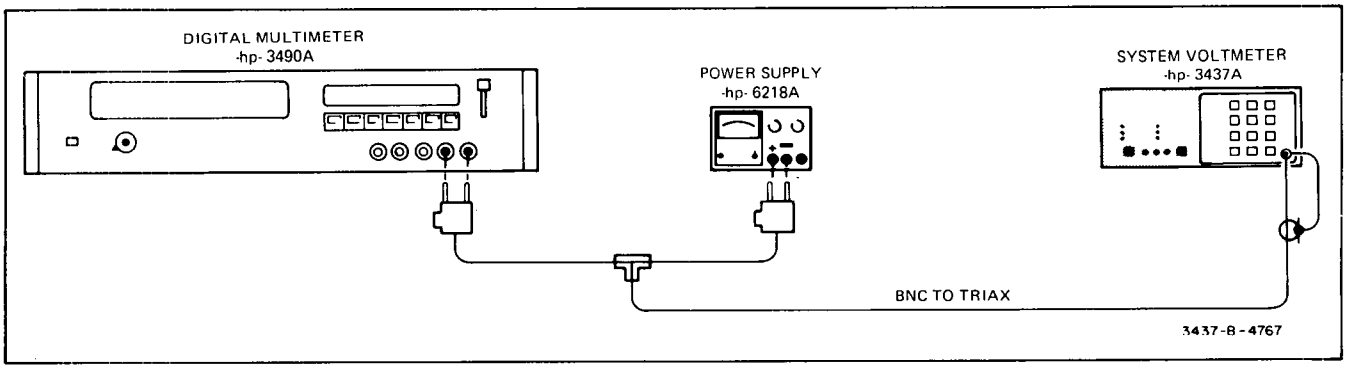


Figure 5-9. Overload Display Test Set-Up.

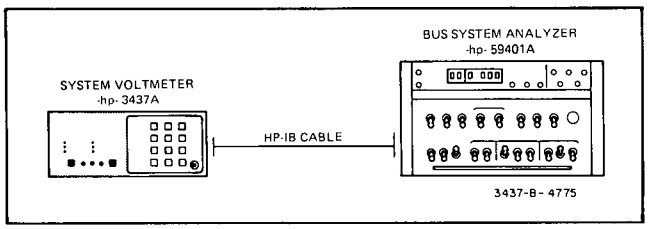


Figure 5-10. Program and Message Code Test Set-Up.

5-26. Program Code Verification.

a. Program the 3437A keyboard as follows:

DELAY	.9999999 sec
NRDGS	9999
ENAB RQS	7
RANGE	1 V
TRIGGER	EXT
FORMAT	PACKED

b. Set the 59401A controls as follows:

REN	ON
CLEAR	OFF
COMP	OFF
TALK/LISTEN	TALK
FAST/SLOW/ HALT	HALT
SRQ	0
EOI	0
DIO 1-8	"MLA"

c. Using the 59401A, verify program code operation by performing the steps indicated in the following paragraphs.

5-27. Delay (D).

a. Press EXECUTE (3437A - Listen/Remote).

b. Set ATN to 0.

c. Set DIO 1-8 to "D" (104_8), Press EXECUTE.

d. Set DIO 1-8 to "dp" (056_8), Press EXECUTE.

e. Set DIO 1-8 to "S" (123_8), Press EXECUTE.

f. Verify that the numeric entry display indicates SEC DELAY = 0.

5-28. NRDGS (N).

a. Set DIO 1-8 to "N" (116_8), Press EXECUTE.

b. Set DIO 1-8 to "Ø" (060_8), Press EXECUTE.

c. Set DIO 1-8 to "S" (123_8), Press EXECUTE.

d. Verify that the numeric entry display indicate NUM READINGS = 0.

5-29. ENAB RQS (E).

a. Set DIO 1-8 to "E" (105_8), Press EXECUTE.

b. Set DIO 1-8 to "Ø" (060_8), Press EXECUTE.

c. Set DIO 1-8 to "S" (123_8), Press EXECUTE.

d. Verify that the numeric entry display indicates ENAB RQS = 0.

5-30. Range (R 1, 2, 3).

a. Set DIO 1-8 to "R" (122_8), Press EXECUTE.

b. Set DIO 1-8 to "1" (061_8), Press EXECUTE.

c. Verify that the 0.1 V annunciator is illuminated.

d. Set DIO 1-8 to "R" (122_8), Press EXECUTE.

e. Set Dio 1-8 to "2" (062_8), Press EXECUTE.

f. Verify that the 1.0 V annunciator is illuminated.

g. Set DIO 1-8 to "R" (122_8), Press EXECUTE.

h. Set DIO 1-8 to "3" (063_8), Press EXECUTE.

i. Verify that the 10 V annunciator is illuminated.

5-31. Trigger (T1, 2, 3).

a. Set DIO 1-8 to "T" (124_8), Press EXECUTE.

b. Set DIO 1-8 to "1" (061_8), Press EXECUTE.

c. Verify that the INT annunciator is illuminated.

d. Set DIO 1-8 to "T" (124_8), Press EXECUTE.

e. Set DIO 1-8 to "2" (062_8), Press EXECUTE.

f. Verify that the EXT annunciator is illuminated.

g. Set DIO 1-8 to "T" (124_8), Press EXECUTE.

h. Set DIO 1-8 to "3" (063_8), Press EXECUTE.

i. Verify that the HOLD/MAN annunciator is illuminated).

5-32. Format (F 1, 2).

a. Set DIO 1-8 to "F" (106_8), Press EXECUTE.

b. Set DIO 1-8 to "1" (061_8), Press EXECUTE.

c. Verify that the ASCII annunciator is illuminated.

d. Set DIO 1-8 to "F" (106_8), Press EXECUTE.

e. Set DIO 1-8 to "2" (062_8), Press EXECUTE.

f. Verify that the PACKED annunciator is illuminated

5-33. Message Code Verification.

a. Press LOCAL key. Program the 3437A keyboard as follows:

DELAY	.9999999 sec
NRDGS	9999
ENAB RQS	7
RANGE	1 V
TRIGGER	EXT
FORMAT	PACKED

b. Set the 59401A controls as follows:

REN	ON
CLEAR	OFF
COMP	OFF
TALK/LISTEN	TALK
FAST/SLOW/ HALT	HALT
SRQ	0
EOI	0
DIO 1-8	"MLA"

c. Using the 59401A, verify message code operation by performing the steps indicated in the following paragraphs.

5-34. My Listen Address (MLA).

a. Press EXECUTE.

b. Verify that the Listen/Remote annunciators are illuminated.

5-35. My Talk Address (MTA).

a. Set DIO 1-8 to "MTA", Press EXECUTE.

b. Verify that the Talk/Remote annunciators are illuminated.

5-36. Device Clear (DCL).

a. Set DIO 1-8 to "MLA", Press EXECUTE.

b. Set DIO 1-8 to "DCL" (024_8). Press EXECUTE.

c. Press LOCAL key. Verify that the 3437A is configured to its turn-on state. Refer to Table 3-5.

5-37. Selected Device Clear (SDC).

a. Program the 3437A keyboard as follows:

DELAY	.9999999 sec
NRDGS	9999
ENAB RQS	7
RANGE	1 V
TRIGGER	EXT
FORMAT	PACKED

b. Set DIO 1-8 to "MLA".

c. Press EXECUTE (3437A - Listen/Remote).

d. Set DIO 1-8 to "SDC" (004_8), Press EXECUTE.

e. Press LOCAL key. Verify that the 3437A is configured to its turn-on state. Refer to Table 3-5.

5-38. Group Execute Trigger (GET).

a. Set DIO 1-8 to "MLA", Press EXECUTE.

b. Set ATN to 0.

c. Set DIO 1-8 to "T" (124_8), Press EXECUTE.

d. Set DIO 1-8 to "2" (062_8).

e. Press EXECUTE (data ready annunciator should not be illuminated).

f. Set DIO 1-8 to "GET" (010_8).

g. Set ATN to 1, Press EXECUTE.

h. Verify that the DATA READY annunciator is illuminated - indicating that the 3437A has been triggered, and has sampled the input voltage.

5-39. Go To Local (GTL).

a. Set DIO 1-8 to "GTL" (001_8), Press EXECUTE.

b. Verify that the REMOTE annunciator is not illuminated, and that the 3437A can be controlled from the keyboard.

5-40. Local Lock-Out (LLO).

a. Set DIO 1-8 to "MLA".

b. Press EXECUTE (3437A - Listen/Remote).

c. Set DIO 1-8 to "LLO" (021_8), Press EXECUTE.

d. Verify that the 3437A cannot be controlled from the keyboard even though the LOCAL key is pressed.

5-41. Unlisten (UNL).

a. Set REN to OFF (clears LLO).

b. Set DIO1–8 to "MLA", Press EXECUTE.

c. Set DIO 1-8 to "UNL" (077_8), Press EXECUTE.

d. Verify that the LISTEN annunciator is not illuminated.

5-42. Untalk (UNT).

a. Set DIO 1-8 to "MTA".

b. Press EXECUTE (3437A - Talk).

c. Set DIO 1-8 to "UNT" (137_8), Press EXECUTE.

d. Verify that the TALK annunciator is not illuminated.

5-43. Interface Clear (IFC).

a. Set DIO 1-8 to "MLA".

b. Press EXECUTE (3437A - Listen/Remote).

c. Set IFC True. (Press IFC switch.)

d. Verify that the LISTEN annunciator is not illuminated.

5-44. Reading Rate.

NOTE

The following adjustment procedure requires that the top cover be removed. Be extremely careful since lethal voltages are exposed. Be especially careful around the line filter and fuse holder located in the top left rear corner.

5-45. Preliminary.

a. Remove the HP-IB cable from the 3437A.

NOTE

An open HP-IB connector simulates an infinitely fast listener.

b. Set the HP-IB address select switch to TALK only as follows:

1. With the power cord removed from the instrument remove the top cover (fastener located at rear of top cover).
2. Remove the 3 screws that fasten the left side of the logic board to the chassis (the screws are located opposite the logic board hinges).
3. Set the instrument on its right side, and lower the logic board to a horizontal position.
4. Set switch position 6 (HP-IB address switch) to open.
5. Replace the 3 screws that fasten the logic board to the chassis (HP-IB cable tucked between the power transformer and rear panel).
6. Replace the top cover and reconnect the power cord.

5-46. ASCII.

a. Program the 3437A keyboard as follows:

DELAY	277.8 μs
NRDGS	9999
TRIGGER	HOLD/MAN
FORMAT	ASCII

b. Press the HOLD/MAN key.

1. Initiates a burst of readings (9999) at a rate of 3600 readings/second.

c. Verify that the IGNOR TRIG annunciator is NOT illuminated.

d. Program the 3437A delay to 250 μs.

e. Press the HOLD/MAN key.

1. Initiates a burst of readings (9999) at a rate of 4000 readings/second.

f. Verify that the IGNOR TRIG annunciator is illuminated.

5-47. Packed.

a. Program the 3437A keyboard as follows:

DELAY	175.4 μs
NRDGS	9999
TRIGGER	HOLD/MAN
FORMAT	PACKED

b. Press the HOLD/MAN key.

1. Initiates a burst of readings (9999) at a rate of 5700 readings/second.

c. Verify that the IGNOR TRIG annunciator NOT illuminated.

d. Program the 3437A delay to 150 μs.

e. Press the HOLD/MAN key.

1. Initiates a burst of readings (9999) at a rate of 6666 Readings/Second.

f. Verify that the IGNOR TRIG annunciator is illuminated.

5-48. Turn the 3437A OFF and set the HP-IB address switch to its original position. (Refer to Paragraph 5-45).

5-49. Data Format.

5-50. Preliminary.

a. Connect the equipment as illustrated in Figure 5-11.

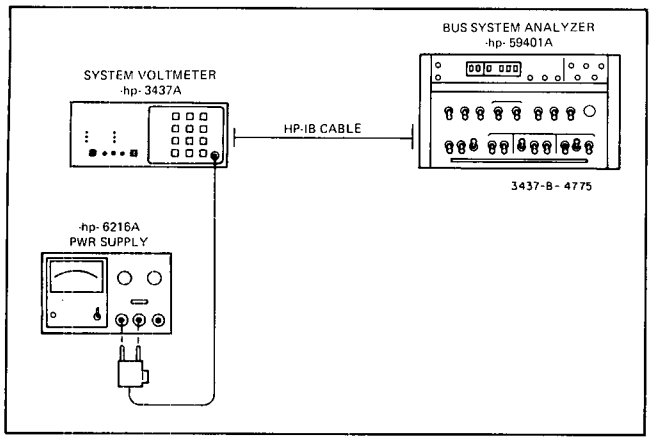


Figure 5-11. Data Format Test Set-Up.

b. Program the 3437A keyboard as follows: (Press LOCAL key to obtain keyboard control.)

DELAY	.25 sec
NRDGS	1
RANGE	1 V
TRIGGER	INT
FORMAT	ASCII

c. Set the 59401A controls as follows:

REN	ON
CLEAR	OFF
COMP	OFF
TALK/LISTEN	TALK
FAST/SLOW/ HALT	HALT
SRQ	0
EOI	0
DIO 1-8	"MLA"

d. Adjust the output of the dc source (set to X1) for a 3437A volts display of 1.532.

e. Using the 59401A, program the 3437A to Talk/Remote and the 59401A to listen as follows:

Press EXECUTE (3437A - Listen/Remote)
Set DIO 1-8 to "MTA"
Press EXECUTE (3437A - Talk/Remote)
Set Talk/Listen to listen.

5-51. ASCII.

a. The 3437A is addressed to talk and will handshake a ASCII data byte (with the 59401A) each time the 59401A EXECUTE key is pressed. (The 1st byte was accepted by the 59401A when Talk/Listen was set to listen.)

b. Using Table 5-6 and the procedure described in Step a, verify the ASCII data format (59401A display).

Table 5-6. ASCII Data Format.

Byte	ASCII Character	Octal Code
1	+	053
2	1	061
3		056
4	5	065
5	3	063
6	2	062
7	CR	015
8	LF & EOI	012 & EOI

5-52. Packed.

a. Using the 59401A, program the 3437A to Packed format, Talk/Remote and the 59401A to listen as follows:

1. Set Talk/Listen to Talk.
2. Set DIO 1-8 to "MLA", Press EXECUTE.
3. Set ATN to 0.
4. Set DIO 1-8 to "F" (106_8), Press EXECUTE.
5. Set DIO 1-8 to "2" (062_8).
6. Press EXECUTE (3437A - Packed Format).
7. Set DIO 1-8 to "MTA", Press EXECUTE.
8. Set Talk/Listen to Listen. (The 3437A is triggered and samples the input voltage. The volts display should indicate + 1.532.)

b. The 3437A is addressed to talk and will handshake a packed data byte (with the 59401A) each time the 59401A EXECUTE key is pressed. (The 1st byte was accepted by the 59401A when Talk/Listen was set to Listen.)

c. Using Table 5-7 and the procedure described in Step b, verify the Packed data format (59401A Display).

Table 5-7. Packed Data Format.

Byte	Octal Code
1	365
2	062 & EOI

5-53. Service Request Status Byte.

a. Connect the equipment as illustrated in Figure 5-10.

b. Program the 3437A keyboard as follows: (Press LOCAL key to obtain keyboard control.)

DELAY	0
NRDGS	1
ENAB RQS	4 (SRQ true when data ready)
TRIGGER	INT

c. Set the 59401A controls as follows:

REN	ON
CLEAR	OFF
COMP	OFF
TALK/LISTEN	TALK
FAST/SLOW/ HALT	HALT
SRQ	0
ATN	1
DIO 1-8	"SPE" (030_8)

d. Using the 59401A initiate a serial poll, address the 3437A to Talk, and handshake the SRQ status byte from the 3437A as follows:

1. Press EXECUTE (initiates a serial poll).
2. Set Talk/Listen to Listen (54901A reads SRQ status byte).

e. Verify that the 59401A display indicates 164.

5-54. Binary Program.

5-55. Preliminary (Cycle 3437A Power).

a. Connect the equipment as illustrated in Figure 5-10.

b. Program the 3437A keyboard as follows: (Press LOCAL key to obtain keyboard control.)

DELAY	500 μs
NRDGS	1976
ENAB RQS	4
RANGE	1 V
TRIGGER	INT
FORMAT	ASCII

c. Set the 59401A controls as follows:

REN	ON
CLEAR	OFF
COMP	OFF
TALK/LISTEN	TALK
FAST/SLOW/ HALT	HALT
SRQ	0
EOI	0
DIO 1-8	"MLA"

d. Using the 59401A, program the 3437A to the Binary Program mode, address the 3437A to LISTEN and the 59401A to TALK as follows:

1. Press EXECUTE (3437A - Listen/Remote).
2. Set DIO 1-8 to "B" (102_8), ATN to 0.
3. Press EXECUTE (BINARY PRGM annunciator should be illuminated).
4. Set DIO 1-8 to "MTA", press EXECUTE.
5. Set Talk/Listen to Listen.

5-56. Learn.

a. The 3437A will handshake (onto the HP-IB) a Binary Program data byte each time the 59401A EXECUTE key is pressed. (The 1st byte was input to the 59401A when Talk/Listen was set to Listen.) Using Table 5-8, verify the Binary Program byte sequence. The octal code is displayed by the 59401A. (The 3437A will terminate the Binary Program mode after the 7th byte is written onto the HP-IB.)

Table 5-8. Binary Program Byte Sequence.

Byte	Octal Code
1	307
2	031
3	166
4	X00[1]
5	000
6	120
7	000 & EOI

[1] (X = don't care)

5-57. Program.

a. Set the 59401A controls as follows:

TALK/LISTEN	TALK
DIO 1-8	"MLA"

b. Using the 59401A, program the 3437A to the Binary Program mode.

1. Press EXECUTE (3437A - Listen/Remote).
2. Set DIO 1-8 to "B" (102_8), ATN to 0.
3. Press EXECUTE (Binary Prgm annunciator should be illuminated).

5-58. The 3437A will read (from the 59401A) a data byte each time the 59401A EXECUTE key is pressed. Using Table 5-8, set the DIO 1-8 switches to the octal codes indicated and handshake the 7 bytes (press EXECUTE) into the 3437A. (The 3437A terminates the Binary Program mode after the 7th byte is read into the 3437A.)

5-59. Verify that the 3437A is programmed as follows: (Press LOCAL to obtain keyboard control.)

DELAY	500 μs
NRDGS	1976
ENAB RQS	4
RANGE	1 V
TRIGGER	INT
FORMAT	ASCII

5-60. ADJUSTMENT PROCEDURE.

WARNING

The following adjustment procedures require that the top cover be removed. Be extremely careful when performing these procedures since lethal voltages are exposed. Be especially careful around the line filter and fuse holder located in the top left rear corner of the instrument.

5-61. Introduction.

5-62. The adjustment procedure requires no additional test equipment and consists of two adjustments that are located on the A1 analog board.

a. Offset Adjust. The offset adjust (R67) compensates for internal offsets within the analog measurement circuitry, and is adjusted for a zero display with the input terminals shorted.

b. Attenuator Compensation (10 volt range). The attenuator compensation adjustment (C4) adjusts the frequency response of the attenuator so that the proper response over the specified 10 volt frequency range is obtained.

1. An internal test source (12 V step) and an internal test trigger is used to perform the adjustment. The test source is connected to the input terminals, and the test trigger is connected to the delay logic (Ext Trig input). The 3437A delay is programmed for 1 μs, and C4 is adjusted for a zero display.

5-63. Preliminary.

a. With the power cord removed from the instrument, remove the top cover (fastener located at rear of top cover).

b. Remove the 3 screws that fasten the left side of the logic board to the chassis. (The screws are located opposite the logic board hinges.)

c. Set the instrument on its right side, and lower the logic board to a horizontal position.

d. Apply power to the instrument.

NOTE

With the logic board extended, the component side of the analog board (illustrated on the guard enclosure) is accessable and provides access to adjustments and test points.

5-64. Adjustments.

5-65. Offset Adjust: A1 Analog Board.

a. Program the 3437A keyboard as follows:

DELAY	.01
NRDGS	9999
RANGE	.1 Volt
TRIGGER	INT

b. Using a shorted triax connector, ground the analog input. (Connect the three ends of the triax test cable together.)

c. Adjust the offset adjust (left-center) for a center-zero display.

1. Set R67 for a 0.001 display.
2. Rotate R67 CW to a point midway between the transition of 0.001 and 0.000 (Note the position of R67).
3. Set R67 for a -0.001 display.
4. Rotate R67 CCW to a point midway between the transition of -0.001 and 0.000 (Note the position of R67).
5. Set R67 midway between the positions noted.

5-66. 10 Volt Range Compensation: A1 Analog Board.

a. Connect the internal test source (located on the A2 logic board) to the analog input terminals, and test trigger to the delay logic external trigger input (Figure 5-12).

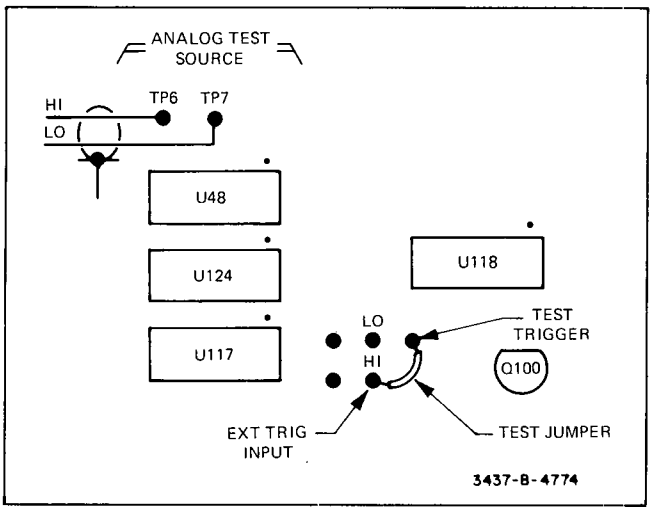


Figure 5-12. Analog Test - Source.

b. Set the 3437A as follows:

DELAY	1 μs
NRDGS	1
RANGE	10 V
TRIGGER	EXT

NOTE

The 10 V range compensation adjustment must be performed with the analog board within the guarded enclosure.

c. Adjust the 10 volt range compensation (bottom right) for a center-zero display (adjustment tool removed).

d. Turn the instrument off and remove the line cord and test cable.

e. Replace the 3 screws that fasten the logic board to the chassis (HP-IB cable tucked between the power transformer and rear panel).

f. Replace the top cover.

5-67. SELECT COMPONENTS.

5-68. Introduction.

5-69. Select components (components whose values are determined by instrument performance) provide a means to compensate for the tolerance of manufactured components. The 3437A uses 8 select components (Table 5-9).

5-70. Select Component Algorithms.

5-71. A1C3 — Input Attenuator Frequency Compensation.

a. Remove existing C3.

b. Configure the 3437A for the 10 volt range compensation adjustment (Paragraph 5-66).

c. Adjust C4 to a position of minimum plate overlap (minimum capacitance).

d. Select C3 according to Table 5-10.

Table 5-9. 3437A Select Components.

Component	Function	Select When Following Components Are Changed	Value [1] Select Procedure	Probable Error Symptoms For Incorrect Selected Value
A1C3	Input Attenuator Frequency Compensation	C_1, C_2, Q_3	Field Selected (Refer to 5-71)	Bandwidth (10 volt range)
A1R8	Input Attenuator Resistance Compensation	R_1	Factory Selected (R_1/R_8 Matched Set)	Accuracy (10 volt range)
A1R14	A_2 Q_3 Offset Compensation	Q_3	Factory Selected (Q_3/R_{14} Matched Set)	Offset
A1R18	A_2 Q_3 Gm Compensation	Q_3	Factory Selected (Q_3/R_{18} Matched Set)	Offset
A1R36 & Trim Tabs	A_2 Q_3 Gain Adjustment	CR_{19}, Q_3 R_1, R_{58}, U_{11}, U_{12}	Field Selected (Refer to 5-72 & 5-74)	Accuracy (all ranges)
A2R211	Sets Outguard Power Supply +5 Volt Output	U_{203}	Field Selected (Refer to 5-75)	Outguard Logic Failure
A2R237	Sets MPU Substrate Bias	MPU	Factory Selected (MPU/R_{237} Matched Set)	Outguard Logic Failure

[1] Factory-selected select components are included with the replacement part (matched set).

Table 5-10. C3 Select Procedure.

Volts Display	Procedure
≤ - 00.01	Error Condition—Check A_1C_1, A_1C_2, A_1CR_2, A_1CR_{38}, A_1U_1
- 00.02 thru - 00.68	Leave C3 an open circuit—Perform the A1R36 & Trim Tabs Algorithm (5-72)
- 00.69 thru - 01.20	Select C3 as 1.5 pF
- 01.21 thru - 01.91	Select C3 as 3.9 pF
≥ - 01.92	Error Condition—Check A_1C_1, A_1C_2, A_1CR_2, A_1CR_{38}, A_1U_1

e. Table 5-11 shows C3 values and corresponding part numbers.

Table 5-11. C3 Values.

C3	-hp- Part Number
1.5 pF	0160-2238
3.9 pF	0160-2247

5-72. A1R36 and Trim Tabs – A2Q3 Gain Adjustment.

5-73. Trim Tabs – A2Q3 Gain Adjustment.

a. Remove R36 and R1 Trim Tabs (Figure 5-13).

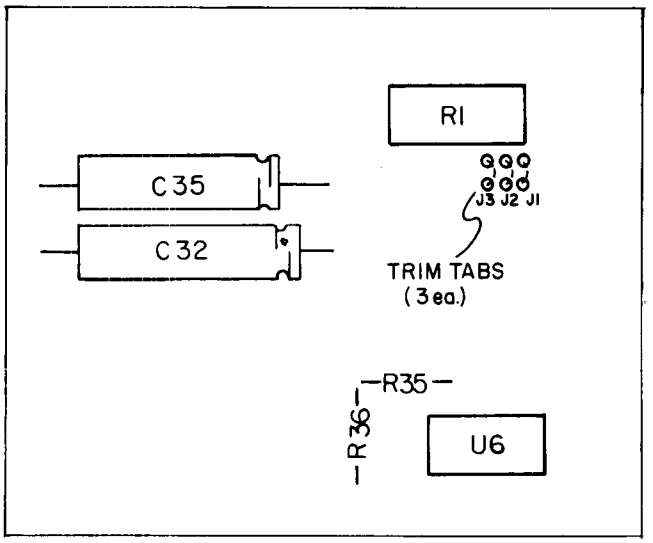


Figure 5-13. R36 and R1 Trim Tabs Location.

b. Trim Tab characteristics.

Table 5-12. Trim Tab Weighting.

J_3	J_2	J_1	N
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

1 = Short
0 = Open
N = $J_1 + J_2 + J_3$
J_1 = Jumper between R_1 Pins 13 & 14
J_2 = Jumper between R_1 Pins 14 & 15
J_3 = Jumper between R_1 Pins 15 & 16

c. Program the 3437A keyboard as follows:

DELAY 25
NRDGS 1
RANGE . . . . . 1 V
TRIGGER . . . . . .INT

d. Apply 1 mV ± 100 μV to the input connector.

e. Adjust the offset adjust (A2R67) for a display midway between the transition of 0.000 and 0.001.

f. Apply + 1.000 V ± 100 μV to the input connector.

g. Find the smallest N for which the volts display indicates ≤ 0.992 (Refer to Step b).

h. Apply a jumper across R36. If out of 10 readings, none are ≤ 1.000, then N is correct. If not, decrease N by 1.

i. Install the Trim Tabs corresponding to N.

5-74. R36 – A1Q3 Gain Adjustment.

a. Open R36 – Determine the input voltage required to cause the volts display to indicate between the transition of 1.000 and 1.001. Note voltage as V_1.

b. Apply a jumper across R36 – Repeat the procedure as outlined in Step a. Note voltage as V_2.

c. Measure and record the value of R35 (typical value is 54 K).

d. Calculate:

1. $GR = \frac{V_1 - .001\ V}{V_2 - .001\ V} \cong 1.02$ Gain Ratio

2. $R_{TH} = (GR - 1)\ R35$ Thevenin Resistance

3. $R_X = R_{TH} \frac{1\ V}{V_1 - 1.001\ V}$ Shunt Trim Required

4. $R_T = R_X - R35$ Trim Required

e. If $R_T \geq 10.0$ K, select R36 as the nearest 1% value to R_T.

f. Otherwise, Calculate:

1. $GR' = 1 + \frac{R_{TH}}{R35' + R_T}$

Where $R_{TH}' = 0.91$ K
$R35' = 53.6$ K

2. $GR'' = 10^{-4}$ x largest in $(10^4\ GR' + .5)$

3. $R_X' = \frac{R_{TH}'}{(GR'' - 1)}$

4. $R_T' = R_X' - R35'$

g. Select R36 as the closest 1% value to R_T'.

5-75. A2R211 – Outguard Power Supply +5 Volt Output.

a. Remove A2R211 from outguard power supply.

b. Measure and record the +5 volt output (A2U107 - 8 and 16).

c. If the +5 volt output is < 4.79 volts or > 5.44 volts, the power supply has failed (Refer to the Service Guide Flowchart).

d. Refer to Table 5-13 to determine the value of A2R211.

Table 5-13. A2R211 Values.

+5 Volt Output	R_{211}	-hp- Part Number
< 4.816 V	Open Circuit	
4.832 ± .016 V	1 MΩ, 5%	0683-1055
4.864 ± .016 V	549 K, 1%	0698-6084
4.896 ± .016 V	365 K, 1%	0757-0478
4.928 ± .016 V	274 K, 1%	0757-0475
4.960 ± .016 V	215 K, 1%	0698-3454
4.992 ± .016 V	182 K, 1%	0757-0471
5.024 ± .016 V	154 K, 1%	0698-4521
5.056 ± .016 V	137 K, 1%	0698-4518
5.088 ± .016 V	121 K, 1%	0757-0467
5.120 ± .016 V	110 K, 1%	0757-0466
5.152 ± .016 V	100 K, 1%	0757-0465
5.184 ± .016 V	90.9 K, 1%	0757-0464
5.216 ± .016 V	84.5 K, 1%	0698-5410
5.248 ± .016 V	78.7 K, 1%	0698-4508
5.280 ± .016 V	73.2 K, 1%	0698-4506
5.312 ± .016 V	68.1 K, 1%	0757-0461
5.344 ± .016 V	63.4 K, 1%	0698-3280
5.376 ± .016 V	60.4 K, 1%	0698-3572
> 5.392 V	57.6 K, 1%	0698-4500

5-76. FRONT PANEL REMOVAL/REPLACEMENT PROCEDURES.

5-77. Introduction.

5-78. The front panel removal/replacement procedures are organized as follows:

a. Display PC Board (03437-66503) - Removal/replacement procedure.

b. Switch (5060-9436) - Removal/replacement procedure.

c. Switch LED (1990-0486) - Removal/replacement procedure.

d. Display (1990-0598) - Removal/replacement procedure.

5-79. Display PC Board - Removal/Replacement Procedure.

a. Remove all cables (including line cord) from instrument.

b. Remove top and bottom instrument covers.

c. Remove plastic trim-strip from top of front casting.

d. Set line switch to the "ON" position.

e. Using a small flat-blade screwdriver, separate the line switch extender shaft from line switch (Figure 5-14).

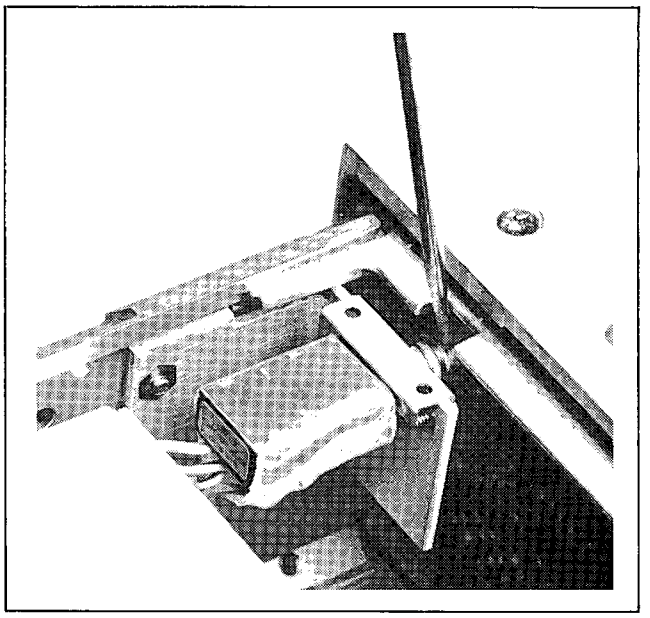


Figure 5-14. Line Switch Extender Shaft Removal.

f. Remove the 10 screws that fasten the front casting to the front panel.

g. Separate front panel assembly from front casting (Figure 5-15).

CAUTION

When installing the front panel assembly in the front casting, make sure the off-centered mounting option on the line switch extender shaft is aligned with the line switch, and is pointing towards bottom of instrument.

h. Separate dress panel from Display P.C. Board assembly.

CAUTION

When reassembling front panel, make sure LEDS (soldered to Display P.C. Board assembly are aligned with the dress panel.

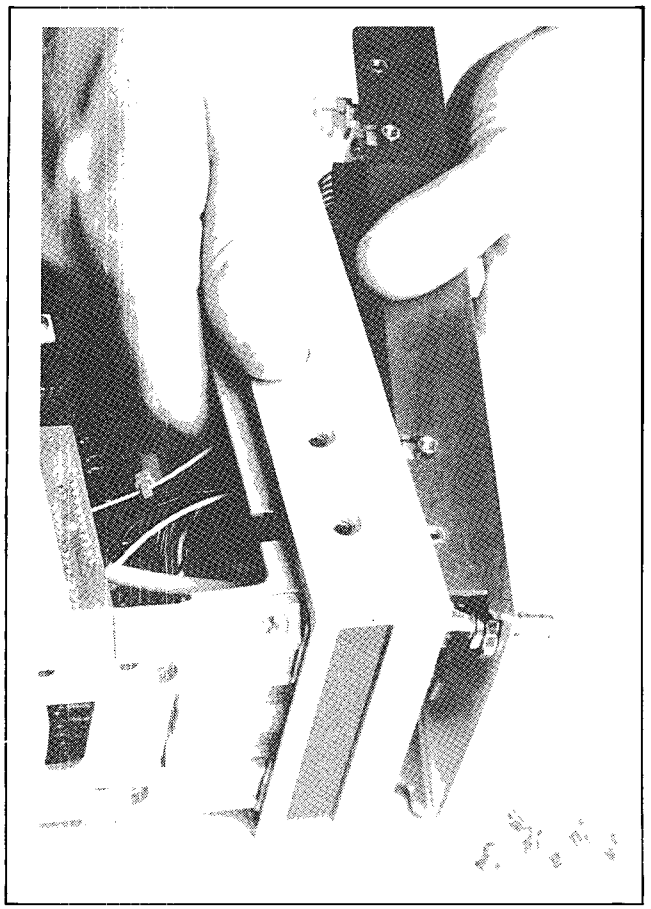


Figure 5-15. Front Panel/Front Casting Separation.

i. Using a small flat-blade screwdriver, free the Display P.C. Board assembly from the instrument by removing the 38 pin connector from Display P.C. Board assembly (Figure 5-16).

j. To replace the Display PC Board assembly, reverse the above procedures, making sure to observe cautions noted in Steps f and h.

NOTE

Display Board PC assembly replacement (03437-66503), does not include display, display filter, front panel switches, line switch extender shaft, or plastic key caps.

5-80. Switch—Removal/Replacement Procedure.

a. Perform Steps a through j of the Display P.C. Board assembly removal/replacement procedure.

b. Remove the 9 screws that fasten switch-clamping subpanel to Display P.C. Board assembly. Remove switch-clamping subpanel (Figure 5-17).

CAUTION

Switches are not attached to Display P.C. Board assembly.

c. Remove defective switch.

d. Remove defective switch key-cap. (It may be necessary to destroy defective switch in order to remove key-cap.)

e. Install new switch onto the Display PC Board assembly.

f. Replace switch-clamping subpanel. (Install key-cap on new switch.)

g. Perform Step j of the Display PC Board removal/replacement procedure.

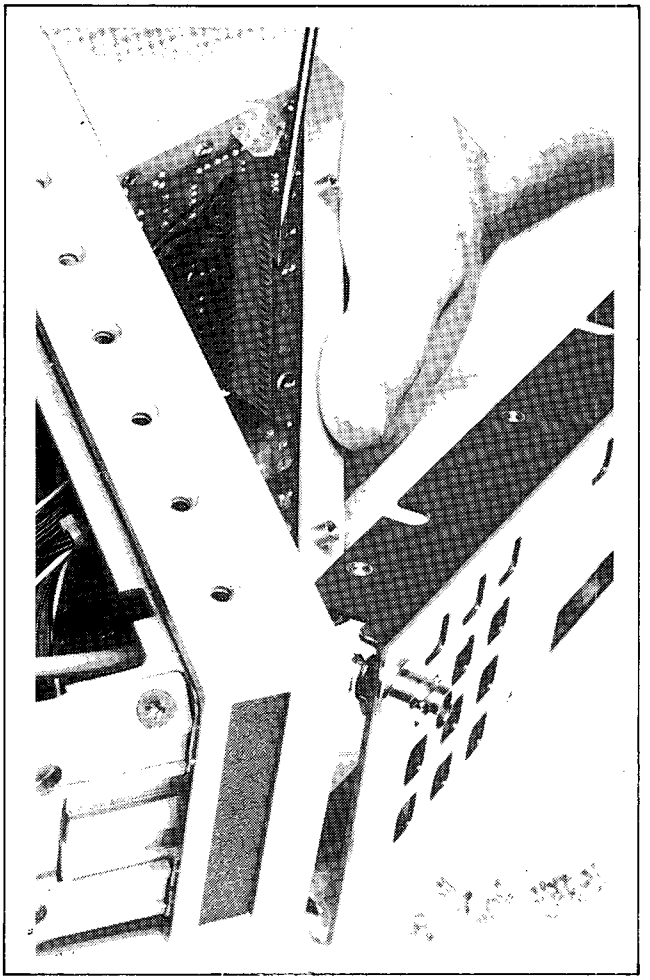


Figure 5-16. Display Connector Removal.

5-81. Switch LED—Removal/Replacement Procedure.

a. Perform steps a through i of the Display P.C. Board assembly removal/replacement procedures.

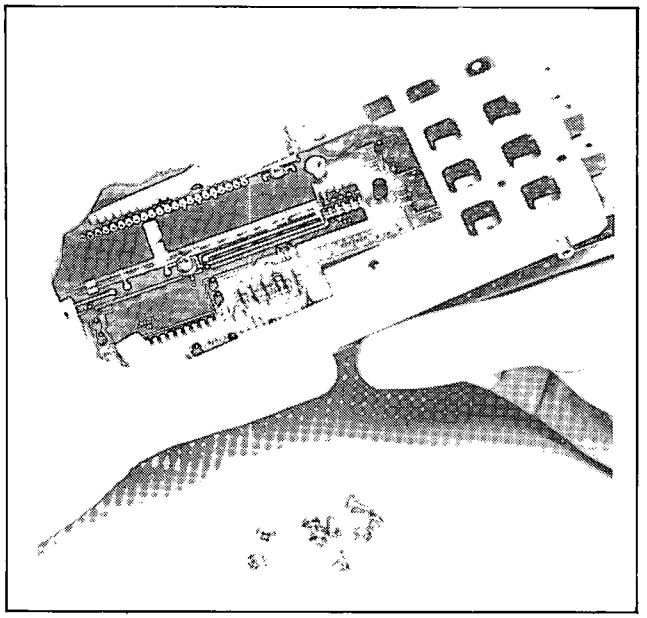


Figure 5-17. Switch-Clamping Subpanel Removal.

b. Remove the 9 screws that fasten switch-clamping subpanel to Display P.C. Board assembly. Remove switch clamping subpanel (Figure 5-17).

c. Remove switches.

d. Desolder defective LED.

e. To insure that the newly installed LED will not rub against the switch plunger (when switch is pressed), a soldering guide is required. Fabricate a soldering guide from a piece of 0.125" I.D. thin walled plastic tubing 3/16" in length. (If tubing is not available, a 3/16" strip of paper rolled to obtain an approximate I.D. of 0.125" is satisfactory.)

f. Insert tubing (or rolled paper) into bottom of defective LED's switch plunger (Figure 5-18).

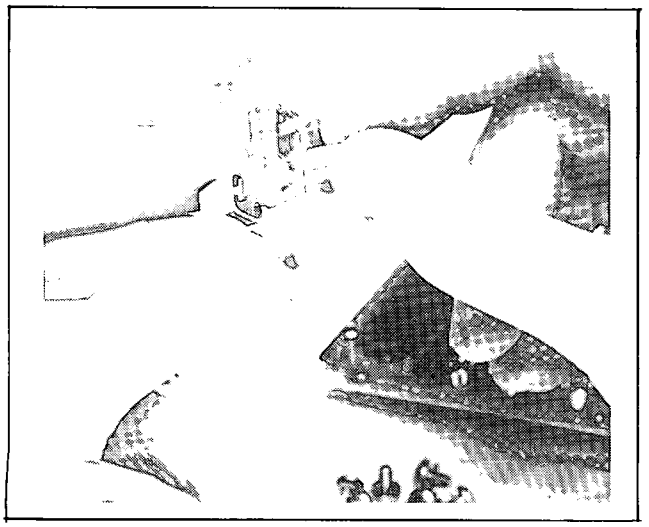


Figure 5-18. Tubing Insertion Into Switch Plunger.

g. Insert new LED into bottom of switch plunger containing tubing (Figure 5-19).

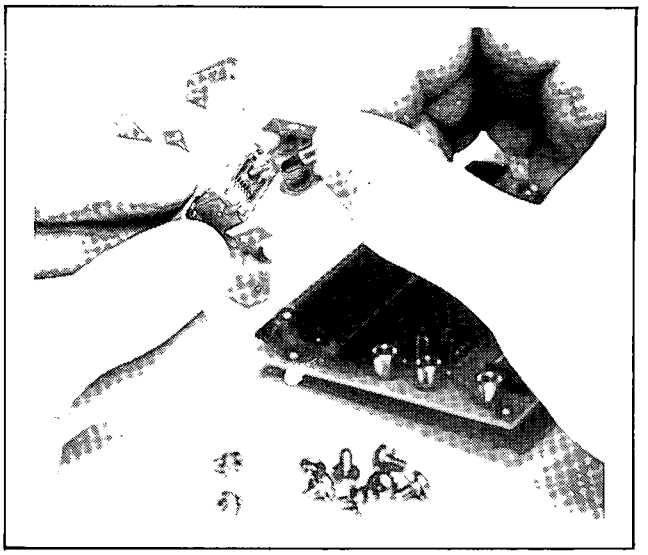


Figure 5-19. LED Insertion Into Switch Plunger.

h. Rotate LED (in bottom of switch plunger) so that the shortest lead will pass through the Display P.C. Board assembly mounting hole that is identified with a dot (Figure 5-20).

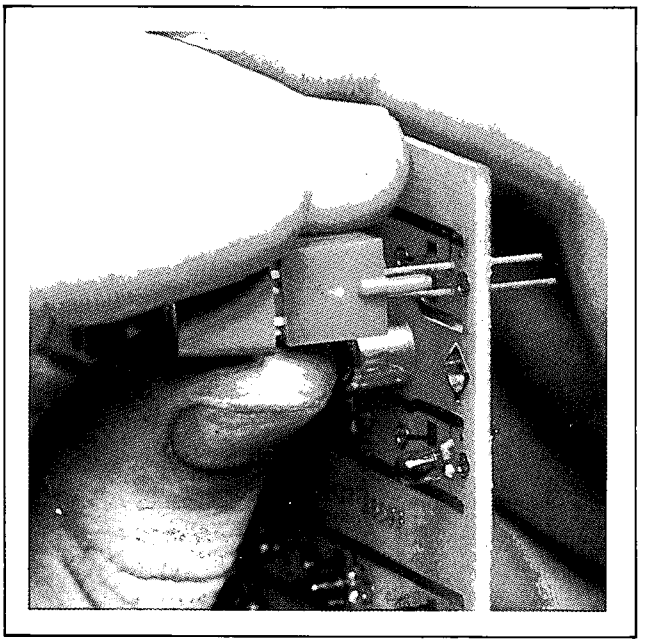


Figure 5-20. Display P.C. Board Assembly Switch/LED Installation.

i. Install switch and LED combination onto the Display PC Board assembly (Figure 5-20).

j. Grasp LED leads (back side of Display P.C. Board assembly) and pull LED flush against front side of Display P.C. Board assembly (Figure 5-21).

k. Solder LED to Display P.C. Board assembly.

CAUTION

Press switch against front surface of Display P.C. Board assembly while soldering LED. Do not melt plastic legs or allow solder flux to get into switch.

l. Remove switch.

m. Remove tubing (or rolled paper) from switch plunger.

n. Deflux Display PC Board assembly.

NOTE

Do not allow Display (1990-0589) to come in contact with either water or solvents.

o. Place switch over LED and operate several times to insure switch plunger does not rub against LED, and that the light-pipe in key-cap does not contact LED before switch plunger bottoms.

CAUTION

If the results of Step o are not satisfactory, repeat the LED installation procedure.

p. Install switch (over new LED) onto Display P.C. Board assembly. (Install remaining switches.)

q. Replace switch clamping subpanel.

Figure 5-21. Display P.C. Board Switch/LED Alignment.

r. Perform Step j of the Display PC Board removal/replacement procedure.

5-82. Display—Removal/Replacement Procedures.

a. Perform Steps a through i of the Display PC Board assembly removal/replacement procedure.

b. Remove the three mounting screws (and associated hardware) that fastens the Display to the Display Board PC assembly.

c. Lift Display off connector contacts by raising left side of display (Figure 5-22).

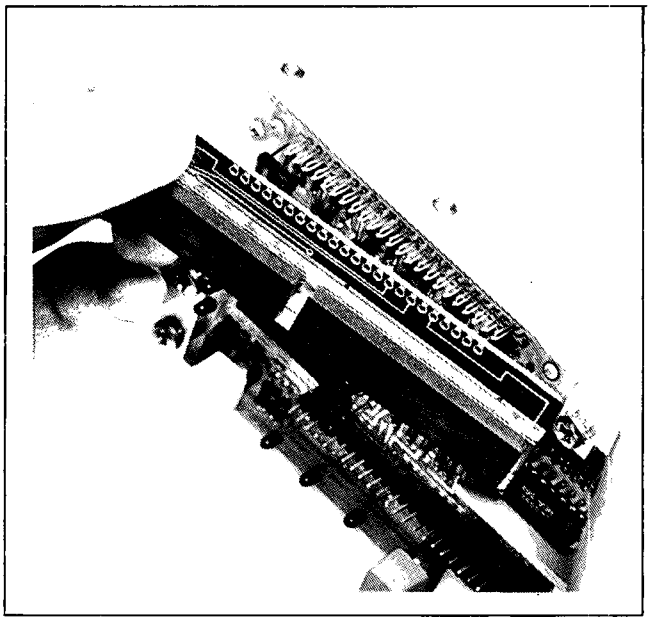


Figure 5-22. Display Removal.

d. To replace Display, reverse the above procedure.

e. Perform Step j of the Display Board PC assembly removal/replacement procedure.

5-83. TROUBLESHOOTING PROCEDURES.

5-84. Analog/Power Supply Circuits.

5-85. Conventional techniques (voltage and waveform analysis) are used to troubleshoot the analog and power supply circuits. Detailed procedures are outlined in the Service-Guide Flowchart (Figure 5-24).

5-86. Logic Circuits.

5-87. Troubleshooting microprocessor—based logic requires a technique that differs from that used to troubleshoot conventional—based logic circuits.

5-88. During normal instrument operation, the 3437A microprocessor accesses and executes program instructions contained in external memory. The normal sequence of program instruction is disrupted when the microprocessor is forced into a program subroutine or (because of an interrupt request) is forced to jump to a interrupt - request service subroutine.

5-89. Executing nonsequential program instructions (typical event), causes changing data patterns to be present within the logic circuitry. To overcome this situation, a unique method (developed by Hewlett-Packard) is used to troubleshoot the 3437A microprocessor based logic circuits. The method is referred to as Data Stream Analysis (DSA).

5-90. The Data Stream Analysis technique forces the microprocessor to continuously execute test routines. This results in continuous repetitive data patterns to be present at data nodes throughout the logic section.

5-91. A logic tracer (used to probe the logic circuit data nodes) identifies the repetitive data patterns by generating a signature (4 digit alpha - numeric code) characterizing the accumulative data pattern occuring over a specific period of time.

5-92. The test signatures obtained are then compared to reference signatures (signatures generated by an instrument that is known to be in proper working order). Corresponding signatures (test & reference) imply that the section of the logic circuit that is exercised by the test routine, is functioning properly. If corresponding signatures are not obtained, then that particular section of the logic circuit is not functioning properly, and service procedures outlined in the troubleshooting flowcharts are followed.

5-93. To force the microprocessor to execute test routines (generation of continuous repetitive data patterns) a test ROM is used. The test ROM contains 8 test routines that exercises various sections of the logic circuitry. An additional test (one that does not require the test ROM) is also provided, resulting in a total of 9 separate tests available as an aid in troubleshooting the Logic/Display circuitry. The following paragraphs describe these tests.

NOTE

Since the 3437A uses more than 2000 (of the possible 2048) words of program instruction for normal instrument operation, an additional ROM (512 words) is required to implement the DSA technique. When troubleshooting the logic circuits, the program control ROM that is socket mounted is replaced with the DSA test ROM.

5-94. Program Control ROM. The program control ROM test provides a method of verifying the contents of the program control memory (U41 - U44). The bi-directional buffers (U28 - U31) are removed, causing the contents of the program control memory to be sequentially written onto the data and instruction bus.

NOTE

Removing the bi-directional buffers forces the MPU data lines high, allowing the MPU program counter to continuously cycle between 0-2047.

5-95. The entire 2048 words (bytes) of instruction can be verified by the DØ - D7 signature set. If the signatures are not correct, the logic tracer is configured to monitor the data and instruction bus for the period of time that a specific ROM is enabled, allowing the defective ROM to be identified. A defective MPU (program counter capability) can also be identifed by monitoring the program address bus (PA0 - PA10) signature set (program control ROM inputs).

5-96. DSA ROM. The DSA ROM test provides a method of verifying the contents of the DSA test ROM. The test is performed in a similar manner as described in the program control ROM test, with the exception that the DSA test ROM is substituted in place of the program control ROM (U41) causing the Contents of the DSA test ROM (512 instructions) to be written onto the data and instruction bus during program counter steps 0-511.

5-97. MPU and MPU "Write" Interface Logic. The MPU and MPU–write–interface logic test provides a method of verifying that the MPU internal circuitry and the MPU write capability, as well as the logic devices that the MPU writes into, are functioning properly. The test routine exercises the MPU internal circuitry, then forces the MPU to write all possible data combinations into each logic device controlled by the device - select - write logic.

5-98. Scan Address. The scan address test provides a method of verifying proper operation of the scan counter, digit and annunciator memories, and display logic circuits. Data is written into the digit and annunciator memories, then the MPU is forced into a non read/write mode so that the contents of the digit and annunciator memories are scanned and written onto the annunciator and digit data bus, allowing signatures to be verified throughout the display and display control logic circuits.

5-99. MPU and MPU "Read" Interface Logic. The MPU and MPU–read–interface logic test provides a method of verifying that the MPU read capability as well as the logic devices that the MPU reads from, are functioning properly. The MPU writes into each logic device (that has read capability), then reads back the same data. Since this test depends upon the proper operation of the MPU and MPU write interface logic, as well as the digit and annunciator memories, the DSA tests previously described must be completed prior to performing this test.

5-100. HP–IB Interrupt Encode Logic. The HP–IB interrupt encode logic test provides a method of verifying proper operation of the HP–IB interrupt encode logic. An HP–IB test connector is used so that the talk–interface logic functions as a data–source for the listen interface logic. The test routine provides stimulus for each logic device within the interrupt encode logic.

5-101. Delay Logic. The delay logic test provides a means of verifying proper operation of the delay logic circuitry (with the exception of the analog interpolator). The test routine provides stimulus for each logic device in the delay logic circuitry.

5-102. Delay Logic Downcounters. The delay logic downcounter test provides a method of verifying proper operation of the downcounter chain (U105–U112). The downcounters are preset to binary 9 (1001), then are forced to count towards zero. When each downcounter underflows, it presets itself, resulting in a continuous 9–0 downcount sequence.

5-103. Analog/Logic Interface. The analog/logic interface test provides a method of generating the logic control signals (range bits and successive approximation register clock) used to interface the analog and logic circuits. This test is intended to be used primarily as an analog circuit troubleshooting tool.

5-104. Annunciator and Digit Display Verification. The annunciator and digit display verification test provides a method of verifying proper operation of the annunciator and digit displays. All annunciators are illuminated, and the alpha symbols "–" and ".", as well as the integers "0–9" are displayed by the digit display. Signatures are not required for this test.

5-105. Service–Guide–Flowchart.

5-106. The service guide flowchart (Figure 5-24) illustrates the sequence of events that should be performed whenever the 3437A requires service.

5-107. Cabling Diagram.

5-108. Figure 5-23 illustrates the 3437A interconnecting cables. (The 3437A interconnecting cables are referred to in the troubleshooting flowcharts.)

5-109. TROUBLESHOOTING GUIDES.

5-110. Introduction.

5-111. The following paragraphs describe 3437A troubleshooting techniques along with illustrating a specific troubleshooting example.

5-112. Troubleshooting Techniques.

5-113. Input Amplifier (A1Q3) Network. Preliminary.

a. Remove Q6 drain from the HI - Z node and connect it (Q6 drain) to TP15 (+9 volts).

b. Change R14 to 50 kΩ. (If C11 = 6.8 μF, remove from circuit.)

c. Connect the junction of C11/R14 to the HI - Z node.

d. Ground Q3 A/B gates.

5-114. Measure the currents through R14 and R19 (they should be equal). If $IR_{14} \neq IR_{19}$, then a HI–Z node component is functioning either as a current source ($IR_{14} < IR_{19}$) or as a current sink ($IR_{14} > IR_{19}$). $IR_{14} \cong 409\ \mu A$.

5-115. Measure the currents through R17 and R21 (they should be equal and the sum should = IR_{19}). If $IR_{17} \neq IR_{21}$, then a stage imbalance exists. ($IR_{17} \cong 205\ \mu A$).

5-116. Measure the voltages across R_{14} and R_{15} (they should be equal). If $VR_{14} \neq VR_{15}$, then the current mirror network is defective ($VR_{14} \cong 17.8$ V).

5-117. Reconfigure the input amplifier to its original state (refer to Paragraph 5-113).

5-118. Program the 3437A keyboard as follows:

RANGE. . . . . .1 volt
TRIGGER . . . . . HOLD/MAN

5-119. Apply a 200 mV p–p (1 kHz) voltage to the input connector.

5-120. View the waveform at the HI–Z node. The waveform amplitude should be ≅ 4 volts peak–to–peak.

5-121. View the waveform at TP2 (S/H Input). The waveform amplitude should be the same as in 5-120.

5-122. Analog-to-Digital Converter. Program the 3437A keyboard as follows:

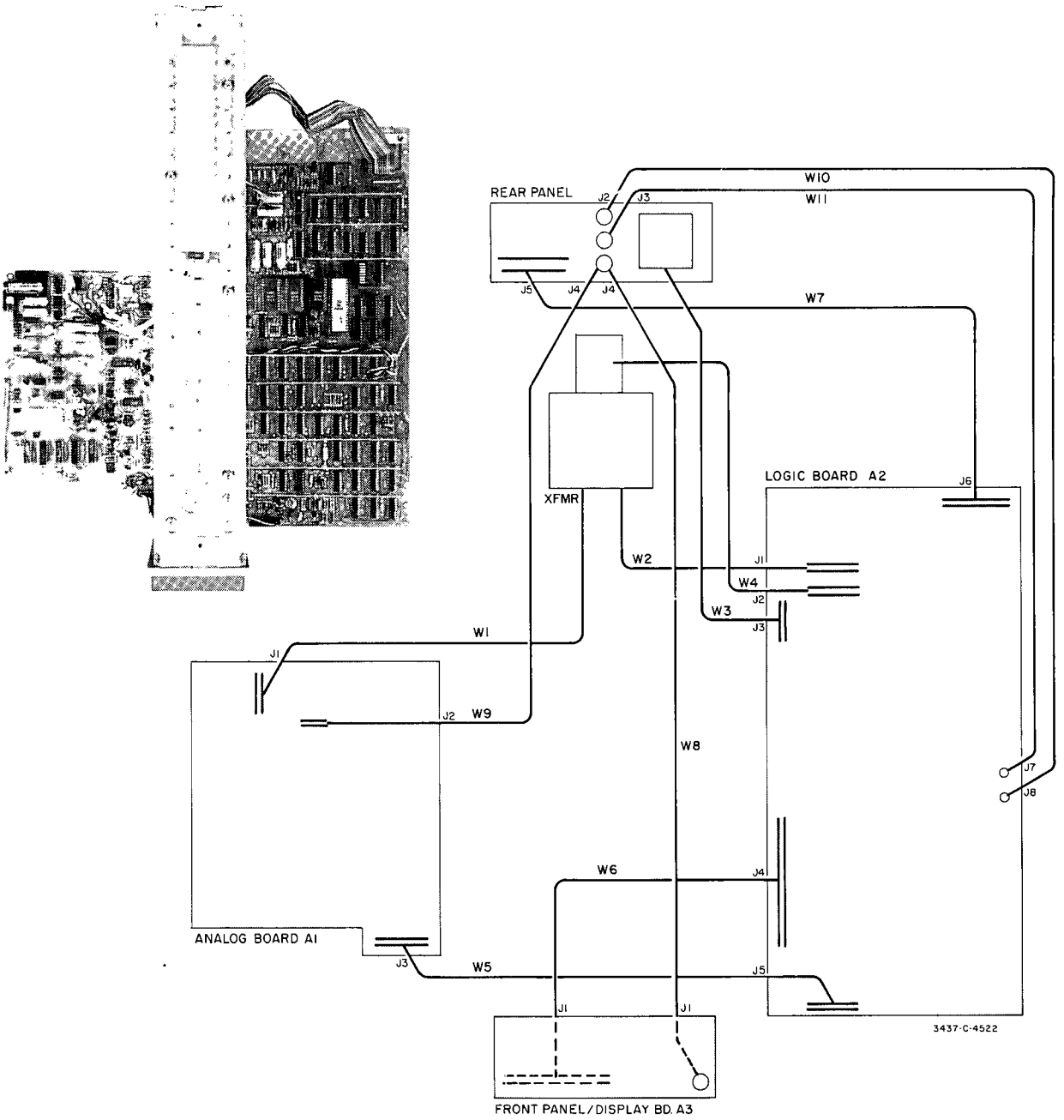
DELAY. 001
NRDGS. 9999
RANGE. . . . . 1 volt
TRIGGER . . . . . INT

5-123. Connect TP8 to TP18. (Forces a "–" overload condition, causing the successive approximation registers to continually set and clear the Q0–Q13 output stages.)

5-124. The performance of the successive approximation registers, converter switches, and the weighted resistor array can be verified by monitoring corresponding outputs of U17–U18, U14–U16, and R58 (1).

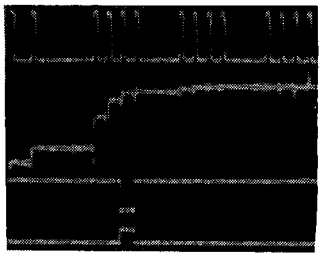
5-125. DSA Tests.

5-126. The DSA tests can be abbreviated by verifying only those signatures pertaining to the instrument problem. If a delay–related problem exists, the signatures verifying the HP–IB "write" capability (DSA test E–1) do not correspond to the problem, therefore, do not need to be verified.



CABLE	NO. WIRES	FROM ⟷ TO		
W1	4	PWR XMFR	A1	PWR XMFR SECONDARY
W2	6	PWR XMFR	A2	PWR XMFR SECONDARY
W3	4	FAN	A2	FAN POWER
W4	6	CHASSIS MOUNTED COMPONENTS	A2	CONNECTS OUTGUARD POWER SUPPLY COMPONENTS TO A2 BOARD
W5	10	A1	A2	ANALOG/LOGIC INTERFACE
W6	28	A2	A3	LOGIC/DISPLAY INTERFACE
W7	24	(A2 & REAR PANEL)		HP-IB (BI-DIRECTIONAL)
W8	2	FRONT PANEL	REAR PANEL	PARALLELS ANALOG INPUT CONNECTORS
W9	2	REAR PANEL	A2	ANALOG INPUT
W10	2	REAR PANEL	A2	DELAYED TRIGGER OUTPUT
W11	2	REAR PANEL	A2	EXTERNAL TRIGGER INPUT

Figure 5-23. 3437A Cabling Diagram.



5-127. The annunciator and digit display verification (DSA test E–8) can be performed in lieu of checking the outguard clocks (10 MHz and Scan) and power supply voltages. A successful test E–8 verifies these networks to be functioning properly.

5-128. The annunciator and digit display verification test can also be performed in lieu of the Scan address/display control test (DSA test E–2). A successful test E–8 verifies that those components checked in test E–2 are functioning properly.

5-129. General.

5-130. If the volts display indicates between a 1200–1600 count offset (10 volt range), and the Inguard power supply voltages are correct, the probable defect is A1R58.

5-131. If the "1" or "0" LED is illuminated and the volts display indicates 9999, the probable defect is opto–isolator A1U19.

5-132. If the 3437A does not turn on properly (keyboard not active, irregular display, etc.), a probable cause could be that the MPU switched +12 volts is not being applied in the proper sequence. To verify the switching sequence (illustrated in Figure 4-29) temporarily ground pin 40 of the microprocessor. If the 3437A begins to function properly, the probable defect is U201 of the outguard power supply.

5-133. Analog Circuit Troubleshooting Example.

5-134. Problem. A1U17 pins 8 and 16 shorted together.

5-135. Solution. The Service Guide flowchart indicates that the problem is most likely to be in the Analog measurement circuitry, and directs the user to verify the Inguard power supply voltages. The resulting power supply voltages are shown below:

Test Point	Voltage	Test Point	Voltage
TP13	+38.1 V	TP17	0 V
TP14	+22.8 V	TP18	0 V
TP15	+11.3 V	TP19	- 6.3 V
TP16	+ .58 V	TP20	- 10.6 V

5-136. Since the Inguard power supply voltages are incorrect, the user is directed to troubleshooting Flowchart C (Inguard Power and Reference Supplies).

5-137. Troubleshooting Flowchart C (all answers correct) directs the user to troubleshooting Flowchart C–1 (continuation of C).

5-138. Troubleshooting Flowchart C–1 identifies the problem to be excessive sink current existing at the Analog ground node, causing that node to be too negative. The user is directed to the Analog Ground diagram (P/O Inguard Power Supplies Troubleshooting Flowchart C–1) to identify the defective component(s).

5-139. Refer to the Analog ground circuit diagram (Table 5-14) for the following discussion.

5-140. Treating the Analog ground node like the "hub" of a wheel, and the test nodes as "spokes", meter each "spoke" (prior to its branch point) to determine which "spoke" contains an abnormally high current.

5-141. When the test node (carrying the highest current) is identified that node is metered (at each branching point) to identify the defective component(s). The test node voltages are shown below:

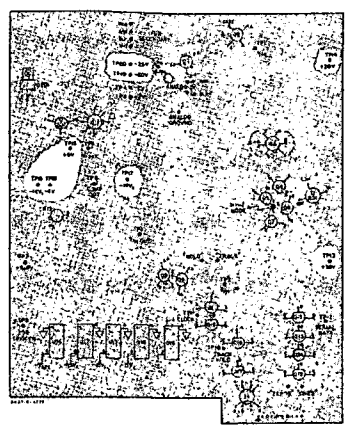
Test Node	Voltage (μV)	Test Node	Voltage (μV)
5	+302	28	0
9	+6	32	+5
14	+68	33	0
10	+12	31	- 2
12	0	34	- 591
19	+2	35	+2
22	+3	30	- 4
23	+2	36	0
25	0	39	+41

5-142. Since the path between node 34 and analog ground appears to contain the highest current (α 591 μV) the branches from node 34 are metered to determine which component is functioning as a current sink. The test-node voltages are shown below:

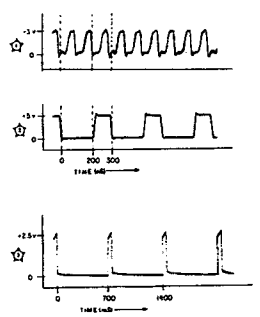
Test Node	Voltage (μV)
58	- 1094
57	- 1094
59	- 1153
60	- 1219
62	- 1519
63	- 1528
64	- 1585

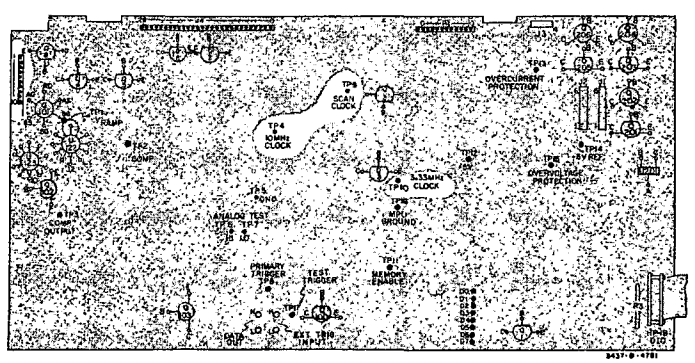
5-143. According to the test node voltages, node 64 is the node that is functioning as a current sink. The node is inspected (shorts, solder splash, etc.) and found to be satisfactory.

5-144. The corresponding test node component (A1U17) is replaced, restoring the instrument to normal operation. To complete the service procedure, the user should verify the analog and logic performance tests as outlined in the Service Guide flowchart.



ANALOG BOARD COMPONENT PIN-OUT





LOGIC BOARD COMPONENT PIN-OUT

NOTES

1. THE ANNUNCIATOR AND DIGIT DISPLAY VERIFICATION (DSA TEST-8) CAN BE PERFORMED IN LIEU OF CHECKING THE OUTGUARD CLOCKS (10 MHZ AND SCAN) AND POWER SUPPLY VOLTAGES. A SUCCESSFUL TEST E-8 VERIFIES THESE NETWORKS TO BE FUNCTIONING PROPERLY.

2. REFER TO TROUBLESHOOTING GUIDES PARAGRAPH 5-136.

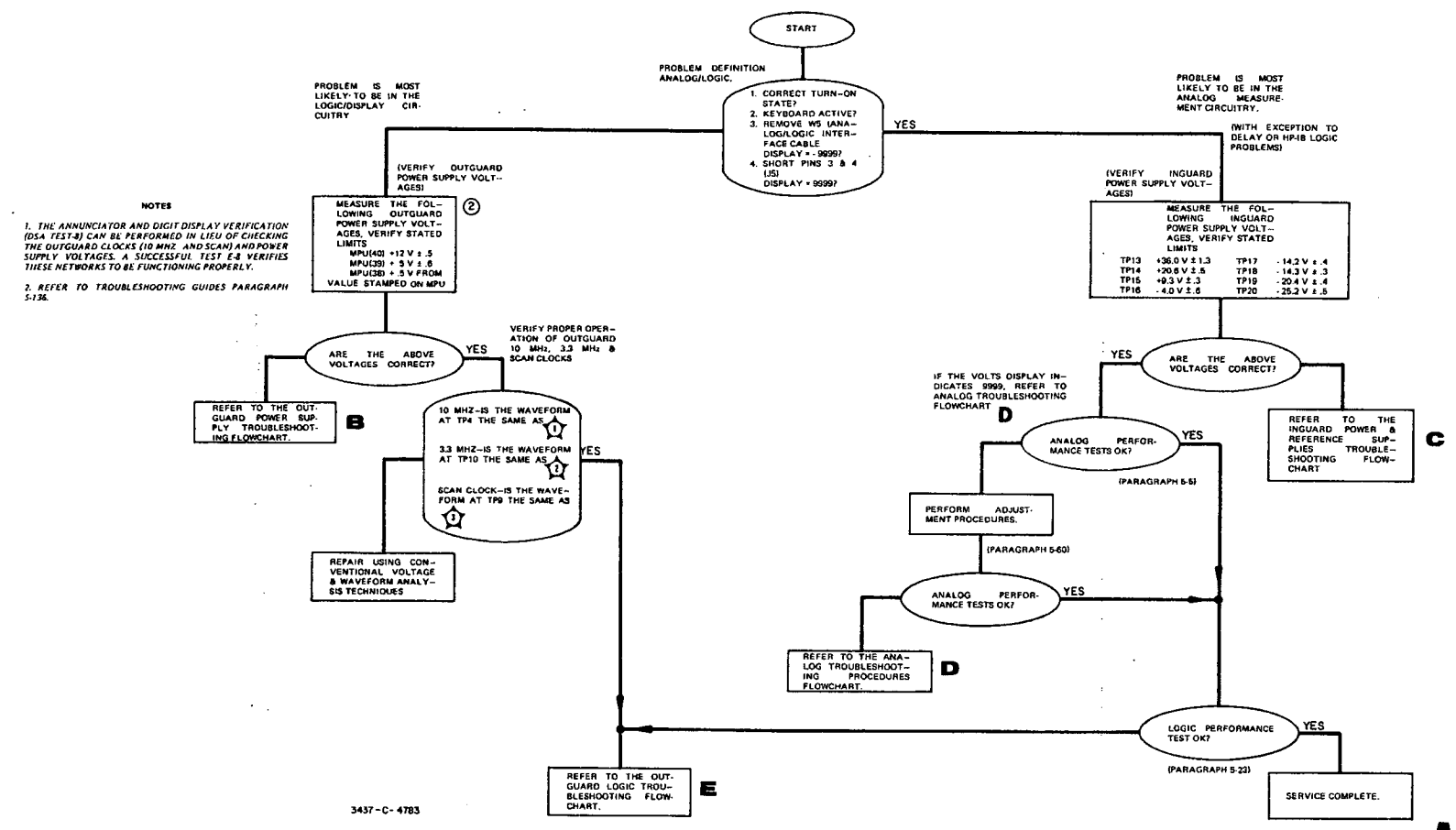
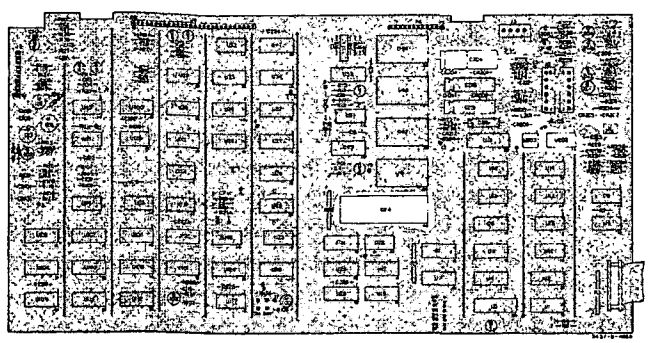
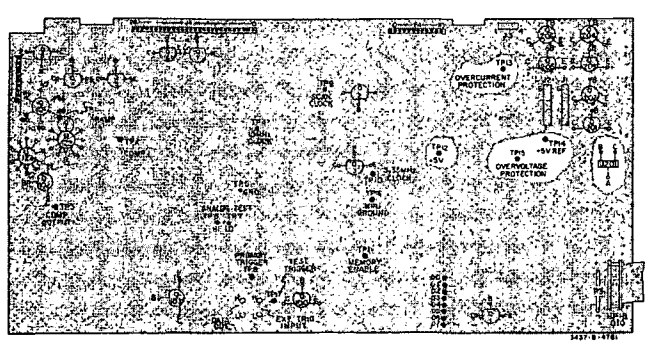


Figure 5-24. 3437A Service Guide Flowchart.



LOGIC BOARD COMPONENT LOCATOR



LOGIC BOARD COMPONENT PIN-OUT

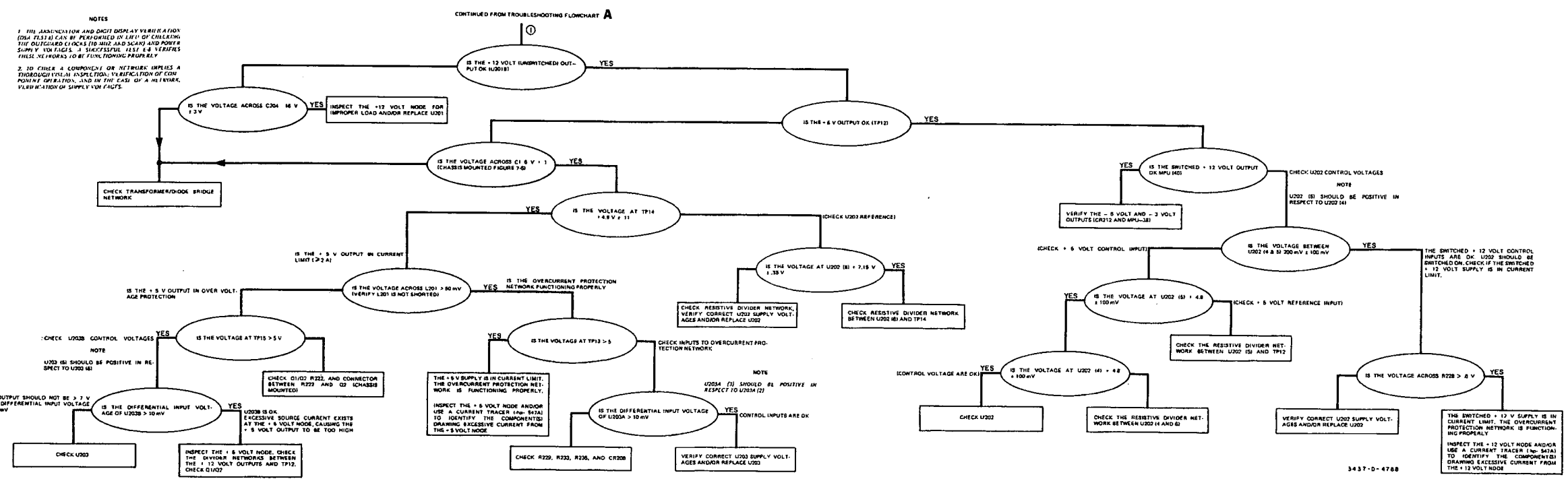
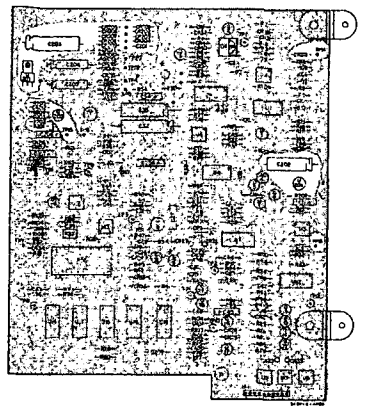
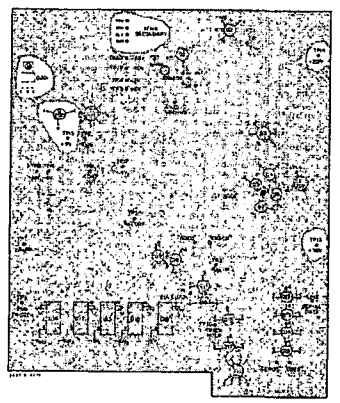


Figure 5-25. Outguard Power Supply Troubleshooting Flowchart.



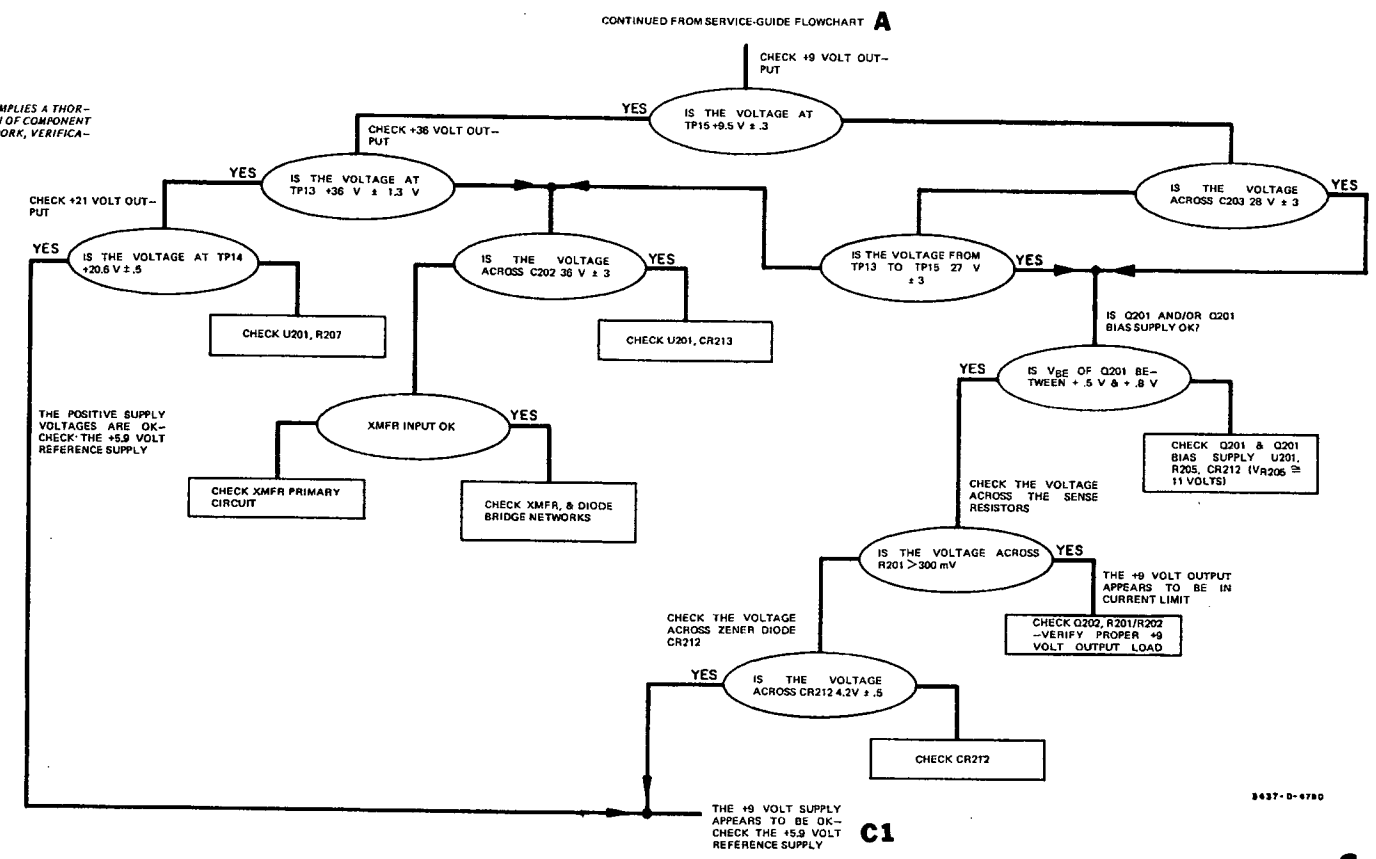
ANALOG BOARD COMPONENT LOCATOR



ANALOG BOARD COMPONENT PIN-OUT

NOTE

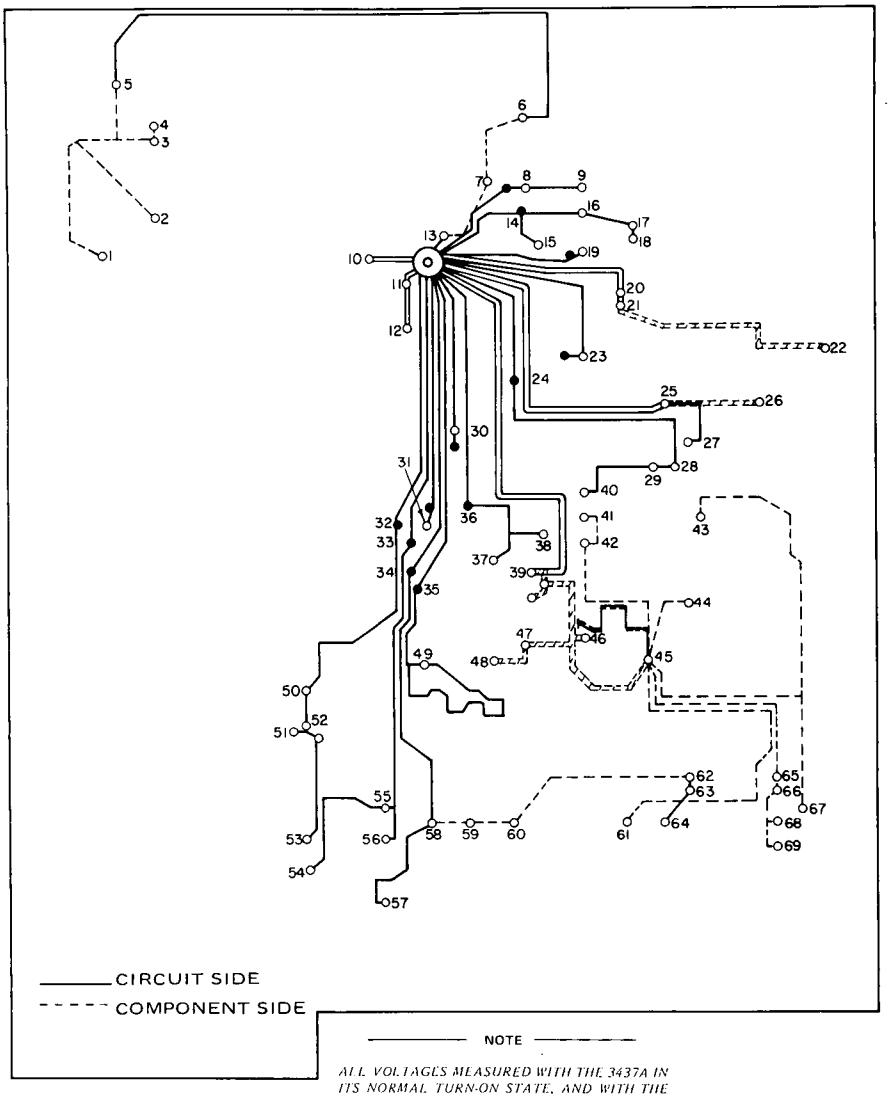
TO CHECK A COMPONENT OR NETWORK IMPLIES A THOROUGH VISUAL INSPECTION; VERIFICATION OF COMPONENT OPERATION, AND IN THE CASE OF A NETWORK, VERIFICATION OF SUPPLY VOLTAGES.



C

Figure 5-26. Inguard Power Supplies Troubleshooting Flowchart.

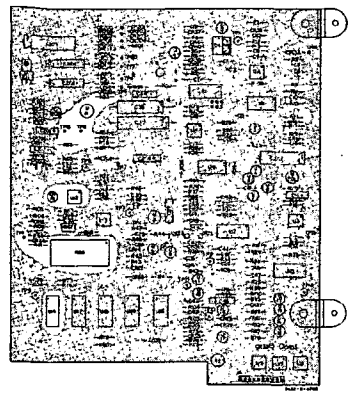
Table 5-14. Analog Ground Network.



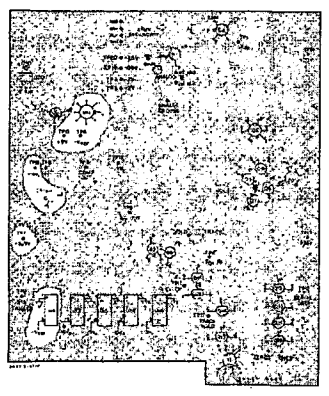
NOTE

ALL VOLTAGES MEASURED WITH THE 3437A IN ITS NORMAL TURN-ON STATE, AND WITH THE TEST DVM LOW INPUT TERMINAL CONNECTED TO THE ANALOG GROUND NODE.

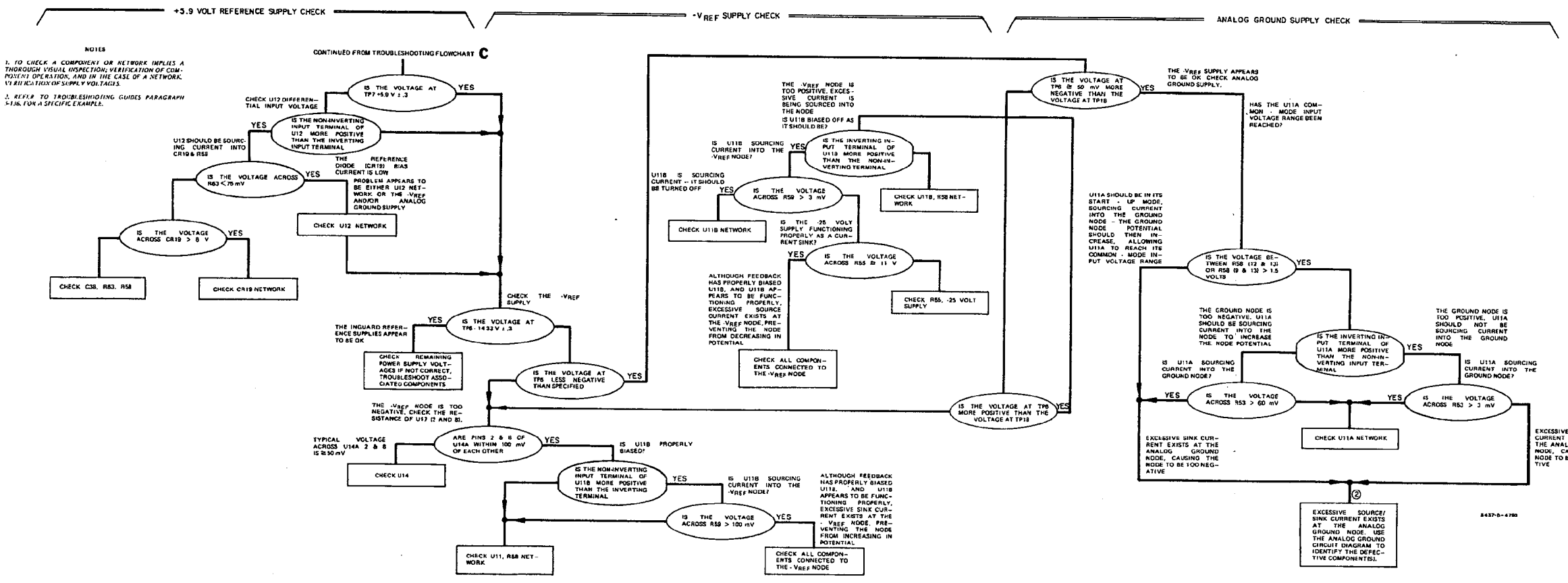
Test Node	Typical Voltage	Node Component
1	≤ ± 10 μV	C10
2	≤ ± 10 μV	R109
3	≤ ± 10 μV	C9
4	≤ ± 10 μV	C8
5	≤ ± 10 μV	–
6	≤ ± 10 μV	–
7	≤ ± 10 μV	–
8	≤ ± 10 μV	W1 Shield
9	+ 14 μV	CR215
10	≤ ± 10 μV	R1 Pin 16
11	≤ ± 10 μV	C35
12	≤ ± 10 μV	C32
13	≤ ± 10 μV	–
14	- 40 μV	PAD
15	- 40 μV	C34
16	- 58 μV	CR15
17	- 36 μV	CR16
18	- 38 μV	CR221
19	+ 74 μV	R53
20	+ 17 μV	–
21	+ 17 μV	–
22	+ 14 μV	C206
23	≤ ± 10 μV	R57
24	≤ ± 10 μV	PAD
25	≤ ± 10 μV	R57
26	≤ ± 10 μV	C207
27	≤ ± 10 μV	C37
28	≤ ± 10 μV	Serial Data Cable Shield
29	≤ ± 10 μV	TP8 Shield
30	≤ ± 10 μV	C208
31	≤ ± 10 μV	C27
32	≤ ± 10 μV	PAD
33	≤ ± 10 μV	PAD
34	≤ ± 10 μV	PAD
35	≤ ± 10 μV	PAD
36	≤ ± 10 μV	PAD
37	≤ ± 10 μV	C31
38	≤ ± 10 μV	C30
39	≤ ± 10 μV	TP3 Shield
40	≤ ± 10 μV	C43
41	≤ ± 10 μV	C42
42	≤ ± 10 μV	C41
43	≤ ± 10 μV	U12 Pin 3
44	≤ ± 10 μV	C39
45	≤ ± 10 μV	R58 Pin 5
46	≤ ± 10 μV	C40
47	≤ ± 10 μV	C29
48	≤ ± 10 μV	R46
49	≤ ± 10 μV	C24
50	+ 28 μV	C44
51	+ 26 μV	C23
52	+ 25 μV	TP2 Shield
53	≤ ± 10 μV	C45
54	≤ ± 10 μV	TP10 Shield
55	≤ ± 10 μV	TP11 Shield
56	≤ ± 10 μV	C46
57	≤ ± 10 μV	R101
58	≤ ± 10 μV	U16 Pin 16
59	≤ ± 10 μV	U16 Pin 1
60	≤ ± 10 μV	U18 Pin 16
61	≤ ± 10 μV	U15 Pin 1
62	≤ ± 10 μV	R73
63	≤ ± 10 μV	R74
64	≤ ± 10 μV	U17 Pin 16
65	≤ ± 10 μV	C33
66	≤ ± 10 μV	C36
67	≤ ± 10 μV	TP9 Shield
68	≤ ± 10 μV	U14 Pin 1
69	≤ ± 10 μV	U14 Pin 3



ANALOG BOARD COMPONENT LOCATOR

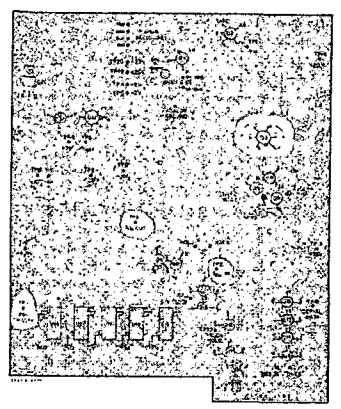


ANALOG BOARD COMPONENT PIN-OUT

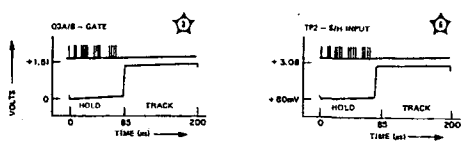


C1

Figure 5-27. Inguard Reference Supplies Troubleshooting Flowchart.



ANALOG BOARD COMPONENT PIN-OUT



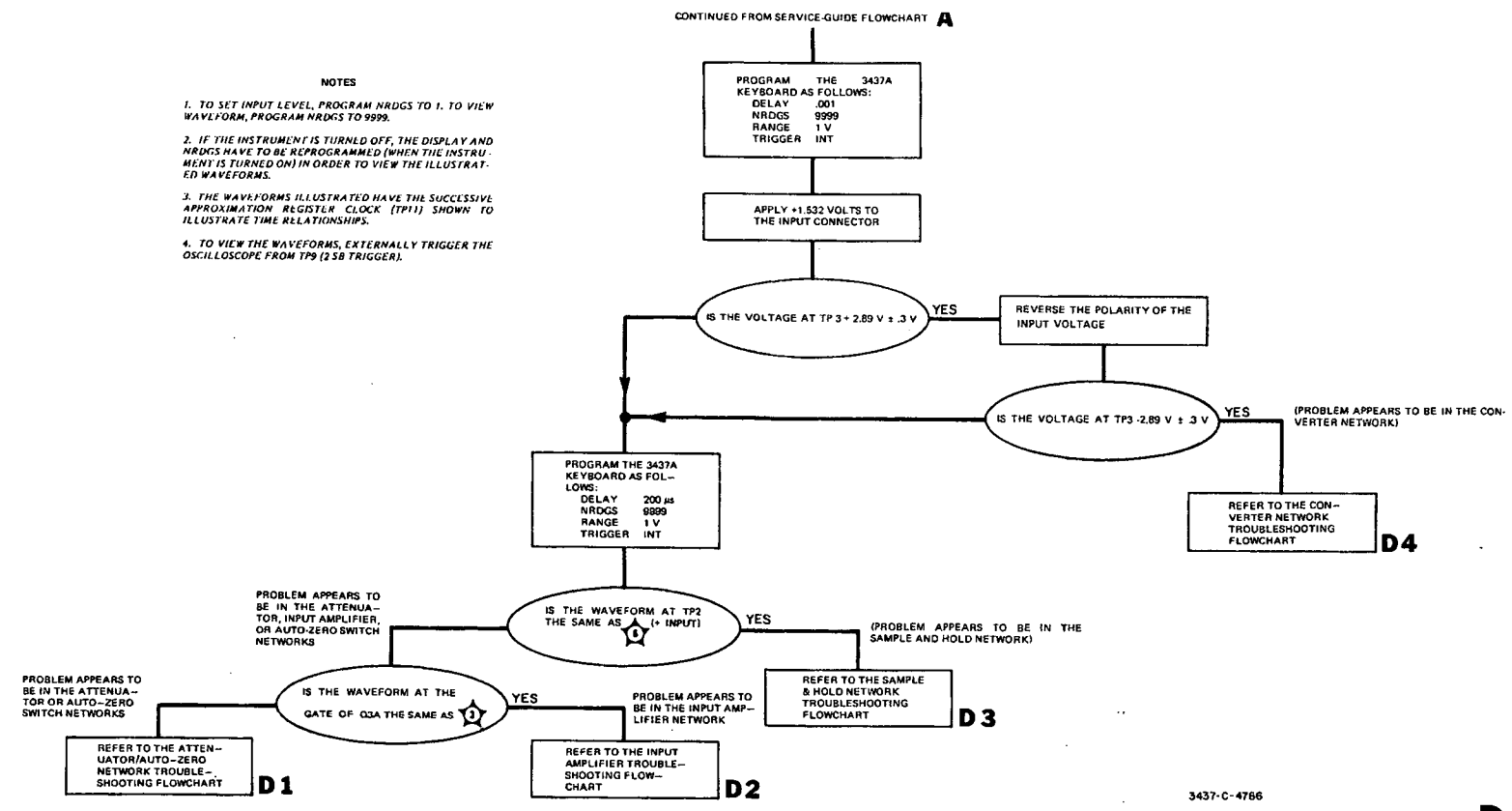
NOTES

1. TO SET INPUT LEVEL, PROGRAM NRDGS TO 1. TO VIEW WAVEFORM, PROGRAM NRDGS TO 9999.

2. IF THE INSTRUMENT IS TURNED OFF, THE DISPLAY AND NRDGS HAVE TO BE REPROGRAMMED (WHEN THE INSTRUMENT IS TURNED ON) IN ORDER TO VIEW THE ILLUSTRATED WAVEFORMS.

3. THE WAVEFORMS ILLUSTRATED HAVE THE SUCCESSIVE APPROXIMATION REGISTER CLOCK (TP11) SHOWN TO ILLUSTRATE TIME RELATIONSHIPS.

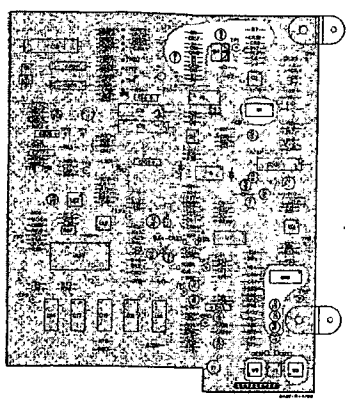
4. TO VIEW THE WAVEFORMS, EXTERNALLY TRIGGER THE OSCILLOSCOPE FROM TP9 (2 SB TRIGGER).



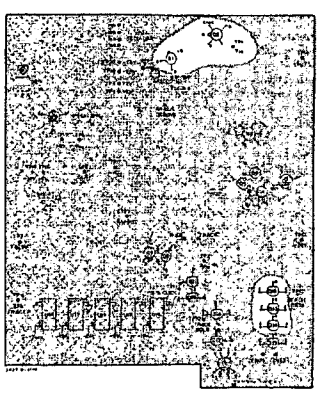
3437-C-4766

D

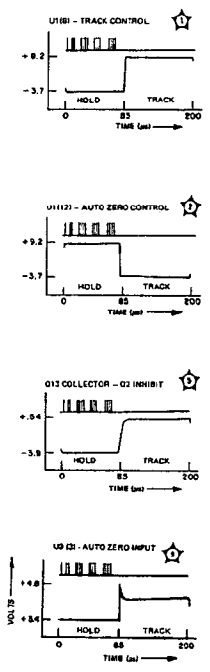
Figure 5-28. Analog Measurement Circuitry Troubleshooting Procedures Flowchart.



ANALOG BOARD COMPONENT LOCATOR



ANALOG BOARD COMPONENT PIN-OUT



NOTES

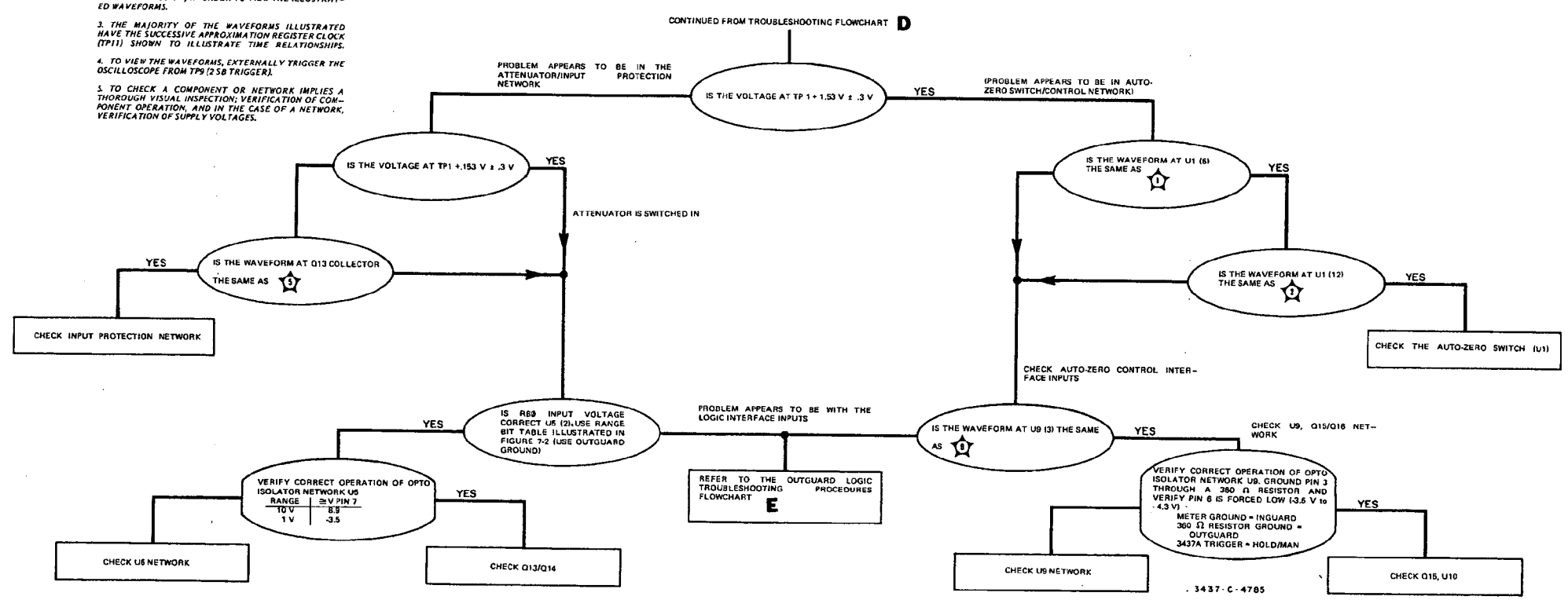
1. *TO SET INPUT LEVEL, PROGRAM NRDGS TO 1. TO VIEW WAVEFORM, PROGRAM NRDGS TO 9999.*

2. *IF THE INSTRUMENT IS TURNED OFF, THE DELAY AND NRDGS HAVE TO BE REPROGRAMMED (WHEN THE INSTRUMENT IS TURNED ON) IN ORDER TO VIEW THE ILLUSTRATED WAVEFORMS.*

3. *THE MAJORITY OF THE WAVEFORMS ILLUSTRATED HAVE THE SUCCESSIVE APPROXIMATION REGISTER CLOCK (TP11) SHOWN TO ILLUSTRATE TIME RELATIONSHIPS.*

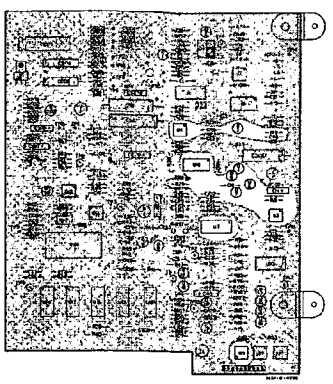
4. *TO VIEW THE WAVEFORMS, EXTERNALLY TRIGGER THE OSCILLOSCOPE FROM TP9 (2.5 B TRIGGER).*

5. *TO CHECK A COMPONENT OR NETWORK IMPLIES A THOROUGH VISUAL INSPECTION; VERIFICATION OF COMPONENT OPERATION, AND IN THE CASE OF A NETWORK, VERIFICATION OF SUPPLY VOLTAGES.*

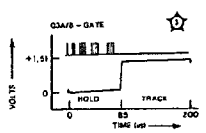


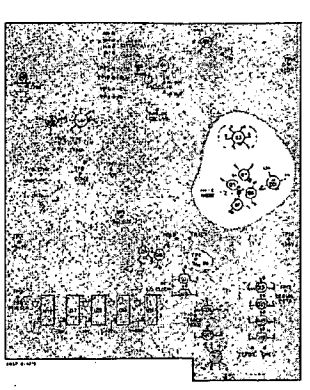
D1

Figure 5-29. Input Attenuator/Auto Zero Network Troubleshooting Flowchart.

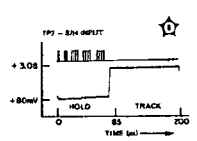


ANALOG BOARD COMPONENT LOCATOR





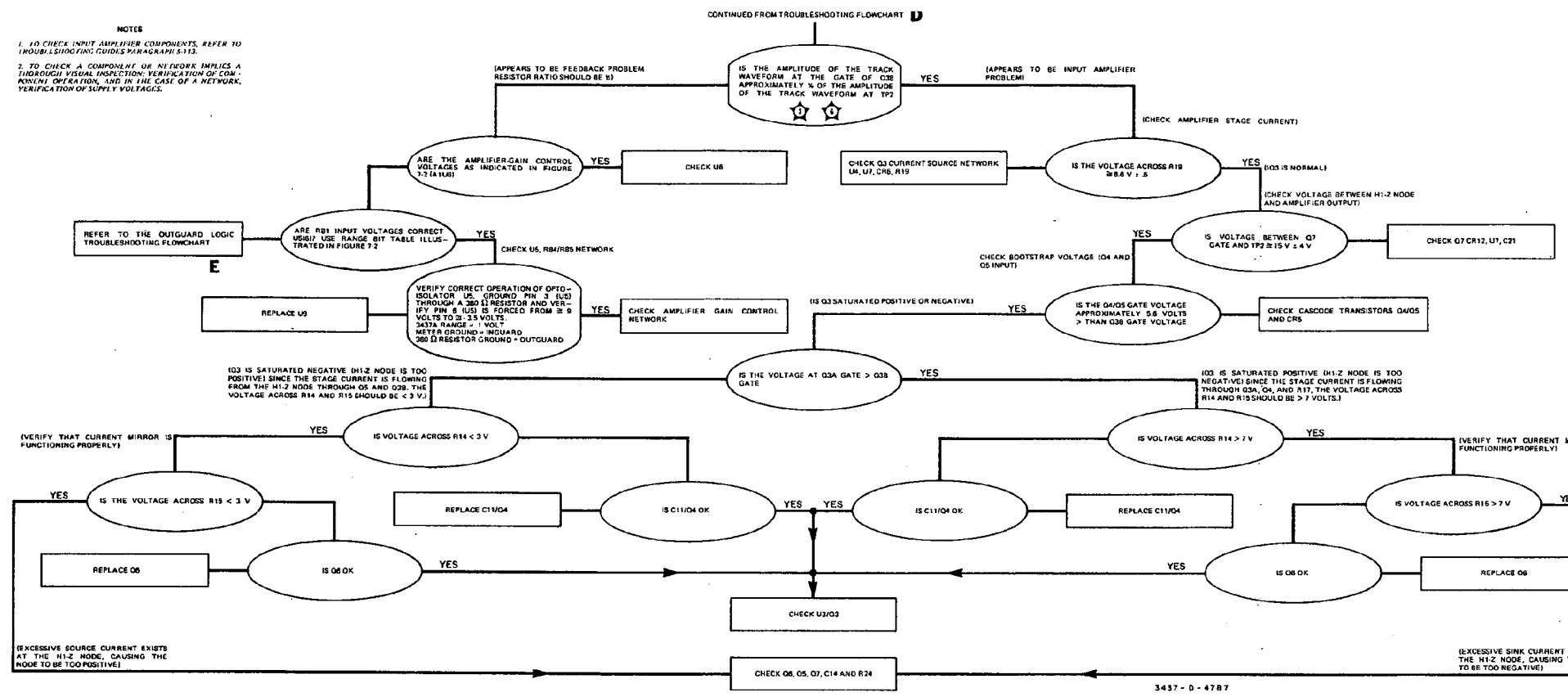
ANALOG BOARD COMPONENT PIN-OUT



NOTES

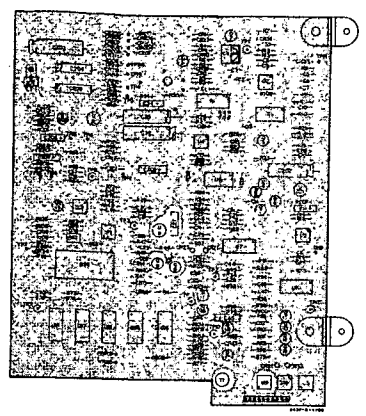
1. TO CHECK INPUT AMPLIFIER COMPONENTS, REFER TO TROUBLESHOOTING GUIDES PARAGRAPH 5-113.

2. TO CHECK A COMPONENT OR NETWORK IMPLIES A THOROUGH VISUAL INSPECTION; VERIFICATION OF COMPONENT OPERATION, AND IN THE CASE OF A NETWORK, VERIFICATION OF SUPPLY VOLTAGES.

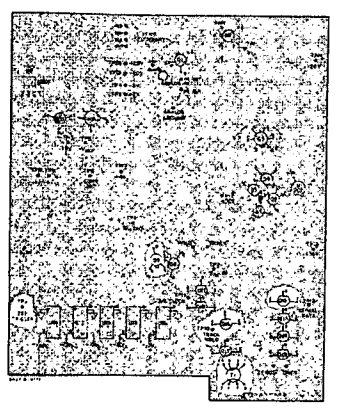


D2

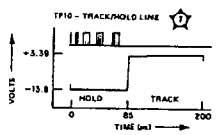
Figure 5-30. Input Amplifier Troubleshooting Flowchart.

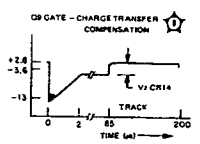


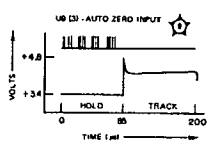
ANALOG BOARD COMPONENT LOCATOR

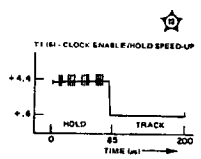


ANALOG BOARD COMPONENT PIN-OUT









NOTES

1. TO SET INPUT LEVEL, PROGRAM NRDGS TO 1. TO VIEW WAVEFORM, PROGRAM NRDGS TO 9999.

2. IF THE INSTRUMENT IS TURNED OFF, THE DELAY AND NRDGS HAVE TO BE REPROGRAMMED (WHEN THE INSTRUMENT IS TURNED ON) IN ORDER TO VIEW THE ILLUSTRATED WAVEFORMS.

3. THE MAJORITY OF THE WAVEFORMS ILLUSTRATED HAVE THE SUCCESSIVE APPROXIMATION REGISTER CLOCK (TP11) SHOWN TO ILLUSTRATE TIME RELATIONSHIPS.

4. TO VIEW THE WAVEFORMS, EXTERNALLY TRIGGER THE OSCILLOSCOPE FROM TP9 (2 SB TRIGGER).

5. TO CHECK A COMPONENT OR NETWORK IMPLIES A THOROUGH VISUAL INSPECTION; VERIFICATION OF COMPONENT OPERATION, AND IN THE CASE OF A NETWORK, VERIFICATION OF SUPPLY VOLTAGES.

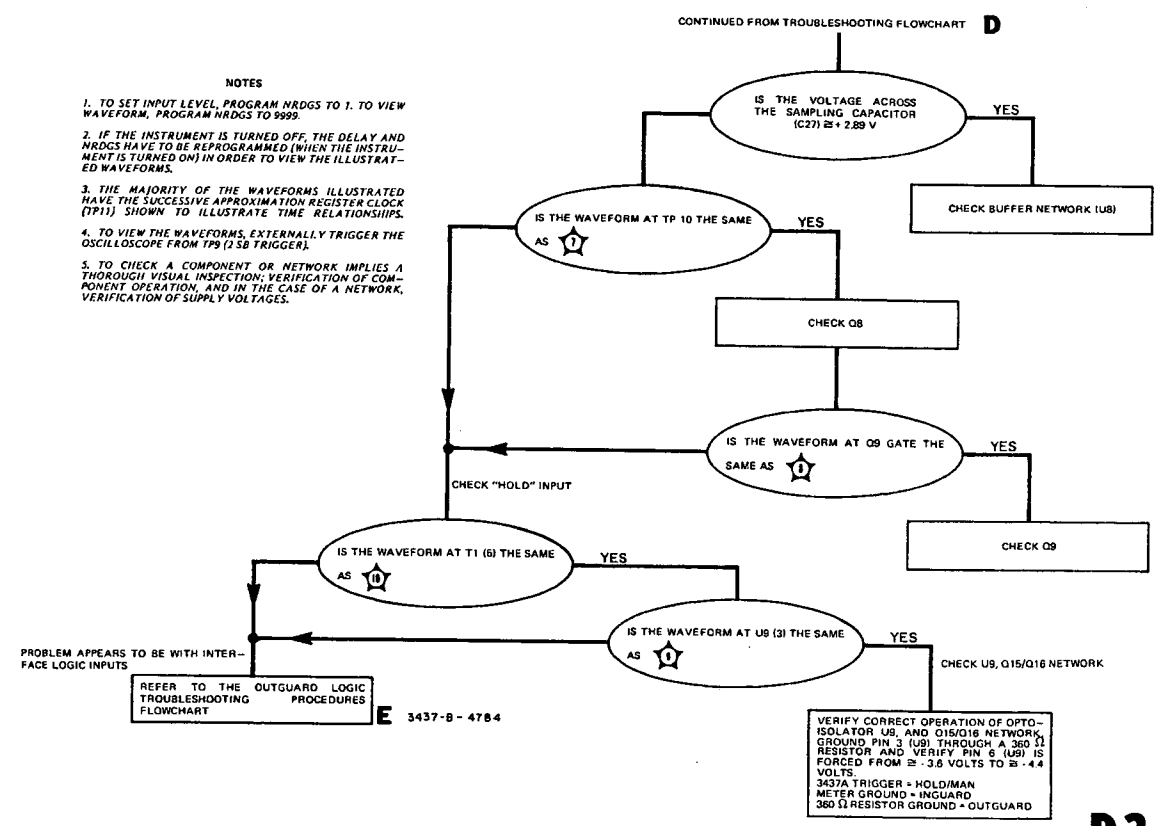
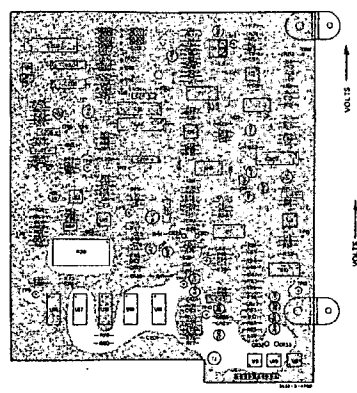
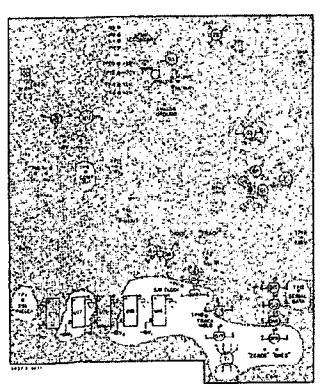


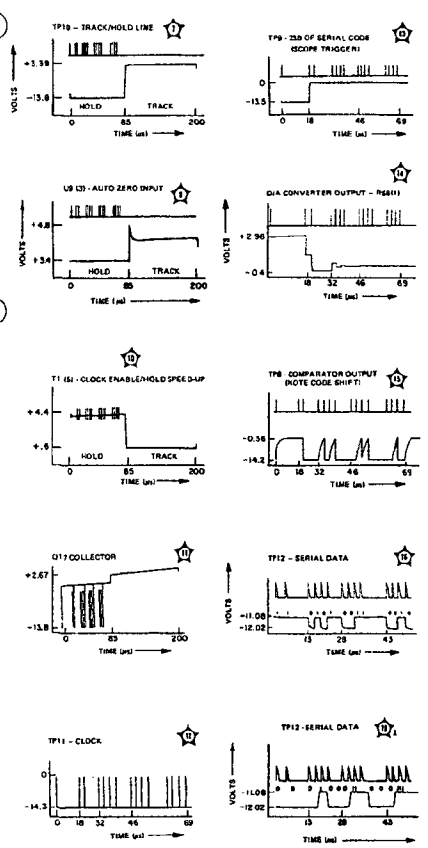
Figure 5-31. Sample and Hold Network Troubleshooting Flowchart.



ANALOG BOARD COMPONENT LOCATOR



ANALOG BOARD COMPONENT PIN-OUT



NOTES

1. *TO SET INPUT LEVEL, PROGRAM NRDGS TO 1. TO VIEW WAVEFORM, PROGRAM NRDGS TO 9999.*

2. *IF THE INSTRUMENT IS TURNED OFF, THE DELAY AND NRDGS HAVE TO BE REPROGRAMMED (WHEN THE INSTRUMENT IS TURNED ON) IN ORDER TO VIEW THE ILLUSTRATED WAVEFORMS.*

3. *THE MAJORITY OF THE WAVEFORMS ILLUSTRATED HAVE THE SUCCESSIVE APPROXIMATION REGISTER CLOCK (TP11) SHOWN TO ILLUSTRATE TIME RELATIONSHIPS.*

4. *TO VIEW THE WAVEFORMS, EXTERNALLY TRIGGER THE OSCILLOSCOPE FROM TP9 (2 SB TRIGGER).*

5. *TO CHECK A COMPONENT OR NETWORK IMPLIES A THOROUGH VISUAL INSPECTION; VERIFICATION OF COMPONENT OPERATION, AND IN THE CASE OF A NETWORK, VERIFICATION OF SUPPLY VOLTAGES.*

6. *TO CHECK CONVERTER COMPONENTS, REFER TO TROUBLESHOOTING GUIDES PARAGRAPH 5-123.*

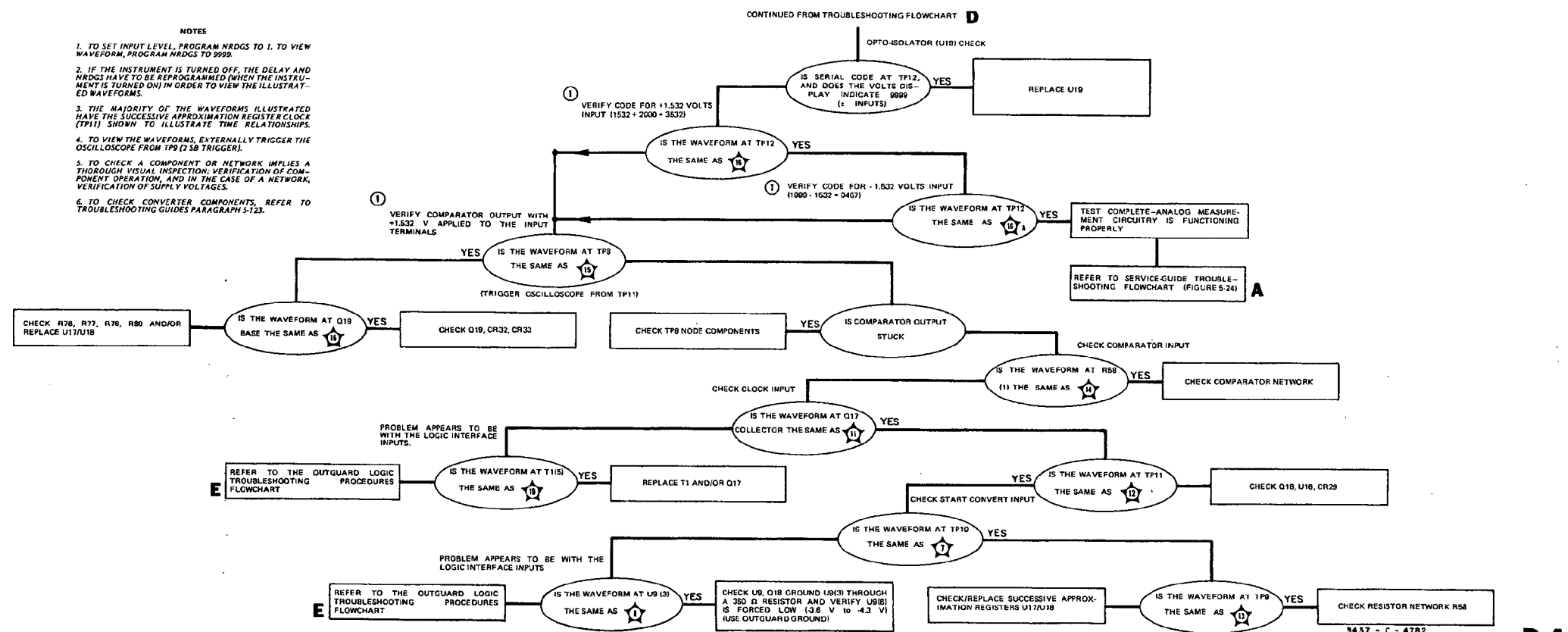


Figure 5-32. Analog/Digital Converter Network Troubleshooting Flowchart.

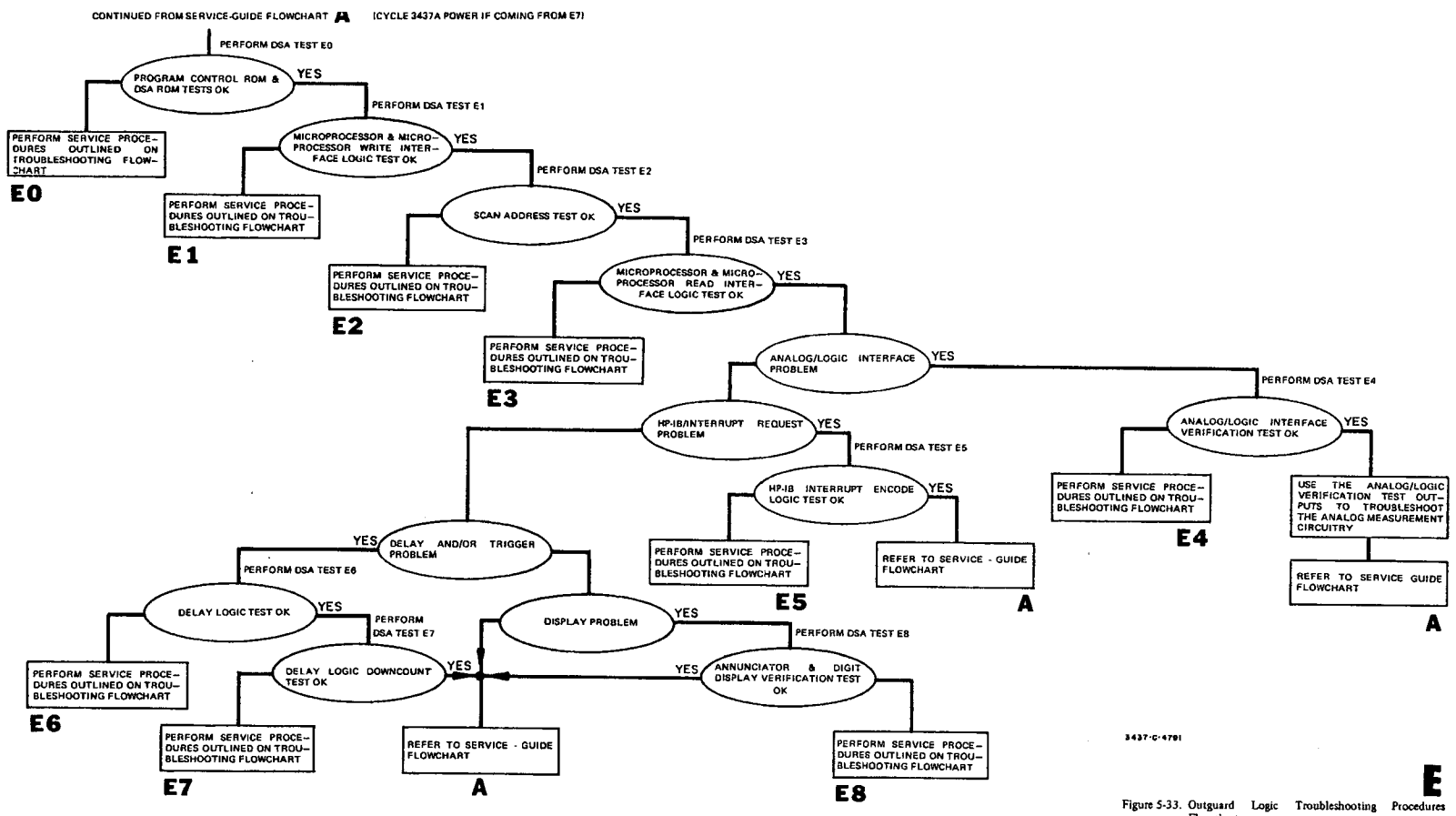
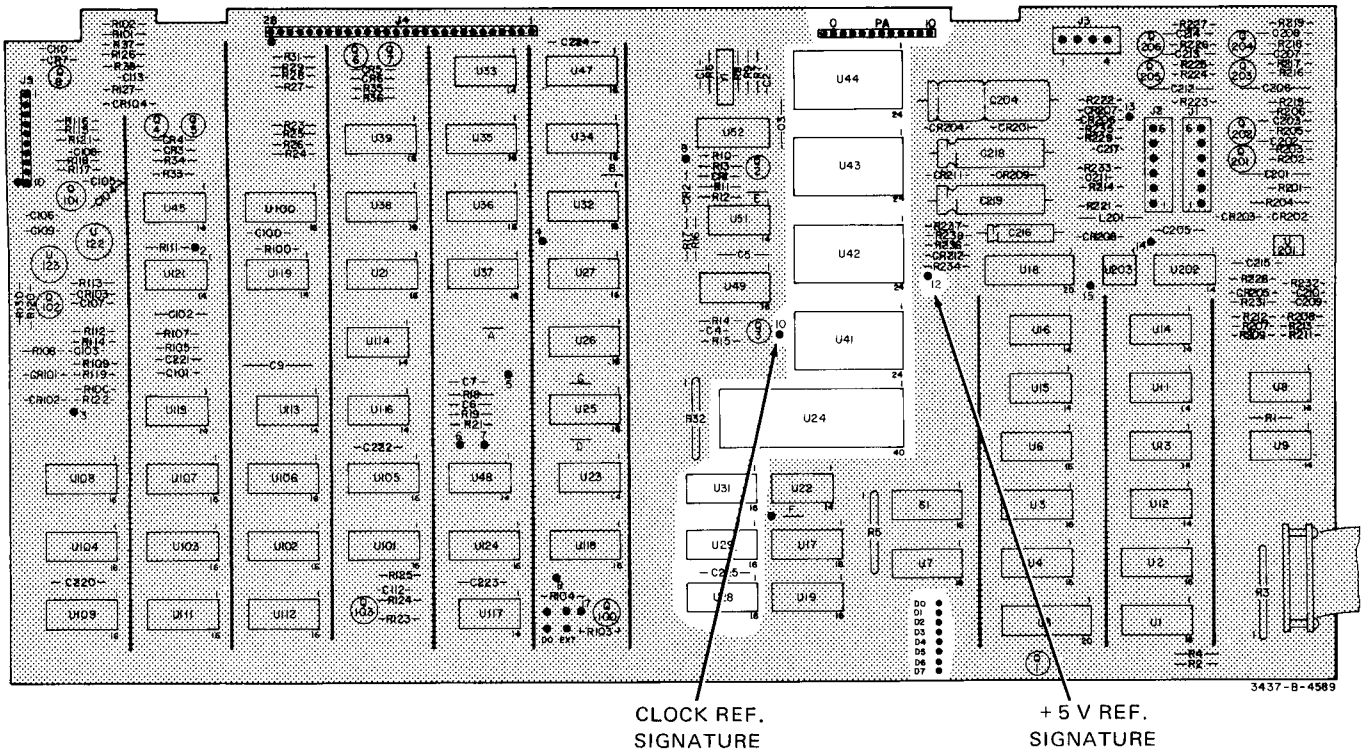


Figure 5-33. Outguard Logic Troubleshooting Procedures Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2", "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/ I Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

1

Test Point	Signature
D0	7HH1
D1	9F63
D2	67PU
D3	P7F0
D4	99H5
D5	947F
D6	F487
D7	2535

2

Test Point	Signature
PA0	2A1F
PA1	A206
PA2	C133
PA3	8F3U
PA4	331P
PA5	7C47
PA6	C25F
PA7	5H21
PA8	19H6
PA9	HP66
PA10	U81P

3

U41	Signature
9	HH6A
10	AFPF
11	U75C
13	A95C
14	3F2H
15	FFU8
16	5055
17	60PH

4

U41	Signature
1	2946
2	F61C
3	0106
4	3A9A
5	H10F
6	HH53
7	0863
8	29PP
18	8P54
19	8P54
20	0000
21	0000
23	4596
24	8P54

5

U42	Signature
9	1P23
10	HP98
11	62PP
13	HHFU
14	C830
15	1A3U
16	P870
17	2U4F

6

U42	Signature
1	9835
2	0772
3	4U2A
4	4442
5	P030
6	H0AA
7	HA07
8	C21A
12	0000
18	7A70
19	8P54
20	0000
21	0000
23	1734
24	7A70

7

U43	Signature
9	C4AU
10	CU0P
11	69HA
13	FF02
14	51P4
15	2CFP
16	FC26
17	23F8

8

U43	Signature
1	2946
2	F61C
3	0106
4	3A9A
5	H10F
6	HH53
7	0863
8	29PP
12	0000
18	8P54
19	8P54
20	0000
21	0000
23	4596
24	8P54

9

U44	Signature
9	1H91
10	67C7
11	1825
13	C2H7
14	17A4
15	3AUP
16	HU21
17	F956

10

U44	Signature
1	9835
2	0772
3	4U2A
4	4442
5	P030
6	H0AA
7	HA07
8	C21A
12	0000
18	7A70
19	8P54
20	0000
21	0000
23	1734
24	7A70

20

DSA ROM	Signature
9	6AU4
10	A5U2
11	135A
13	6P4B
14	F06P
15	9CF3
16	AA66
17	A36B

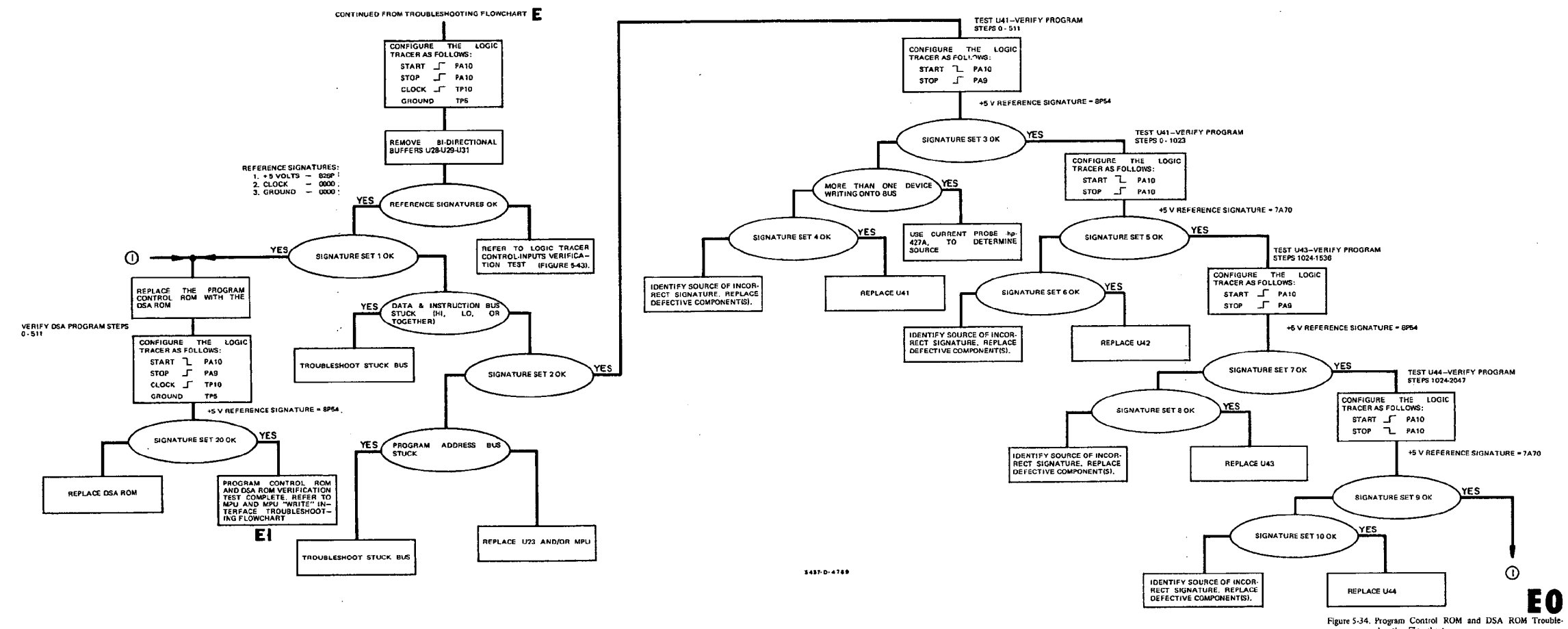
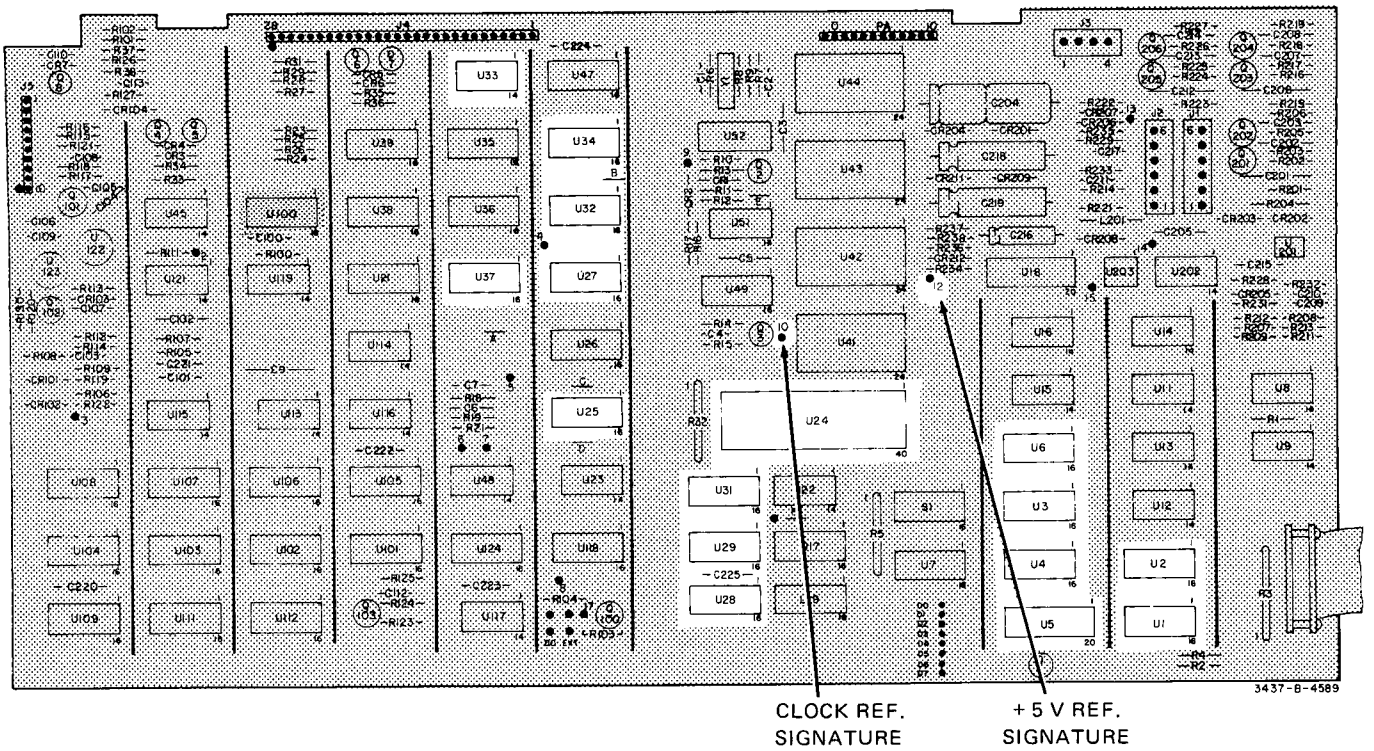


Figure 5-34. Program Control ROM and DSA ROM Troubleshooting Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/ Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

30

U27	Signature
7	5377
9	1SAF
10	6U29
11	8857
12	U188
13	H901
14	P949
15	AP28

31

MPU	Signature
12	3479
13	APA6
14	6C51
15	884H

32

U27	Signature
1	884H
2	6C51
3	APA6
4	3479
5	0000
6	UP34

33

U25	Signature
7	6994
9	8857
10	PC02
11	0502
12	CH02
13	5H02
14	P5P5
15	3P9U

34

U25	Signature
1	884H
2	6C51
3	APA6
4	0000
5	0000
6	3479

35

MPU	Signature
32	5FH0
33	FH05
34	H059
35	0594
36	0000
37	94CU

36

U34	Signature
3	HC16
6	1039
10	45H6
13	HA82

37

MPU	Signature
18	3F85
19	2088
20	4A9U
21	3C53
22	AH91
23	6PH7
24	53H3
25	P790

38

U32	Signature
1	2088
4	P5P5
5	3P9U
9	3C53
10	4A9U
11	5377
15	3F85

39

U37	Signature
3	274F
6	7C95
9	U188
11	C5PP
14	5U1H

40

U33	Signature
3	269H
6	HPC4
8	35FH
11	UC15

41

U6	Signature
2	7089
5	5280
7	HPF5
9	P949
10	60C1
12	0CA0
15	P1P8

42

U8	Signature
3	3C53
4	6PH7
6	AH91
11	4A9U
13	2088
14	3F85

43

U3	Signature
12	H879
14	4AC8
U4	———
2	P22A
4	4H67
6	FUCA
10	F34A
12	5ABH
14	F4PU

44

U5	Signature
3	3C53
4	4A9U
7	2088
8	3F85
13	P790
14	53H3
17	6PH7
18	AH91

45

U1	Signature
2	H2HA
7	4C1H
9	F2PU
15	502P
U2	———
2	F530
7	6A7H
9	47PH
15	4FC8

46

U5	Signature
2	FUCA
5	F4PU
6	4H67
9	P22A
12	H879
15	4AC8
16	5ABH
19	F34A

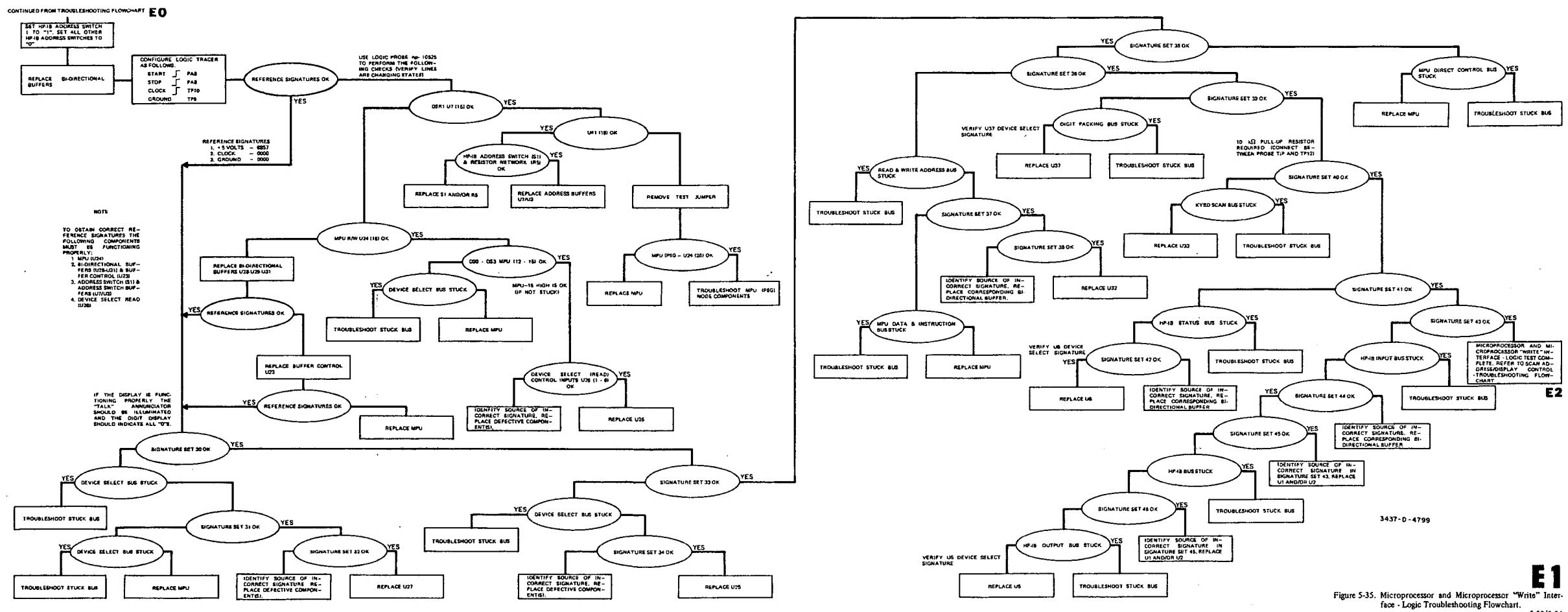
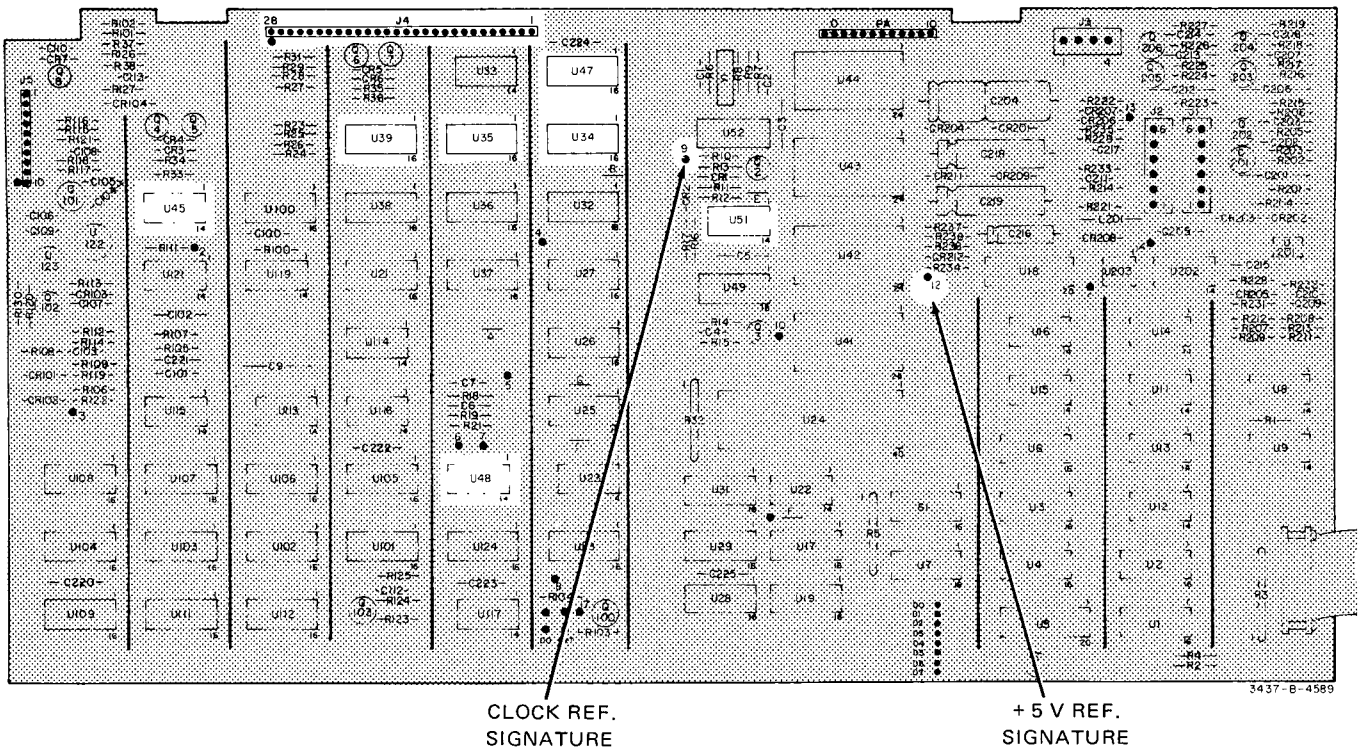


Figure 5-35. Microprocessor and Microprocessor "Write" Interface - Logic Troubleshooting Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/ Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

50

U47	Signature
1	3UP3
7	1674
9	263C
15	3817

51

U48	Signature
1	0000
3	3U9F

52

U34	Signature
4	3UP3
7	3817
9	263C
12	1674

53

U35	Signature
3	3U9F
6	3UP3
7	007U
9	3UP3
11	3UP3

54

U39	Signature
3	3U9F
5	3UP3
7	007U
9	3UP3
11	007U

55

U45	Signature
1	3UP3
4	007U
10	3UP3
13	007U

56

J4	Signature
16	007U
17	3UP3
18	007U
19	3UP3

57

A3A1U1	Signature
1	0000
2	3UP3
3	0000
4	3UP3
5	3UP3
6	3UP3
7	0000
9	3U9F

NOTE

IF THE ANNUNCIATOR AND DIGIT DISPLAY (DSA TEST E-2) CORRESPONDS TO THE CONTENTS OF NOTE 2 (PREVIOUS PAGE), THE ANNUNCIATOR AND DIGIT DISPLAY VERIFICATION TEST (DSA TEST E-8) CAN BE PERFORMED IN LIEU OF THE SCAN ADDRESS/DISPLAY CONTROL TEST. A SUCCESSFUL TEST E-8 VERIFIES THAT THOSE COMPONENTS CHECKED IN TEST E-2 ARE FUNCTIONING PROPERLY.

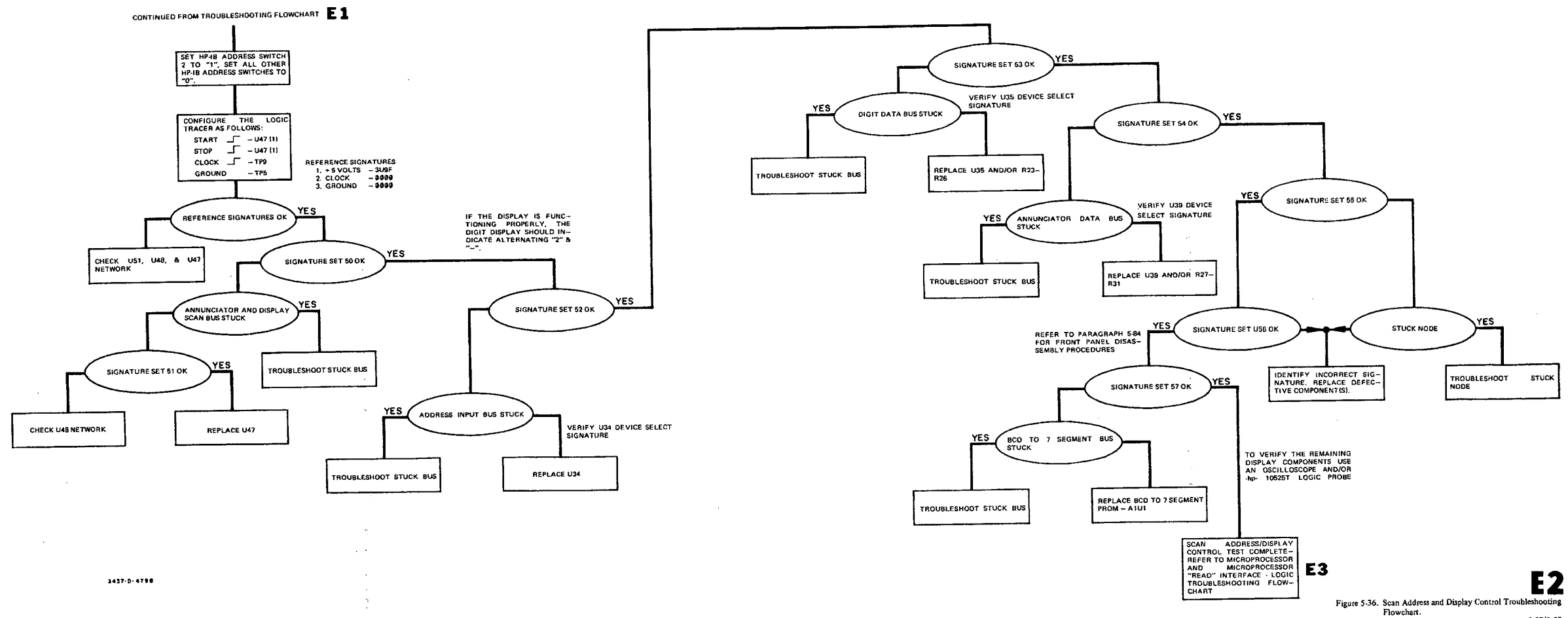
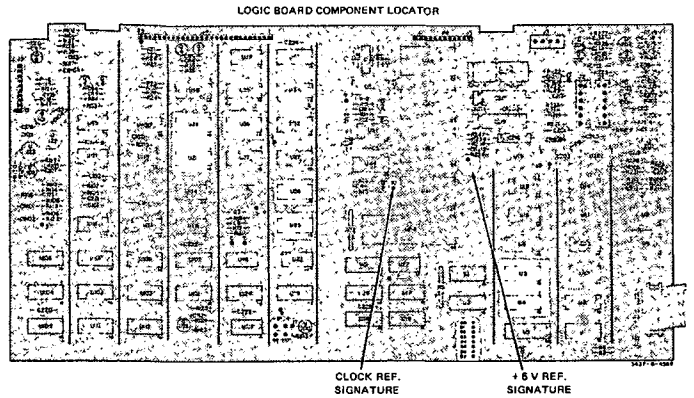


Figure 5-36. Scan Address and Display Control Troubleshooting Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0.9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

60

Test Point	Signature
D0	F104
D1	3C52
D2	1U61
D3	UC3H
D4	26FC
D5	8876
D6	0469
D7	4141

61

U26	Signature
7	0P31
9	5CC6
10	5CA2
12	P164
13	5CU2
14	0001

62

U26	Signature
1	9421
2	UH4P
3	C299
4	AH63
5	FF0C
6	5CC2
U25	——
7	H5HA

63

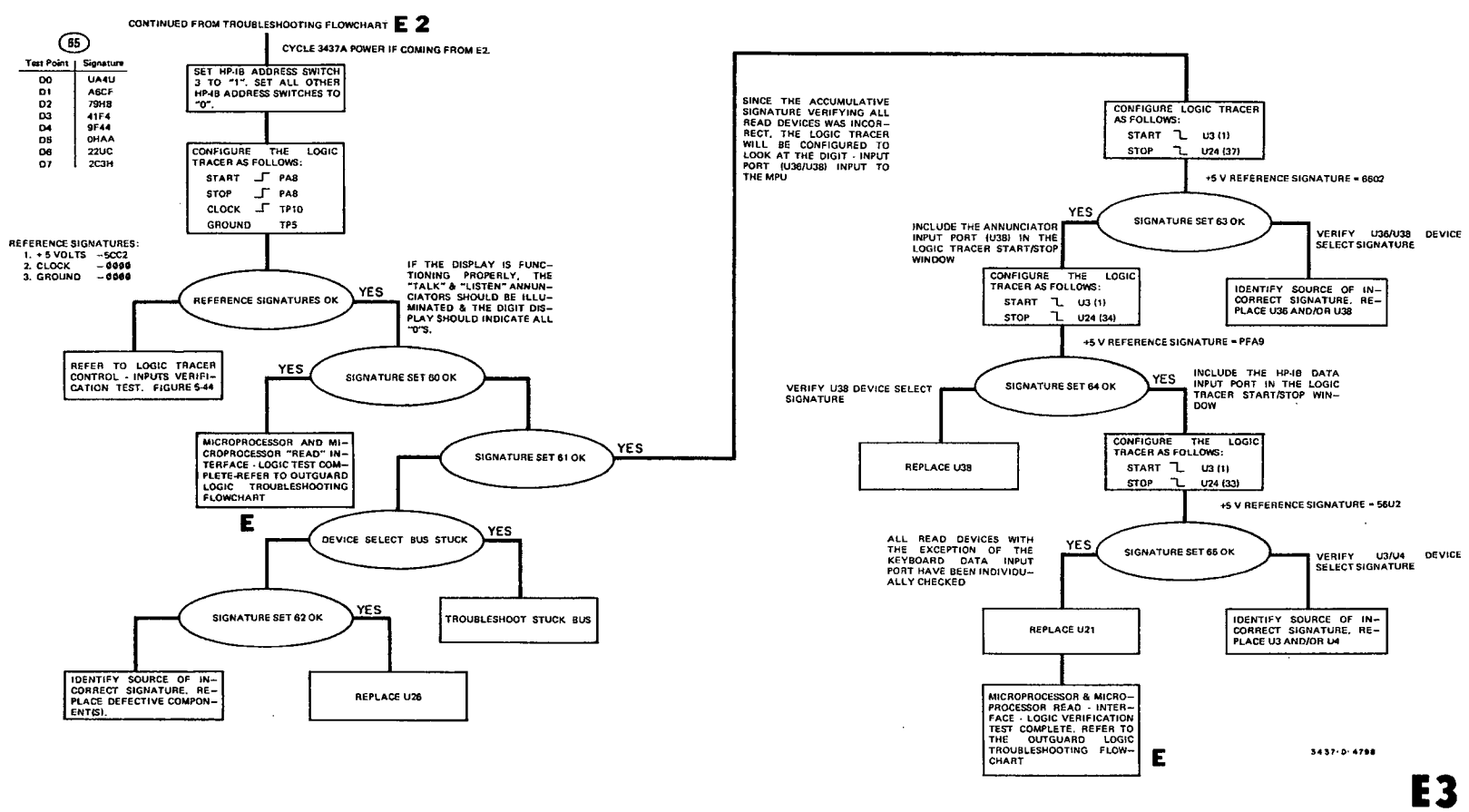
Test Point	Signature
D0	911H
D1	3FU6
D2	PF37
D3	659A
D4	98P3
D5	5444
D6	C84U
D7	C9F9

64

Test Point	Signature
D0	8A9A
D1	4383
D2	UC41
D3	0703
D4	C80P
D5	4785
D6	PC0U
D7	8420

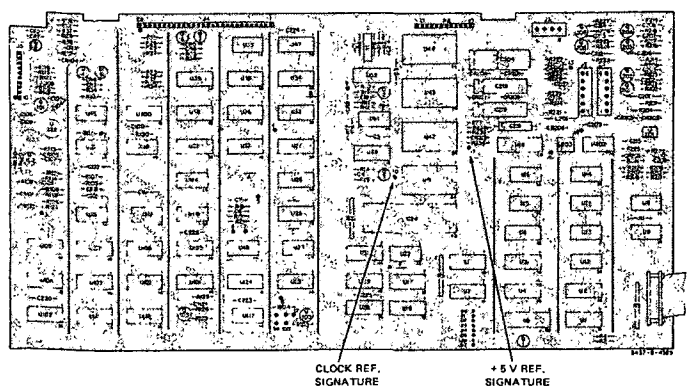
65

Test Point	Signature
D0	UA4U
D1	A6CF
D2	79H8
D3	41F4
D4	9F44
D5	0HAA
D6	22UC
D7	2C3H



E3

Figure 5-37. Microprocessor and Microprocessor "Read" Interface - Logic Troubleshooting Flowchart.



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"'s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay NRDGS Hold Man Packed=ON All Others = OFF
3	"0"'s	Talk & Listen = ON All Others = Low Intensity
4	"4"'s	ON
5	"5"'s	ON
6	"6"'s	ON
7	"7"'s	ON
8	Alternating "–", ".", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an hp- current tracer -hp- 547A to trace the stuck node current.

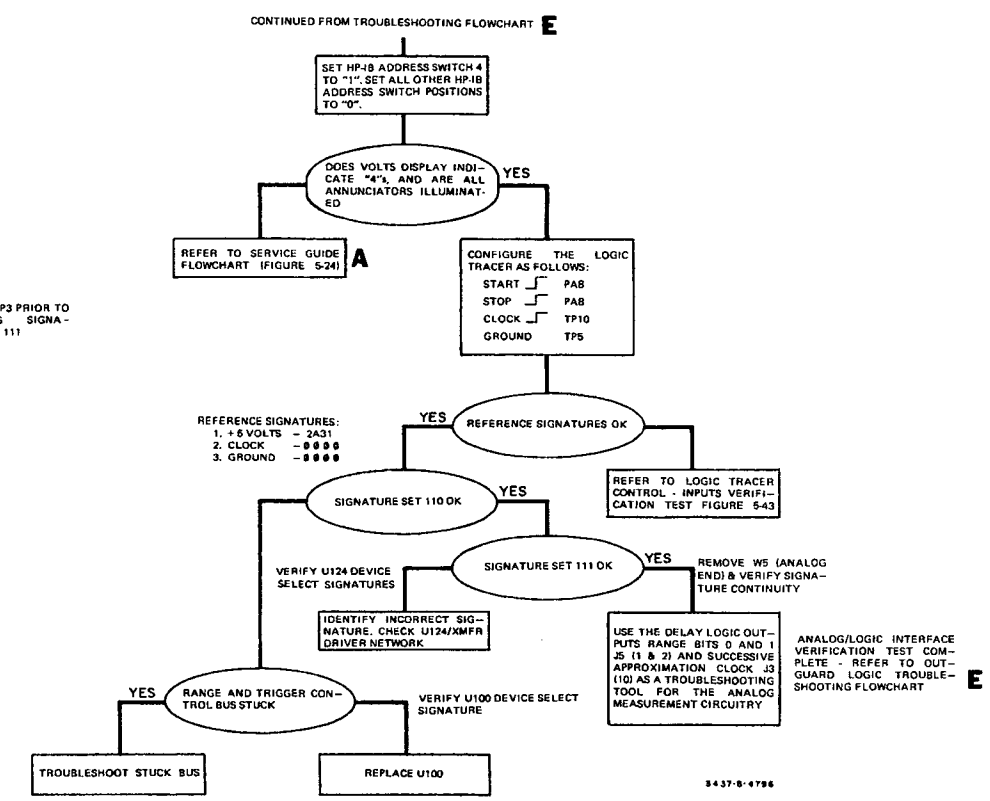
Rev. A

(110)

U100	Signature
3	HH84
6	6293

(111) GROUND TP3 PRIOR TO VERIFYING SIGNATURE SET 111

U124	Signature
1	0000
2	0000
3	2A31
4	2A71
5	2CC2
6	0183
7	2A31
8	0000
10	2A31
11	2CC2
12	0000
13	0000
14	2A21
15	2C33
U117	——
4	2A31
5	2CC2
6	0183
J5	——
7	0183
10	2CC2

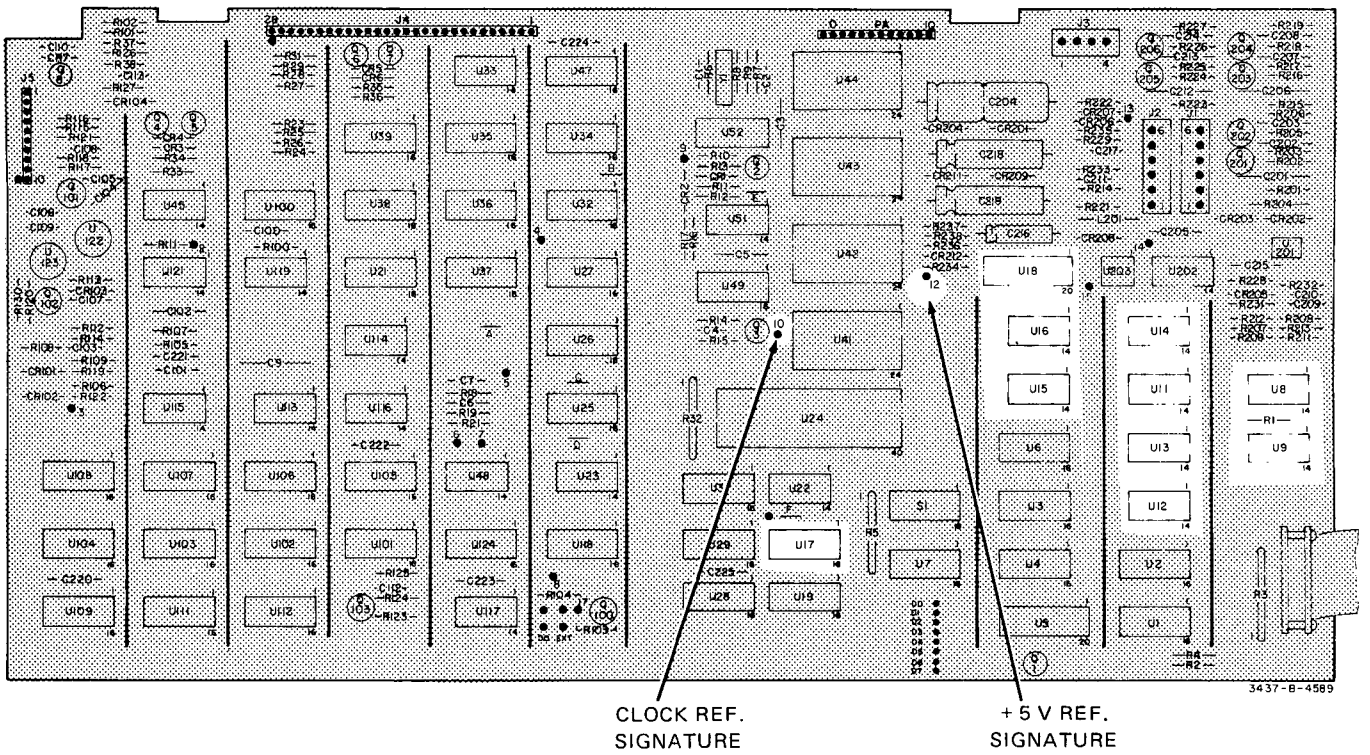


E4

Figure 5-38. Analog/Logic Interface - Logic Troubleshooting Flowchart.

Rev. A 5-61/5-62

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/ Man Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

70

U8	Signature
1	0FH1
2	11P9
3	F603
4	HC3F
5	CH35
6	A00A
8	11P9
9	0FH1
10	05A6
11	1899
12	7P0H
13	6332

71

U9	Signature
1	10U5
2	C86F
3	1899
4	112P
5	HC3F
6	F603
8	CH35
9	AF1C
10	112P
11	0FH1
12	10U5
13	F51C

72

U11	Signature
1	A00A
2	CH35
3	7P0H
4	6332
5	F3A2
6	HP9H
10	1899
11	05A6
12	0FH1
13	11P9
J13	——
8	10U5
9	0HFA
10	6332

73

U12	Signature
3	0F11
4	112P
5	721F
6	6U23
8	058F
9	1553
10	F51C
11	H824
12	AF1C
13	C124
U13	——
11	0F11
12	6332
13	6U23

74

U13	Signature
1	0FH1
2	F400
3	FBH1
4	H93U
5	H9A0
6	F400
U14	——
4	0HFA
5	721F
8	F9FA

75

U15	Signature
6	CHAU
8	5H89
9	2P80

76

U16	Signature
5	F603
8	CHP3

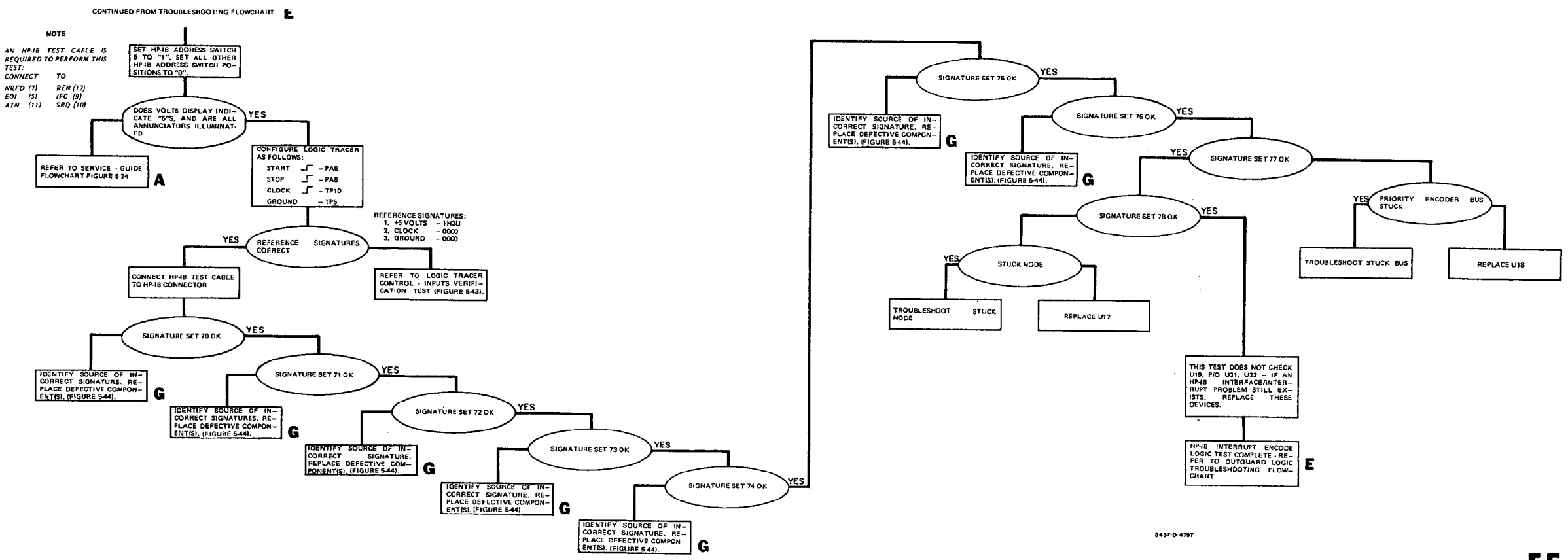
77

U18	Signature
2	78U1
9	UFP7
12	H567
15	1UNF
19	7GA1

REMOVE HP-IB TEST CABLE BEFORE VERIFYING SIGNATURE (U18 (12).

78

U17	Signature
6	0000
7	9179
9	632H or 9A61

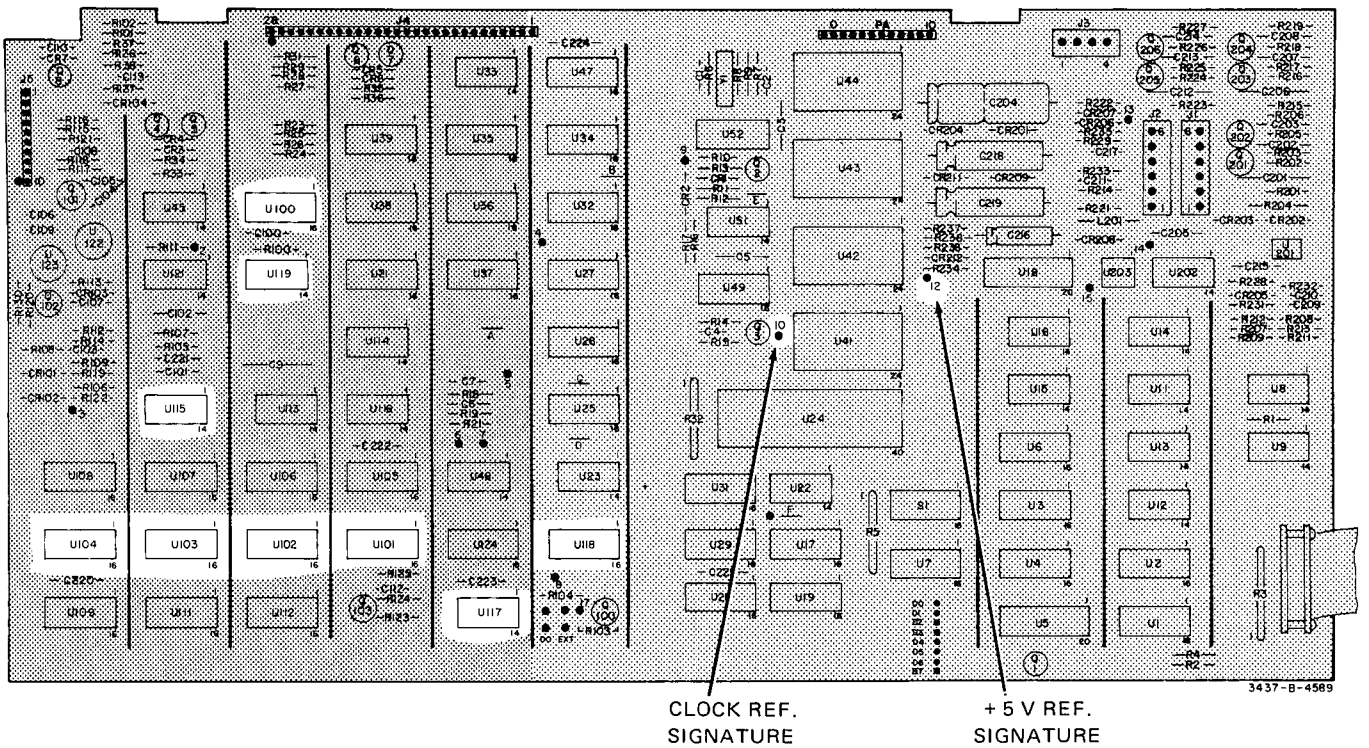


Rev. A

E5

Figure 5-39. HP-IB Interrupt Encode-Logic Troubleshooting Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

80

U100	Signature
3	1631
6	A910
9	4257
11	735P
14	FPC0
15	1203

81

U117	Signature
8	AUPH
9	735P
10	HFC3
U118	——
8	53H4
10	8U67
11	3C0A
12	AUPH
13	HFC3
14	HFC3
15	255H

82

U117	Signature
1	255H
2	53H4
3	7689
U118	——
1	02F8
2	7689
3	HFC3
4	AUPH
5	0000
6	HFC3
7	CP7C

83

U115	Signature
8	56P5
9	0000

84

U101	Signature
4	900H
5	4003
6	38C7
7	64C3
9	2A34
10	6060
11	11F5
14	3572

85

U102	Signature
4	979A
5	9C98
6	PA5H
7	U043
9	9FA8
10	0060
11	0C4H
14	3572

86

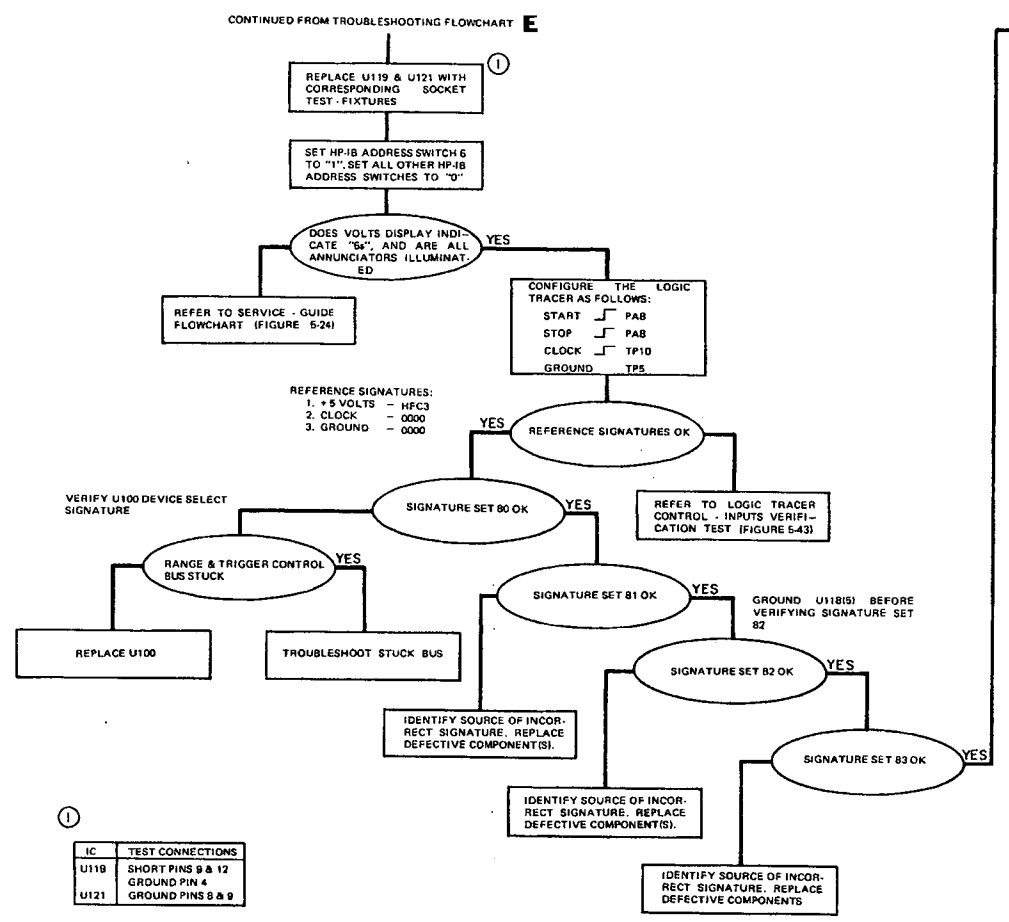
U103	Signature
4	H637
5	1A32
6	45AA
7	68H9
9	4H01
10	PF1F
11	3CC1
14	3572

87

U104	Signature
4	PU01
5	3A9A
6	072U
7	534B
9	A51D
10	44P6
11	PUCC
14	3572

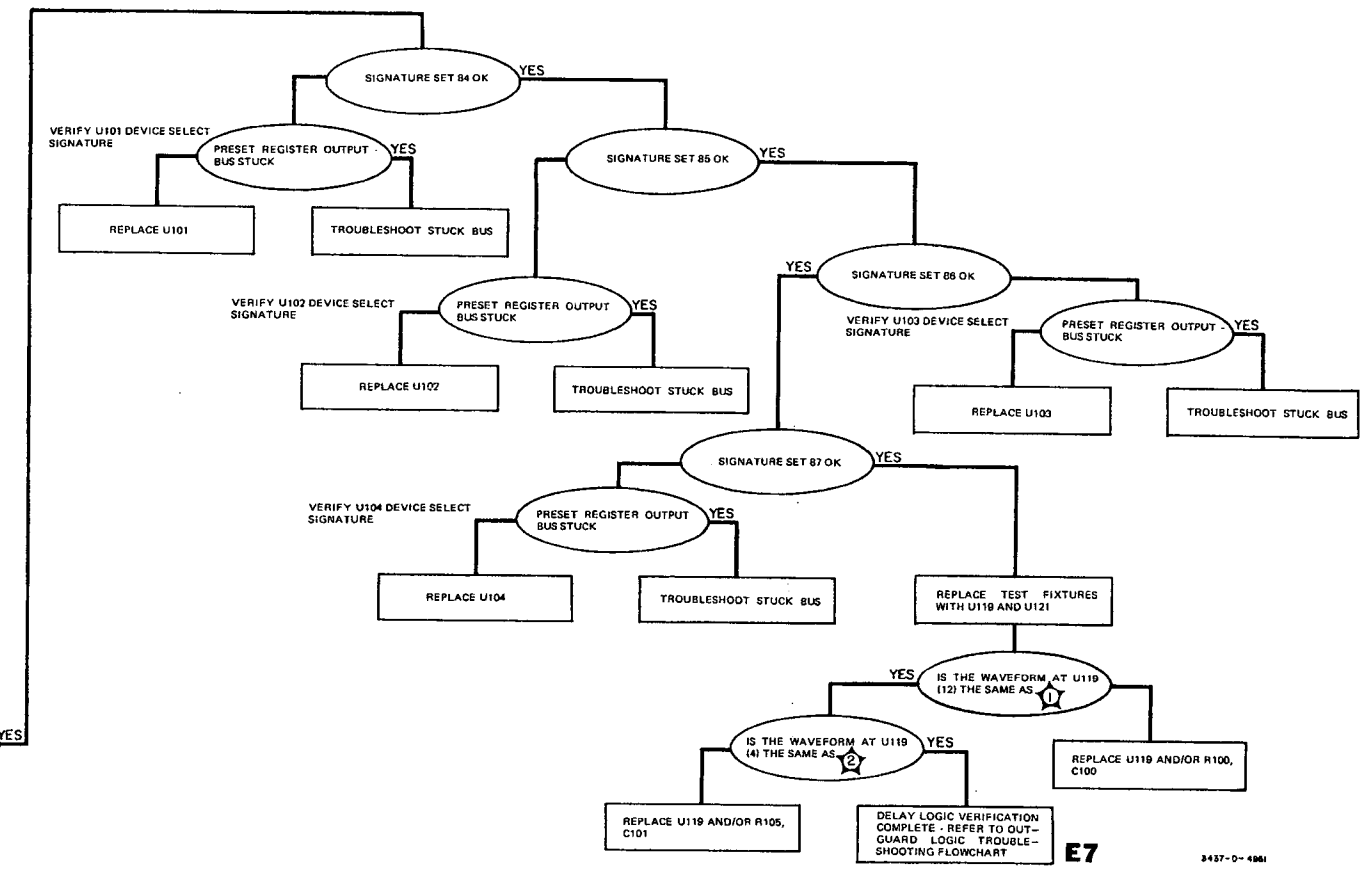
1 — 4V, 0, 130 µs (Typical)

2 — 4V, 0, 100 ns (Typical)



1

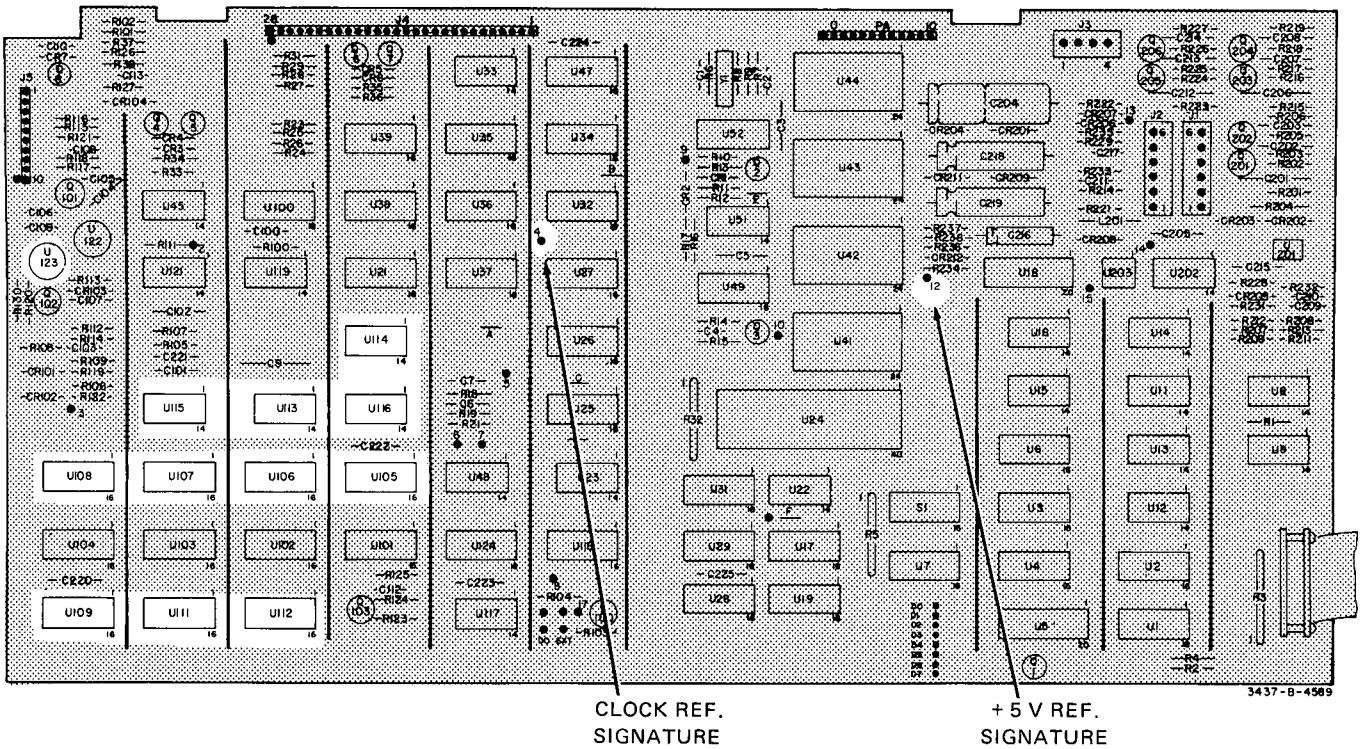
IC	TEST CONNECTIONS
U119	SHORT PINS 9 & 12
	GROUND PIN 4
U121	GROUND PINS 8 & 9



E6

Figure 5-40. Delay Logic Troubleshooting Flowchart.

LOGIC BOARD COMPONENT LOCATOR



NOTES

1. Perform the outguard logic troubleshooting tests in the order indicated. Service procedures (outlined in the troubleshooting flowcharts) are based upon results of previous tests.

2. Each DSA test is identified by a particular front panel display. The following table identifies each DSA test and corresponding front panel display.

DSA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2	Alternated "2" "–"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Delay, NRDGS Hold/ Man, Packed=ON All Others = OFF
3	"0"s	Talk & Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7	"7"s	ON
8	Alternating "–", "·", "0-9"	ON

3. If an incorrect signature is obtained, perform the following steps prior to replacing a component(s):

a. Verify that the logic tracer is configured as stated in the troubleshooting flowchart.

b. Verify that the reference signatures are correct.

c. Verify (if possible) that the front panel display corresponds to the DSA test selected.

d. Perform a thorough visual and mechanical inspection of the circuit board signature path (open, short, solder splash, etc). Review the circuit diagrams identifying the location of the test signature sets (Figures 5-44, 5-45 and 5-46).

e. Verify that the component(s) have the correct supply voltages, and that the required device select signatures are correct.

4. To troubleshoot a stuck-node (stuck implies that a node is held "high" or "low" or that two or more lines of a bus are connected together):

a. Perform a thorough visual and mechanical inspection of the circuit board (open, short, solder splash etc).

b. Use an -hp- current tracer -hp- 547A to trace the stuck node current.

90

U105	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

91

U106	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

92

U107	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

93

U108	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

94

U109	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

95

U111	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

96

U112	Signature
2	0066
3	0157
4	0000
5	03U9
6	0078
7	0183
11	03U9
12	0205
14	0000

97

U113	Signature
2	3HF0
8	FF65
10	3HF0

98

U116	Signature
1	FF65
2	0000
3	9AHP
4	0000
5	AU63
6	81F8
8	AU63
9	FF65
10	0000
11	PC40
12	9AHP
13	025H

99

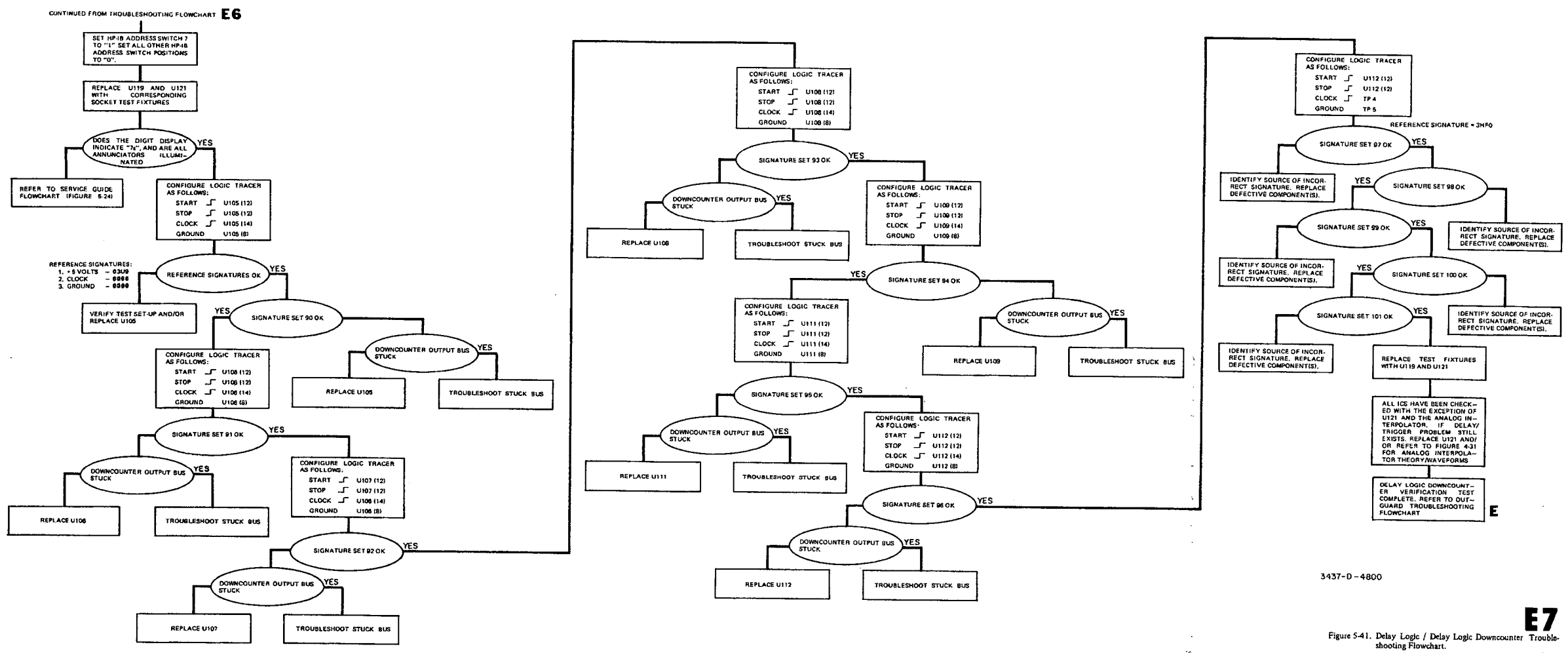
U114	Signature
1	CUHU
2	UHU1
3	7UPP
4	0000
5	3HF0
6	0000
8	0000
9	81F8
10	CF09
11	0000
12	FF65
13	U1A5

100

U115	Signature
2	3HF0
3	0000
4	U1A5
5	H117
6	C475

101

U123	Signature
1	0000
2	C476
3	3HF0
4	3HF0
5	0000
6	3HF0
7	0000
8	0000
9	C475
10	3HF0
TP3	C475



E7

Figure 5-41. Delay Logic / Delay Logic Downcounter Troubleshooting Flowchart.

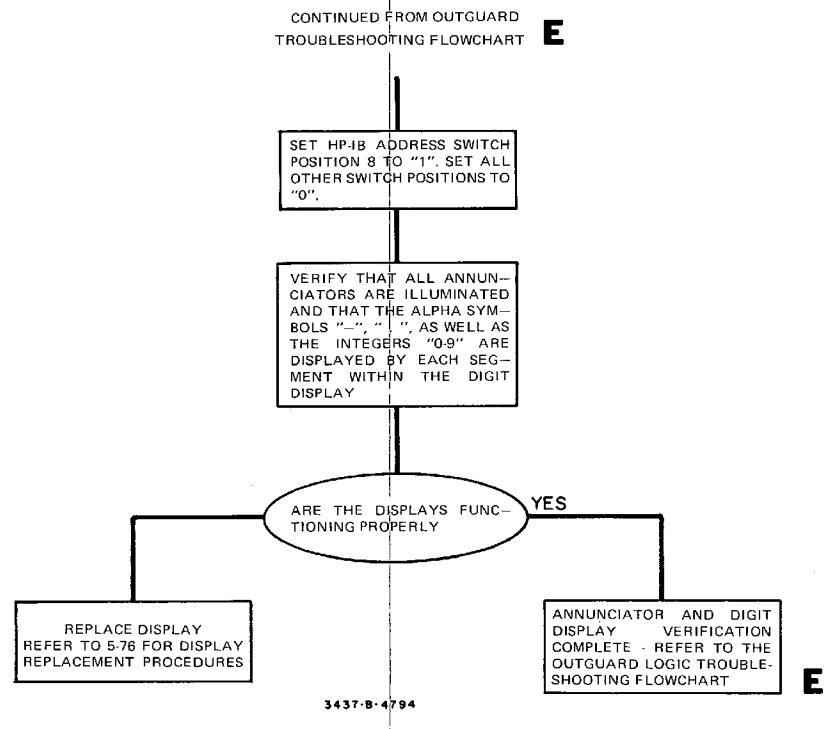


Figure 5-42. Annunciator and Digit Display Troubleshooting Flowchart.

LOGIC TRACER CONTROL INPUTS VERIFICATION TEST. THIS TEST VERIFIES THAT THE 3437A IS PROVIDING THE REQUIRED LOGIC TRACER CONTROL INPUTS (CLOCK, START/STOP).

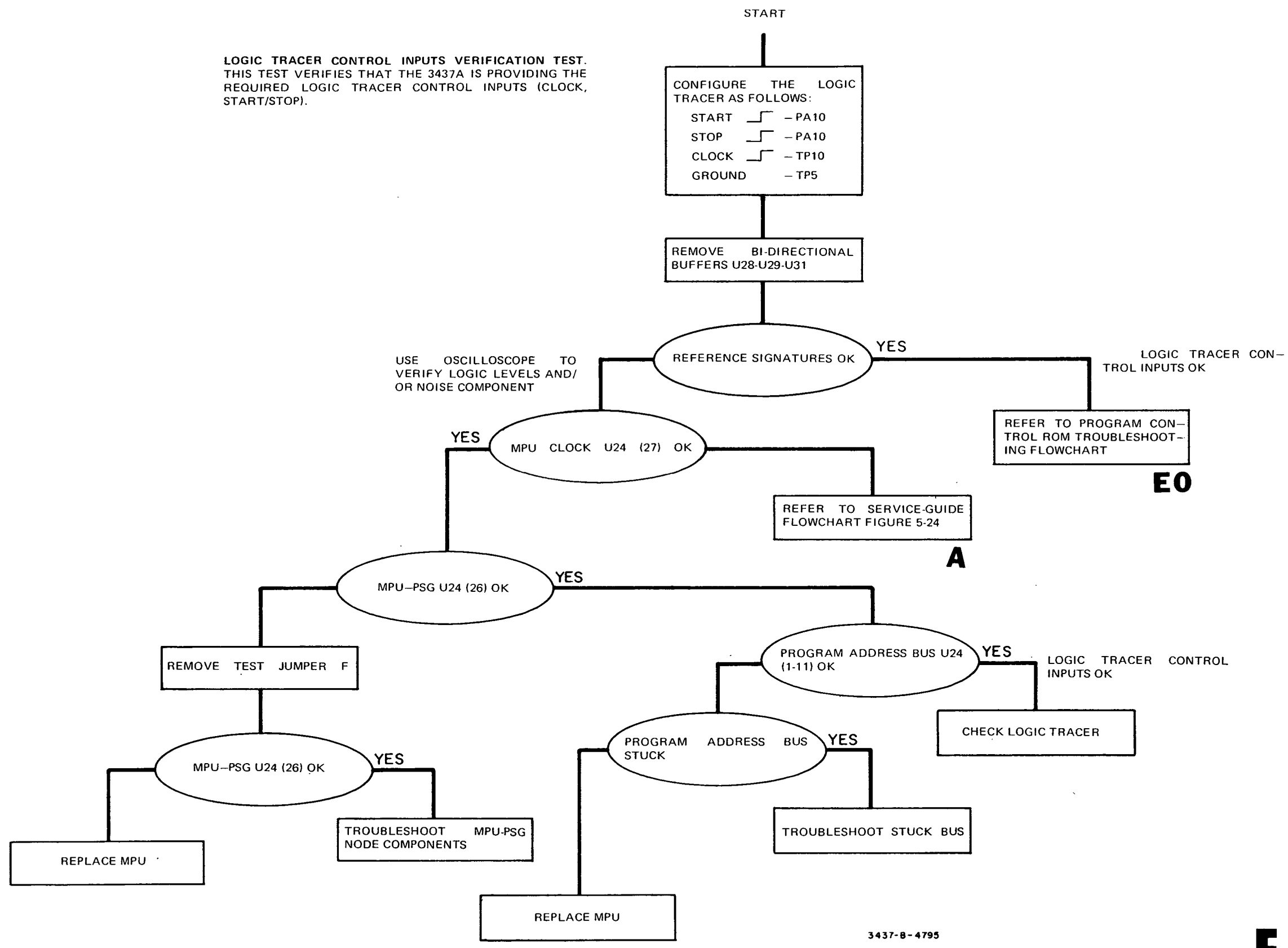


Figure 5-43. Logic Tracer Control - Inputs Troubleshooting Flowchart.

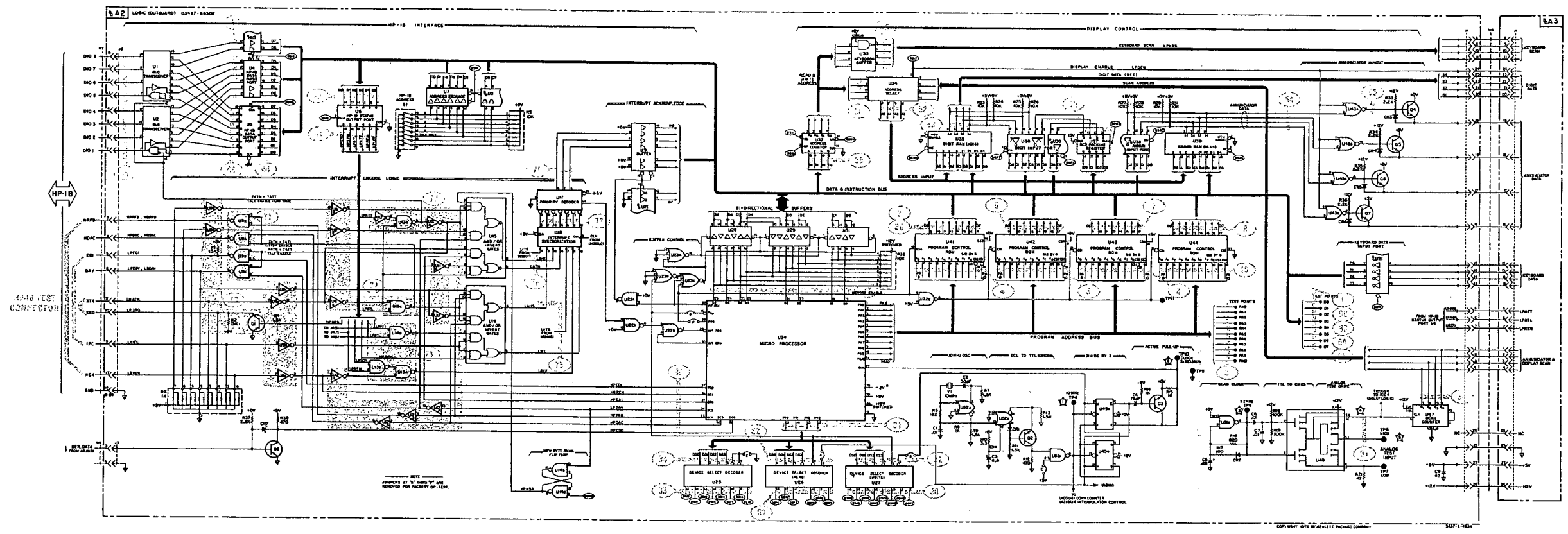


Figure 5-44. Signature Set Locator, Outguard Logic.
Rev. A 5-79/5-80

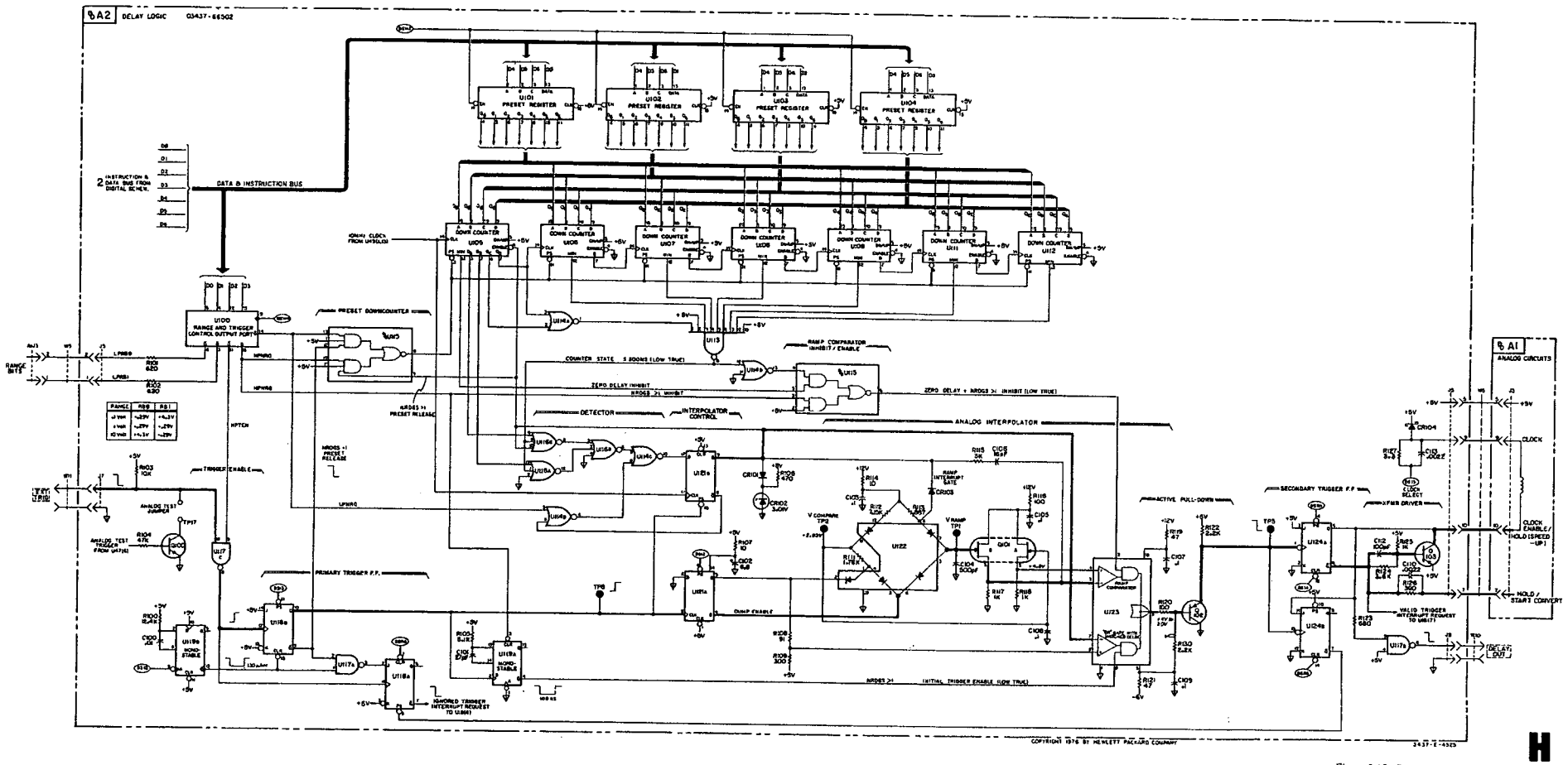


Figure 5-45. Signature Set Locator Delay Logic.
Rev. A 5-81/5-82

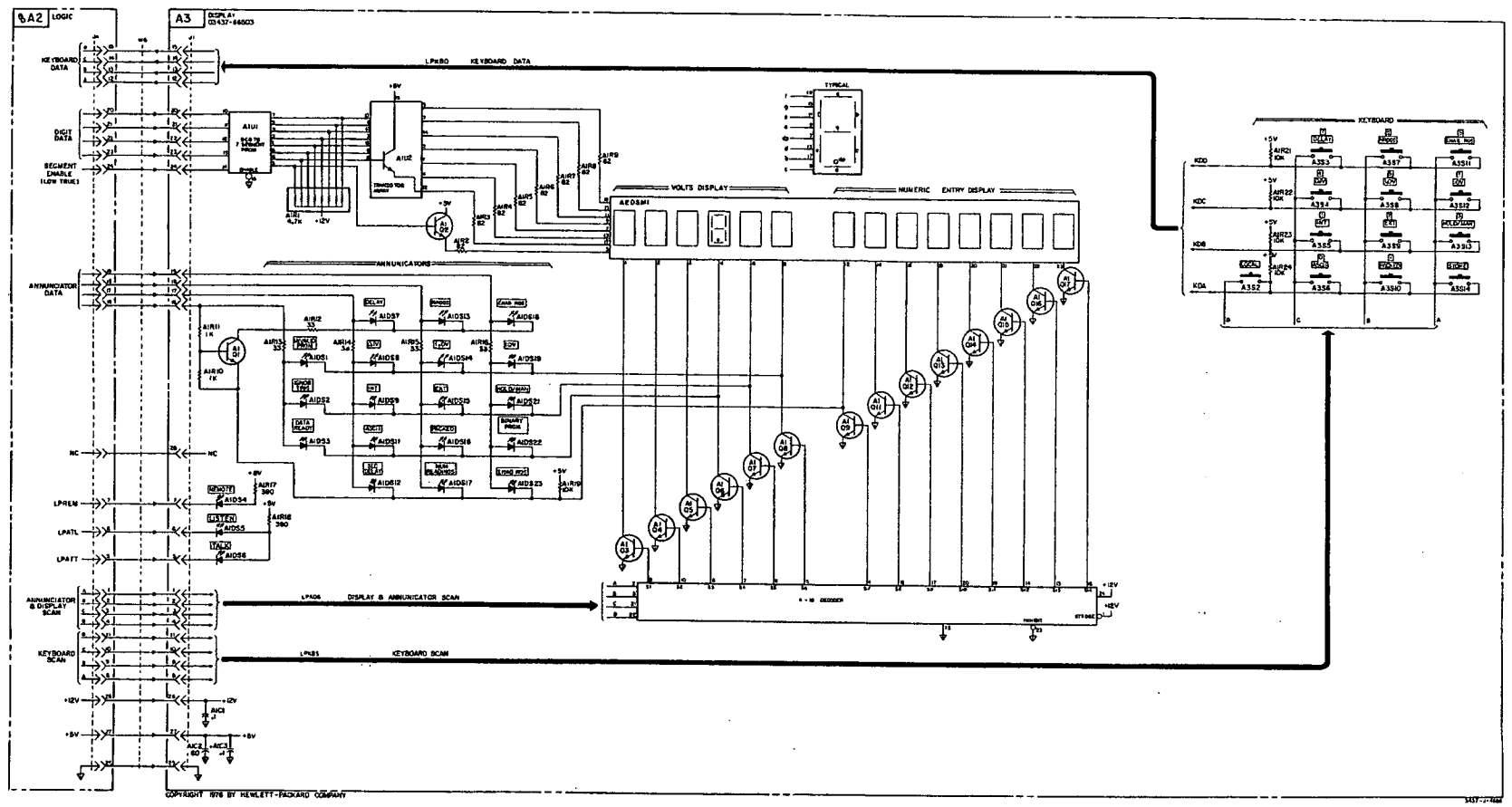


Figure 5-46. Signature Set Locator Display.

5-145. NOISE MEASUREMENT PROCEDURE (HIGH RESOLUTION DC SOURCE).

5-146. To measure the noise component of the high resolution dc source, perform the following procedure:

a. Connect the divided output of the DC source to both channels of an oscilloscope having alternate sweep capability. (Position each trace equi-distance from the center of the CRT so that a distinct separation is visible. Set the gain control for each channel (volts/division) equal.

b. Using one of the position controls, vary the position of one trace so that the separation between the traces (dark band) just disappears.

c. Disconnect the DC source from the oscilloscope. The separation between the noise free traces represents *twice* the RMS noise component of the DC source.

1. The oscilloscope bandwidth must be ⩾ the bandwidth of the 3437A voltage range being calibrated. (Both vertical channels must be identically calibrated.)

5-147. The 3437A voltage ranges and corresponding RMS–noise voltage maximum values are shown below.

Range	Volts/Count	Maximum RMS Noise Voltage - 0.2 Counts
.1 Volt	100 μV	20 μV
1 Volt	1 mV	200 μV
10 Volt	10 mV	2 mV

5-148. 3437A PERFORMANCE TEST FIXTURES.

5-149. Performance–Test Source Interface (-hp- 34114A).

5-150. The performance–test source interface (illustrated in Figure 5-47) functions as a waveform shaping network, assuring that the negative transition of the -hp- 3310A output waveform (3437A dynamic accuracy performance test) does not go below zero (Figure 5-48).

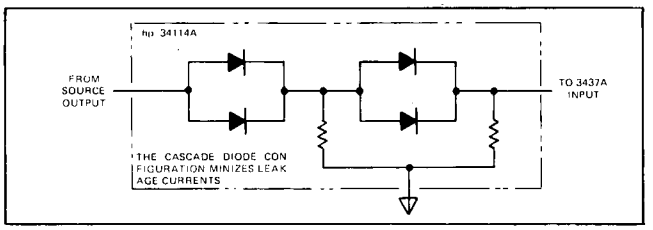


Figure 5-47. Performance-Test Source Interface.

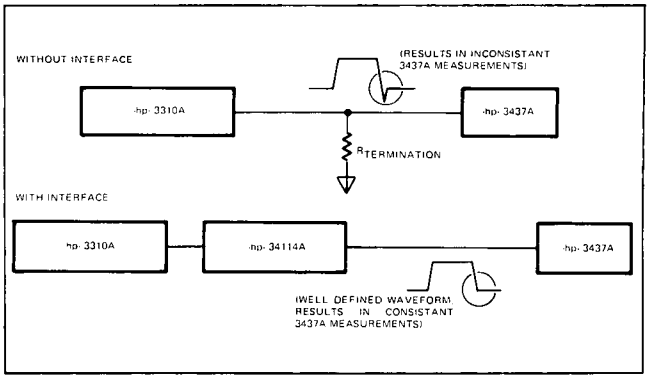


Figure 5-48. Source-Interface Implementation.

5-151. Performance–Test Trigger Interface (-hp- 34113A).

5-152. The performance–test trigger interface (illustrated in Figure 5-49) level shifts the DC component of the -hp- 180A main gate output so that the output waveform occurs within the specified voltage range of the 3437A external trigger input (Figure 5-50).

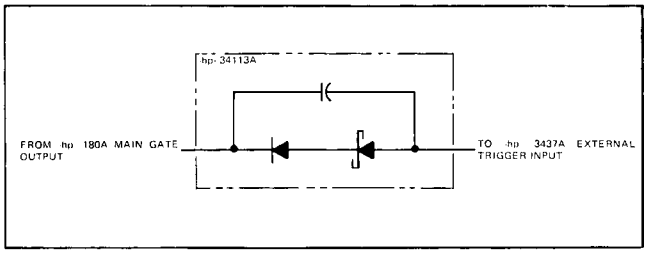


Figure 5-49. Performance-Test Trigger Interface.

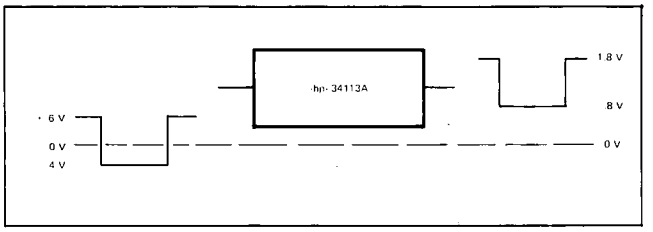


Figure 5-50. Trigger Interface Implementation.

5-153. The -hp- 34113A level shifts the main gate output ≅ 1.2 volts (2 silicon diode drops).

NOTE

The trigger interface is not required if the main gate output of the oscilloscope used in the performance–tests is within the defined standard TTL voltage levels (negative edge).

PERFORMANCE TEST CARD

Hewlett-Packard 3437A
System Voltmeter
Serial No. _____

Test Performed By _____
Date _____

NOTE

The test limits provide an additional significant figure so that the stability of the LSD can be verified.

Test Description	Specification	Limit	Test Result
1. Static Accuracy	90 days, 25°C, ± 5°C		
A. .1 Volt Range	± 0.05°% of reading ± 1.6 digits		
+ .0400		.03982 to .04018	_____
- .0400		-.04018 to -.03982	_____
- .0800		-.08020 to -.07980	_____
+ .0800		.07980 to .08020	_____
+ .1200		.11978 to .12022	_____
- .1200		-.12022 to -.11978	_____
- .1600		-.15976 to -.16024	_____
+ .1600		.16024 to .15976	_____
B. 1 Volt Range	± 0.03% of reading ± 1.6 digits		
+ 0.400		.3983 to .4017	_____
- 0.400		- .4017 to - .3983	_____
- 0.800		- .8018 to - .7982	_____
+ 0.800		.7982 to .8018	_____
+ 1.200		1.1980 to 1.2020	_____
- 1.200		-1.2020 to -1.1980	_____
- 1.600		-1.6021 to -1.5979	_____
+ 1.600		1.5979 to 1.6021	_____
C. 10 Volt Range	± 0.05% of reading ± 1.8 digits		
+ 04.00		3.980 to 4.020	_____
- 04.00		- 4.020 to - 3.980	_____
- 08.00		- 8.022 to - 7.978	_____
+ 08.00		7.978 to 8.022	_____
+ 12.00		11.976 to 12.024	_____
- 12.00		-12.024 to -11.976	_____
- 16.00		-16.026 to -15.974	_____
+ 16.00		15.974 to 16.026	_____
2. Dynamic Accuracy			
10 volt range 10 volt step	± 200 mV of final value within 700 ns	- 200 mV to + 200 mV	_____
10 volt range 10 V step	± 30 mV of final value within 7.5 μs	- 30 mV to + 30 mV	_____
1 volt range 1 V step	± 20 mV of final value within 700 ns	- 20 mV to + 20 mV	_____
1 volt range 1 V step	± 3 mV of final value within 1.5 μs	- 3 mV to + 3 mV	_____
.1 volt range .1 V step	± 200 μV of final value within 25 μs	- 200 μV to + 200 μV	_____
3. Bandwidth (3 dB)			
A. .1 volt range	40 kHz	⩾40 kHz	_____
B. 1 volt range	1.1 MHz	⩾1.1 MHz	_____
C. 10 volt range	1.0 MHz	⩾1.0 MHz	_____

PERFORMANCE TEST CARD (Cont'd)

Test Description	Specification	Limit	Test Result
4. Delay			
A. Accuracy	± 0.008% Delay + Delay Offset		
0		75 ns to 125 ns	_____
100 ns		175 ns to 225 ns	_____
500 ns		575 ns to 625 ns	_____
1 μs		1.075 μs to 1.125 μs	_____
500 μs		499.960 μs to 500.165 μs	_____
1 ms		.999920 ms to 1.0002050 μs	_____
500 ms		499.960 ms to 500.040125 μs	_____
.9999999		.9999199975 sec to 1.000080030 sec	_____
B. Jitter			
0	⩽2 ns	⩽2 ns	_____
100 ns	⩽2 ns	⩽2 ns	_____
500 ns	⩽10 ns + 0.0002% delay	⩽10 ns	_____
1 μs		⩽10 ns	_____
500 μs		⩽11 ns	_____
1 ms		⩽12 ns	_____
500 ms	⩽110 ns	⩽110 ns	_____
.9999999	⩽110 ns	⩽110 ns	_____
5. Number of Readings	Number of readings programmed		
10		10	_____
50		50	_____
100		100	_____
500		500	_____
1000		1000	_____
5000		5000	_____
9999		9999	_____
6. Common Mode Rejection Ratio	⩾75 dB (1 kΩ unbalance in low input lead @ 60 Hz)	⩾75 dB	_____
7. Overload Display			
.1 volt range	± .9999		_____
1 volt range	± 9.999		_____
10 volt range	± 99.99		_____
8. HP-IB Interface			
A. Program code	3437A response		_____
D	delay entry		_____
N	NRDGS entry		_____
E	ENAB RQS entry		_____
R_1	.1 volt		_____
2	1 volt		_____
3	10 volts		_____
T_1	INT		_____
2	EXT		_____
3	Hold/man		_____
F_1	ASCII		_____
2	packed		_____

PERFORMANCE TEST CARD (Cont'd)

Test Description	Specification	Limit		Test Result
B. Message code	3437A response			
MLA	remote & addressed to listen			_____
MTA	remote & addressed to talk			_____
DCL	turn on state			_____
SDC	turn on state			_____
GET	trigger in any trigger mode			_____
GTL	remote to local			_____
LLO	local key disabled			_____
UNL	unlisten			_____
UNT	untalk			_____
IFC	unlisten/untalk			_____
C. Reading Rate				
ASCII	⩾3700 Hz			_____
Packed	⩾5900 Hz			_____
D. Format				
ASCII	6 byte data format	+ 1.532 CR LF&EOI		_____
Packed	2 byte daga format	Byte	Octal Code	
		1	365	_____
		2	062 & EOI	_____
E. SRQ Status Byte		044		_____
F. Binary Prgm				
Learn		Byte	Code	
		1	307	_____
		2	031	_____
		3	166	_____
		4	X00	_____
		5	000	_____
		6	120	_____
		7	000 & EOI	_____
Prgm		Delay	500 μs	_____
		NRDGS	1976	_____
		ENAB RQS	4	_____
		Range	1 V	_____
		Trigger	INT	_____
		Format	ASCII	_____

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information concerning replacement parts as well as a table of abbreviations (Table 6-2) that are used throughout the manual. Included is a parts listing (alphanumeric order of reference designators), and ordering information.

6-3. Table of Replaceable Parts.

6-4. Table 6-3 lists the 3437A replaceable parts. The table contains the following information:

a. -hp- part number.

b. Total quantity of part used in instrument.

c. Part description.

d. Manufacturer's code (Table 6-1).

e. Manufacturer's part number.

6-5. Chassis Mounted and Miscellaneous Parts.

6-6. Chassis mounted components, mechanical and miscellaneous parts not having reference designators, are listed at the end of Table 6-3.

6-7. Ordering Information.

6-8. To obtain replacement parts, address order (or inquiry) to the nearest Hewlett-Packard Sales and Service Office (Appendix A). Identify parts by -hp- Part Numbers. Include the instrument model and serial number.

6-9. Non-Listed Parts.

6-10. To obtain a part that is not listed, include:

a. Instrument model and serial number.

b. Description of the part.

c. Function (and location) of the part.

Table 6-1. Code List of Manufacturers.

Mfr. No.	Manufacturer	Address
0011J	Jermyn Industries	Seven Oaks Kent, England
01121	Allen-Bradley Co	Milwaukee, WI 53212
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX 75231
02114	Ferroxcube Corp	Saugerties, NY 12477
02735	RCA Corp Solid State Div	Sommerville, NJ 08876
04713	Motorola Semiconductor Products	Phoenix, AZ 85008
07263	Fairchild Semiconductor Div	Mountain View, CA 94040
15818	Teledyne Semiconductor	Mountain View, CA 94040
17856	Siliconix Inc	Santa Clara, CA 95050
19701	Mepco/Electra Corp	Mineral Wells, TX 76067
24226	Gowanda Electronics Corp	Gowanda, NY 14070
24546	Corning Glass Works (Bradford)	Bradford, PA 16701
24931	Specialty Connector Co Inc	Indianapolis, IN 46227
27014	National Semiconductor Corp	Santa Clara, CA 95051
28480	Hewlett-Packard Co Corp HQ	Palo Alto, CA 94304
50579	Litronix Inc	Cupertino, CA 95014
56289	Sprague Electric Co	North Adams, MA 01247
72136	Electro Motive Corp Sub IEC	Willimantic, CT 06226
73138	Beckman Instruments Inc Helipot Div	Fullerton, CA 92634
74970	Johnson E F Co	Waseca, MN 56093
75915	Littelfuse Inc	Des Plaines, IL 60016
76854	Oak Ind Inc SW Div	Crystal Lake, IL 60014
95121	Quality Components Inc	St Marys, PA 15857
95275	Vitramon Inc	Bridgeport, CT 06601
98291	Sealectro Corp	Mamaroneck, NY 10544

Table 6-2. Abbreviations.

ACK	Acknowledge
A/D	Analog to Digital
ASCII	American Standard Code for Information Interchange
ATN	Attention
AVAIL	Available
CLK	Clock
CMOS	Complimentary Metal Oxide Semiconductor
COMP	Compensated
DAV	Data Valid
DCØ -6	Direct Control Ø - 6
DIO	Data Input Out
dp	Decimal Point
DSRX	Device Select Read
DSWX	Device Select Write
DSXX	Device Select (Non R/W)
ECL	Emitter Coupled Logic
ENAB RQS	Enable Request
EOI	End or Identify
EXT	External
FF	Flip-Flop
GND	Ground
HP-IB	Hewlett-Packard Interface Bus
IFC	Interface Clear
IGNOR	Ignore
INT ENA	Interrupt Enable
INT REQ	Interrupt Request
MHz	Megahertz
NDAC	Data not Accepted
NRDGS	Number of Readings
NRFD	Not Ready for Data
ns	10^{-9} second
PA	Program Address
PERM	Permanent
PRGM	Program
PROM	Programmable Read-Only-Memory
PSG	Program Source Gate
RAM	Random Access Memory
REF	Reference
REN	Remote Enable
ROM	Read-Only-Memory
RSQ Status	Request Service Status
R/W	Read/Write (Low Read)
SEC	Second
SER	Serial
S/H	Sample and Hold
SRQ	Service Request
TRIG	Trigger
TTL	Transistor Transistor Logic
XMFR	Transformer

Ag . . . . . silver
Al . . . . . aluminum
A . . . . . ampere(s)
Au . . . . . gold

C . . . . . capacitor
cer . . . . . ceramic
coef . . . . . coefficient
com . . . . . common
comp . . . . . composition
conn . . . . . connection

dep . . . . . deposited
DPDT . . . . . double-pole double-throw
DPST . . . . . double-pole single-throw

elect . . . . . electrolytic
encap . . . . . encapsulated

F . . . . . farad(s)
FET . . . . . field effect transistor
fxd . . . . . fixed

GaAs . . . . . gallium arsenide
GHz . . . . . gigahertz = 10^{+9} hertz
gd . . . . . guard(ed)
Ge . . . . . germanium
gnd . . . . . ground(ed)

H . . . . . henry(ies)
Hg . . . . . mercury

Hz . . . . . hertz (cycle(s) per second)

ID . . . . . inside diameter
impg . . . . . impregnated
incd . . . . . incandescent
ins . . . . . insulation(ed)

kΩ . . . . . kilohm(s) = 10^{+3} ohms
kHz . . . . . kilohertz = 10^{+3} hertz

L . . . . . inductor
lin . . . . . linear taper
log . . . . . logarithmic taper

mA . . . . . milliampere(s) = 10^{-3} amperes
MHz . . . . . megahertz = 10^{+6} hertz
MΩ . . . . . megohm(s) - 10^{+6} ohms
met flm . . . . . metal film
mfr . . . . . manufacturer
ms . . . . . millisecond
mtg . . . . . mounting
mV . . . . . millivolt(s) = 10^{-3} volts
μF . . . . . microfarad(s)
μs . . . . . microsecond(s)
μV . . . . . microvolt(s) = 10^{-6} volts
my . . . . . Mylar®

nA . . . . . nanoampere(s) = 10^{-9} amperes
NC . . . . . normally closed
Ne . . . . . neon
NO . . . . . normally open

NPO . . . . . negative positive zero (zero temperature coefficient)
ns . . . . . nanosecond(s) = 10^{-9} seconds
nsr . . . . . not separately replaceable

Ω . . . . . ohm(s)
obd . . . . . order by description
OD . . . . . outside diameter

p . . . . . peak
pA . . . . . picoampere(s)
pc . . . . . printed circuit
pF . . . . . picofarad(s) 10^{-12} farads
piv . . . . . peak inverse voltage
p/o . . . . . part of
pos . . . . . position(s)
poly . . . . . polystyrene
pot . . . . . potentiometer
p-p . . . . . peak-to-peak
ppm . . . . . parts per million
prec . . . . . precision (temperature coeffient, long term stability and/or tolerance)

R . . . . . resistor
Rh . . . . . rhodium
rms . . . . . root-mean-square
rot . . . . . rotary

Se . . . . . selenium
sect . . . . . section(s)
Si . . . . . silicon

sl . . . . . slide
SPDT . . . . . single-pole double-throw
SPST . . . . . single-pole single-throw

Ta . . . . . tantalum
TC . . . . . temperature coefficient
TiO_2 . . . . . titanium dioxide
tog . . . . . toggle
tol . . . . . tolerance
trim . . . . . trimmer
TSTR . . . . . transistor

V . . . . . volt(s)
vacw . . . . . alternating current working voltage
var . . . . . variable
vdcw . . . . . direct current working voltage

W . . . . . watt(s)
w/ . . . . . with
wiv . . . . . working inverse voltage
w/o . . . . . without
ww . . . . . wirewound

* . . . . . optimum value selected at factory, average value shown (part may be omitted)
** . . . . . no standard type number assigned selected or special type

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DECIMAL MULTIPLIERS

Prefix	Symbols	Multiplier	Prefix	Symbols	Multiplier
tera	T	10^{12}	centi	c	10^{-2}
giga	G	10^{9}	milli	m	10^{-3}
mega	M or Meg	10^{6}	micro	μ	10^{-6}
kilo	K or k	10^{3}	nano	n	10^{-9}
hecto	h	10^{2}	pico	p	10^{-12}
deka	da	10	femto	f	10^{-15}
deci	d	10^{-1}	atto	a	10^{-18}

STD-B-2734

DESIGNATORS

A . . . . . assembly
B . . . . . motor
BT . . . . . battery
C . . . . . capacitor
CR . . . . . diode
DL . . . . . delay line
DS . . . . . lamp
E . . . . . misc electronic part
F . . . . . fuse

FL . . . . . filter
HR . . . . . heater
IC . . . . . integrated circuit
J . . . . . jack
K . . . . . relay
L . . . . . inductor
M . . . . . meter
MP . . . . . mechanical part
P . . . . . plug

Q . . . . . transistor
QCR . . . . . transistor-diode
R . . . . . resistor
RT . . . . . thermistor
S . . . . . switch
T . . . . . transformer
TB . . . . . terminal board
TC . . . . . thermocouple
TP . . . . . test point

TS . . . . . terminal strip
U . . . . . microcircuit
V . . . . . vacuum tube, neon bulb,photocell, etc.
W . . . . . cable
X . . . . . socket
XDS . . . . . lampholder
XF . . . . . fuseholder
Y . . . . . crystal
Z . . . . . network

Table 6-3. Replaceable Parts.

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	03437-66501	1	INGUARD P.C. ASSEMBLY	28480	03437-66501
A1C1	0160-3842	1	CAPACITOR-FXD 3.3PF +-.25PF 1000WVAC	28480	0160-3842
A1C2	0160-0946	1	CAPACITOR-FXD 13PF +-5% 500WVDC PORC	95275	VY10CA130JE
A1C3*	0180-999P	2	CAPACITOR, FXD (PAD VALUE)	28480	0180-999P
A1C4	0121-0131	1	CAPACITOR-V TRMR-AIR 1.2/4.2PF 350V	74970	189-0501-005
A1C5	0160-2306	2	CAPACITOR-FXD 27PF +-5% 300WVDC MICA	28480	0160-2306
A1C6	0160-2249	2	CAPACITOR-FXD 4.7PF +-.25PF 500WVDC CER	28480	0160-2249
A1C7	0140-0196	1	CAPACITOR-FXD 150PF +-5% 300WVDC MICA	72136	DM15F151J0300WV1CR
A1C8	0160-3847	15	CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C9	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C10	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C11 Δ5	0180-0291	11	CAPACITOR-FXD 1 UF +-20% 6 VDC TA	04200	150D105X9035A2
A1C12, C13	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C14	0150-0042	1	CAPACITOR-FXD 4.7PF +-5% 500WVDC TI DIOX	95121	TYPE QC
A1C15	0160-2249		CAPACITOR-FXD 4.7PF +-.25PF 500WVDC CER	28480	0160-2249
A1C16	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C17, C18	0150-0121	14	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C19,	0160-2200	1	CAPACITOR-FXD 43PF +-5% 300WVDC MICA	28480	0160-2200
A1C20* Δ1			PAD VALUE		
	0160-2322		CAPACITOR-FXD 18PF +-5% 100V	28480	0160-2322
	0160-2199		CAPACITOR-FXD 30PF +-5% 300V	28480	0160-2199
	0160-2307		CAPACITOR-FXD 47PF +-5% 300V	28480	0160-2307
A1C21	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C22	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C23	0160-2238		CAPACITOR-FXD 1.5PF +-25PF 50WVDC CER	28480	0160-2238
A1C24	0160-2204	2	CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A1C25	0140-0198	2	CAPACITOR-FXD 200PF +-5% 300WVDC MICA	72136	DM15F201J0300WV1CR
A1C26	0160-2264	1	CAPACITOR-FXD 20PF +-5% 500WVDC CER	28480	0160-2264
A1C27	0160-4438	1	CAPACITOR-FXD 470PF +-2.5% 160WVDC POLYP	28480	0160-4438
A1C28	0160-2243	1	CAPACITOR-FXD 2.7PF +-.25PF 500WVDC CER	28480	0160-2243
A1C29	0150-0091	1	CAPACITOR-FXD 1.5PF +-.25PF 500WVDC CER	28480	0150-0091
A1C30	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C31	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C32	0180-0104	2	CAPACITOR-FXD 200UF+75-10% 16VDC AL	56289	30D207G016DF2
A1C33	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C34	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A1C35	0180-0104		CAPACITOR-FXD 200UF+75-10% 16VDC AL	56289	30D207G016DF2
A1C36 Δ1	0160-0127		CAPACITOR-FXD .1UF +100-0% 50WVDC CER	28480	0160-0127
A1C37	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C38	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C41	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C42	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C43	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A1C44 Δ3	0180-0210	1	CAPACITOR-FXD 3.3UF +-20% 15VDC TA	04200	150D335X0015A2
A1C45	0180-0197	4	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A1C46, C47, C48	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A1C49	0160-0128		CAPACITOR-FXD 2.2UF 25WVDC	28480	0160-0128
A1C50	0140-0198		CAPACITOR-FXD 200PF 300VDC	04522	DM15F201J0300WV1CR (S/N ≥ 1630A00271)
A1C201	0150-0121		CAPACITOR-FXD .1UF +80 -20% 50WVDC CER	28480	0150-0121
A1C202	0180-0050	1	CAPACITOR-FXD 40UF+75-10% 50VDC AL	56289	30D406G050DD2
A1C203	0180-2638	1	CAPACITOR-FXD 220UF+75-10% 35VDC AL	56289	500D227H035DF7
A1C204 Δ 10	0180-0050	2	CAPACITOR-FXD 0UF+75-10% 50VDC AL	04200	30D206G050DD2
A1C205 Δ 10	0180-0050		CAPACITOR-FXD 0UF+75-10% 50VDC AL	04200	30D206G050DD2
A1C206	0180-0374	5	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C207	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A1C208	0180-0374		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C209	0160-0128		CAPACITOR-FXD 2.2UF +-20% 50VDC	28480	0160-0128
A1CR1	1901-0376	4	DIODE-GEN PRP 35V 50MA DO-7	28480	1901-0376
A1CR2	1901-0376		DIODE-GEN PRP 35V 50MA DO-7	28480	1901-0376
A1CR3	1901-0519	4	DIODE-SWITCHING 200V 50NS DO-34	28480	1901-0519
A1CR4	1901-0519		DIODE-SWITCHING 200V 50NS DO-34	28480	1901-0519
A1CR5	1902-3104	1	DIODE-ZNR 5.62V 5% DO-7 PD=.4W TC=+.016%	15818	CD 35634
A1CR6	1902-0057	2	DIODE-ZNR 6.49V 5% DO-7 PD=.4W TC=+.029%	04713	SZ 10939-128
A1CR7	1901-0040	23	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR8	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR9	1902-3080	2	DIODE-ZNR 4.53V 2% DO-7 PD=.4W TC=-.027%	04713	SZ 10939-84
A1CR11	1902-3080		DIODE-ZNR 4.53V 2% DO-7 PD=.4W TC=-.027%	04713	SZ 10939-84
A1CR12 Δ6	1902-3235	1	DIODE-ZNR 19.6V 5%	04713	SZ 10939-267
A1CR13	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR14	1902-0057		DIODE-ZNR 6.49V 5% DO-7 PD=.4W TC=+.029%	04713	SZ 10939-128
A1CR15	1902-0126	2	DIODE-ZNR 2.61V 5% DO-7 PD=.4W TC=-.073%	04713	SZ 10939-14
A1CR16	1902-0126		DIODE-ZNR 2.61V 5% DO-7 PD=.4W TC=-.073%	04713	SZ 10939-14
A1CR17	1901-0050	2	DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
A1CR18	1901-0050		DIODE-SWITCHING 80V 200MA 2NS DO-7	28480	1901-0050
A1CR19	1902-0904	1	DIODE, REF,	28480	1902-0904
A1CR21	1990-0486	23	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A1CR22	1902-3002	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	15818	CD 35526

Δ1-7 See note on schematic 1.
Δ10 See note on schematic 5.

See introduction to this section for ordering information

Table 6-3. Replaceable Parts (Cont'd).

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1CR23	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A1CR24	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR27	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR28	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR29	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR31	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR32	1990-0450	2	LED-VISIBLE LUM-INT=800UCD IF=50MA-MAX	28480	1990-0450
A1CR33	1990-0450		LED-VISIBLE LUM-INT=800UCD IF=50MA-MAX	28480	1990-0450
A1CR34	1902-3214	1	DIODE-ZNR 16.2V 2% DO-7 PD=.4W TC=+.066%	28480	1902-3214
A1CR35	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR36	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR37	1901-0376		DIODE-GEN PRP 35V 50MA DO-7	28480	1901-0376
A1CR38	1901-0376		DIODE-GEN PRP 35V 50MA DO-7	28480	1901-0376
A1CR39	1901-0519		DIODE-SWITCHING 200V 50NS DO-34	28480	1901-0519
A1CR40	1901-0519		DIODE-SWITCHING 200V 50NS DO-34	28480	1901-0519
A1CR201 ΔA	1901-0704	16	DIODE-PWR RECT IN4002	28480	1901-0704
A1CR202 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR203 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR204 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR205 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR206 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR207 ΔA	1901-0704		DIODE-PWR RECT IN 4002	28480	1901-0704
A1CR208 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR209 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR211 ΔA	1901-0704		DIODE-PWR RECT IN4002	28480	1901-0704
A1CR212 ΔB	1902-3183	4	DIODE-ZNR 12.1V 2% DO-7 PD=.4W TC=+-.064%	28480	1902-3183
A1CR213 ΔB	1902-3183	4	DIODE-ZNR 12.1 V 2% DO-7 PD=.4W TC=+-.064%	28480	1902-3183
A1CR214	1902-3149	1	DIODE-ZNR 9.09V 5% DO-7 PD=.4W TC=+.057%	04713	SZ 10939-170
A1CR215	1902-3136	1	DIODE-ZNR 8.06V 5% DO-7 PD=.4W TC=+.052%	04713	SZ 10939-155
A1CR216	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR217	1902-3190	1	DIODE-ZNR 13V 5% DO-7 PD=.4W TC=+.06%	04713	SZ 10939-215
A1CR218	1902-0049	2	DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	28480	1902-0049
A1CR219	1902-3085		DIODE-ZNR 4.75V 5% DO-7 PD=.4W TC=-.019%	15818	CD 35613
A1CR221	1902-0029		DIODE-ZNR 12.1V 5% DO-15 PD=1W TC=+.064%	28480	1902-0029
A1CR222	1902-0029		DIODE-ZNR 12.1V 5% DO-15 PD=1W TC=+.064%	28480	1902-0029
A1L201	9100-1620	1	COIL-MLD 15UH 10% Q=65 .155DX.375LG	24226	15/152
A1Q1	1855-0242	1	TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0242
A1Q2 Δ4	1855-0252		TRANSISTOR J-FET	28480	1855-0252
A1Q3	03437-62501	3	MATCHED SET (A2Q3-A2R14-A2R18)	28480	03437-62501
A1Q4	1855-0081	3	TRANSISTOR J-FET 2N5245 N-CHAN D-MODE SI	01295	2N5245
A1Q5	1855-0081		TRANSISTOR J-FET 2N5245 N-CHAN D-MODE SI	01295	2N5245
A1Q6	1855-0082	1	TRANSISTOR MOSFET P-CHAN D-MODE SI	28480	1855-0082
A1Q7	1855-0081		TRANSISTOR J-FET 2N5245 N-CHAN D-MODE SI	01295	2N5245
A1Q8	1855-0091	1	TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0091
A1Q9	1855-0093	1	TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI	28480	1855-0093
A1Q11	1855-0053	1	TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0053
A1Q13	1854-0071	6	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q14	1853-0066	2	TRANSISTOR PNP SI TO-92 PD=625MW	28480	1853-0066
A1Q15	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q16	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q17	1854-0215		TRANSISTOR NPN SI PD=350MW FT=300MHZ	02037	SPS 3611
A1Q18	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1Q19	1853-0066		TRANSISTOR PNP SI TO-92 PD=625MW	28480	1853-0066
A1Q25 Δ7	1855-0252		TRANSISTOR J-FET N-CHAN D-MODE TO-72 SI	28480	1855-0252
A1Q201	1854-0565	1	TRANSISTOR NPN SI PD=1W FT=50MHZ	28480	1854-0565
A1Q202	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A1R1	03437-62502		MATCHED SET (A1R1 & A1R8)	28480	03437-62502
A1R2	0683-4715	8	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R3	0683-3915	4	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A1R4	0683-3915		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A1R5	0683-1045	15	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R6	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R7	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R9	0757-0442	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R10	0683-1015	5	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R11	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R12	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R13	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R15	0698-6704	1	RESISTOR 24.9K .25% .125W F TC=0+-100	24546	NA4
A1R16	0683-2225	11	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R17	0698-4123	2	RESISTOR 499 1% .125W F TC=0+-100	24546	C4-1/8-T0-499R-F
A1R19	0757-0199	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
A1R21	0698-4123		RESISTOR 499 1% .125W F TC=0+-100	24546	C4-1/8-T0-499R-F

Δ1-7 See note on schematic 1.

ΔA These changed from part number 1901-0045 on serial numbers greater than 1630A00620.

ΔB Serial numbers greater than 1630A00135, CR213 was changed from a 5% component to insure that the CR12 changed in Δ6 does not affect overload recovery time.

See introduction to this section for ordering information

Table 6-3. Replaceable Parts (Cont'd).

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R22	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R23	0683-1835	1	RESISTOR 18K 5% .25W FC TC=-400/+800	01121	CB1835
A1R24	0683-3325	6	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R25	0683-3325		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R26	0683-4705	12	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R27	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R28	0683-3325		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R29	0683-1135	1	RESISTOR 11K 5% .25W FC TC=-400/+800	01121	CB1135
A1R30	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R31	0683-3035	2	RESISTOR 30K 5% .25W FC TC=-400/+800	01121	CB3035
A1R32	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R33	0683-1505	1	RESISTOR 15 5% .25W FC TC=-400/+500	01121	CB1505
A1R34	0683-6815	5	RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A1R35	0698-4498	1	RESISTOR 53.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5362-F
A1R36*	0683-999P	1	RESISTOR-FXD (PAD VALUE)	28480	0683-999P
A1R37	0683-5125	3	RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A1R38	0683-2235	7	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A1R39	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R41	0683-5125		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A1R42	0683-6225	2	RESISTOR 6.2K 5% .25W FC TC=-400/+700	01121	CB6225
A1R43	0683-6225		RESISTOR 6.2K 5% .25W FC TC=-400/+700	01121	CB6225
A1R44	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R45	0683-3335	1	RESISTOR 33K 5% .25W FC TC=-400/+800	01121	CB3335
A1R46	0683-6835	1	RESISTOR 68K 5% .25W FC TC=-400/+800	01121	CB6835
A1R47	0683-3325		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R48	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R49	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R51	0683-6825	2	RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A1R52	0683-2025	1	RESISTOR 2K 5% .25W FC TC=-400/+700	01121	CB2025
A1R53	0683-1005	5	RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A1R54	0683-2425	1	RESISTOR 2.4K 5% .25W FC TC=-400/+700	01121	CB2425
A1R55	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A1R57	0698-3156	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1R58	1813-0078	1	RESISTOR (HYBRID)	28480	1813-0078
A1R59	0683-1005		RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A1R61	0698-4478	1	RESISTOR 10.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1072-F
A1R62	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R63	0698-4382	1	RESISTOR 52.3 1% .125W F TC=0+-100	24546	C4-1/8-T0-52R3-F
A1R65	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R66	0683-3925	1	RESISTOR 3.9K 5% .25W FC TC=-400/+700	01121	CB3925
A1R67	2100-3569	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 18-TRN	73138	68WR200K
A1R68	0698-3228	1	RESISTOR 49.9K 1% .125W F TC=0+-100	24546	C-4, T-0
A1R69	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R71	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R72	0683-2205	1	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
A1R73	0757-0270	1	RESISTOR 249K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2493-F
A1R74	0757-0463	1	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-8252-F
A1R75	0683-4745	1	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
A1R76	0683-1635	2	RESISTOR 16K 5% .25W FC TC=-400/+800	01121	CB1635
A1R77	0683-1635		RESISTOR 16K 5% .25W FC TC=-400/+800	01121	CB1635
A1R78	0683-3935	1	RESISTOR 39K 5% .25W FC TC=-400/+800	01121	CB3935
A1R79	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R80	0683-2735	1	RESISTOR 27K 5% .25W FC TC=-400/+800	01121	CB2735
A1R81	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R82	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R83	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R84	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R85	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R86	0683-1535	3	RESISTOR 15K 5% .25W FC TC=-400/+800	01121	CB1535
A1R87	0683-5625	2	RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A1R88	0683-1625	1	RESISTOR 1.6K 5% .25W FC TC=-400/+700	01121	CB1625
A1R89	0683-3005	1	RESISTOR 30 5% .25W FC TC=-400/+500	01121	CB3005
A1R91 Δ7	0683-1636		RESISTOR 36K 5% .25W FC TC=-400/+800	01121	CB1636
A1R92	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R93	0683-2215	2	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R94	0683-2215		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
A1R95	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A1R96 Δ8	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A1R98	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R99	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R100	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R101	0683-1535		RESISTOR 15K 5% .25W FC TC=-400/+800	01121	CB1535
A1R102	0683-3325		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A1R103	0683-1535		RESISTOR 15K 5% .25W FC TC=-400/+800	01121	CB1535
A1R104	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A1R105	0757-0472	1	RESISTOR 200K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2003-F

Δ7,8 See note schematic 1.

See introduction to this section for ordering information

Table 6-3. Replaceable Parts (Cont'd).

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1R106	0698-3243	1	RESISTOR 178K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1783-F
A1R107	0757-0485	1	RESISTOR 681K 1% .125W F TC=0+-100	24546	NA4
A1R108	0698-8349	1	RESISTOR 715K 1% .125W F TC=0+1000	19701	MF5C1/8-TO-7153-F
A1R109	0683-1225	2	RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
A1R115 Δ8	0683-1635		RESISTOR 100 5% .25W FC TC=-400/+500	01607	CB1015
A1R201	06830475	3	RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A1R202	0683-0475		RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A1R203	0683-1035	16	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R204	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A1R205	0683-4325	1	RESISTOR 4.3K 5% .25W FC TC=-400/+700	01121	CB4325
A1R206 Δ10	0683-2425	2	RESISTOR 2.4K5% .25W FC TC=-400/+700	01607	CB2425
A1R207	0683-5625		RESISTOR 5.6K 5% .25W FC TC=-400/+700	01121	CB5625
A1R208	0683-8225	1	RESISTOR 8.2K 5% .25W FC TC=-400/+700	01121	CB8225
A1T1	9100-3881	1	TRANSFORMER, PULSE	28480	9100-3881
A1U1	1820-0981	2	IC-DIGITAL CD4016AY CMOS QUAD BILATL	02735	CD4016AY
A1U2	1820-0477	1	IC LM 301A OP AMP	27014	LM301AN
A1U3	1820-0493	2	IC LM 307 OP AMP	27014	LM307N
A1U4	1826-0208	1	IC LM 310 OP AMP	27014	LM310N
A1U5	1990-0584	1	OPTO-ISOLATOR LED-PXSTR BVCEO=20V	50579	ILD 74
A1U6	1820-0981		IC-DIGITAL CD4016AY CMOS QUAD BILATL	02735	CD4016AY
A1U7	1858-0049	1	TRANSISTOR ARRAY, CA3183E	02735	CA3183E
A1U8	1826-0354	1	OP. AMPL. SPEC. LM310H	27014	LM310H
A1U9	1990-0444	2	OPTO-ISOLATOR LED-PXSTR IF=60 MA - MAX	01295	TIL111
A1U10	1820-1145	4	IC-DIGITAL CD4049AE CMOS HEX 1 INV	02735	CD4049AY
A1U11	1826-0342	1	IC UA 749D OP AMP	07263	UA749DHC
A1U12	1820-0493		IC LM 307 OP AMP	27014	LM307N
A1U13	1826-0065	1	IC LM 311 COMPARATOR	27014	LM311N
A1U14	1820-1145		IC-DIGITAL CD4049AE CMOS HEX 1 INV	02735	CD4049AY
A1U15	1820-1145		IC-DIGITAL CD4049AE CMOS HEX 1 INV	02735	CD4049AY
A1U16	1820-1145		IC-DIGITAL CD4049AE CMOS HEX 1 INV	02735	CD4049AY
A1U17	1820-1722	1	IC-DIGITAL MC14559CP CMOS	04713	MC14559CP
A1U18	1820-1721	1	IC-DIGITAL MC14549CP CMOS	04713	MC14549CP
A1U19	1990-0444		OPTO-ISOLATOR LED-PXSTR IF=60 MA - MAX	01295	TIL111
A1U201	1826-0353	1	IC 78L15 V RGLTR	27014	LM78L15ACH
			A1 MISCELLANEOUS		
	0340-0060	2	TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	98291	FT-E-15
	5040-1449	4	HINGE	28480	5040-1449
A2	03437-66502	1	P.C. ASSEMBLY	28480	03437-66502
A2C1	0150-0093	2	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0150-0093
A2C2	0160-2199	1	CAPACITOR-FXD 30PF +-5% 300WVDC MICA	28480	0160-2199
A2C3	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C4	0160-2202	1	CAPACITOR-FXD 75PF +-5% 300WVDC MICA	28480	0160-2202
A2C5	0180-0373	1	CAPACITOR-FXD .68UF+-10% 35VDC TA	56289	150D684X9035A2
A2C6	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A2C7	0160-3847		CAPACITOR-FXD .01UF +100-0% 50WVDC CER	28480	0160-3847
A2C9	0180-1704	1	CAPACITOR-FXD 47UF+-10% 6VDC TA	56289	150D476X9006B2
A2C100	0160-4064	1	CAPACITOR-FXD .01UF +-10% 25WVDC CER	28480	0160-4064
A2C101	0160-2306		CAPACITOR-FXD 27PF +-5% 300WVDC MICA	28480	0160-2306
A2C102	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C103	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A2C104	0140-0234	1	CAPACITOR-FXD 500PF +-1% 300WVDC MICA	72136	DM15F501F0300WV1C
A2C105	0160-3622	3	CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0160-3622
A2C106	0160-0368	1	CAPACITOR-FXD 16PF +-5% 500WVDC MICA	28480	0160-0368
A2C107	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A2C108	0160-3622		CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0160-3622
A2C109	0160-3622		CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0160-3622
A2C110	0160-4299	2	CAPACITOR-FXD 2200PF +-20% 250WVDC CER	56289	C067F251F222MS22-CDH
A2C112	0160-2204		CAPACITOR-FXD 100PF +-5% 300WVDC MICA	28480	0160-2204
A2C113	0160-4299		CAPACITOR-FXD 2200PF +-20% 250WVDC CER	56289	C067F251F222MS22-CDH
A2C201	0180-0374		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A2C202	0180-1735	3	CAPACITOR-FXD .22UF +-10% 35VDC TA	56289	150D224X9035A2
A2C203	0180-0197		CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
A2C204	0180-2506	1	CAPACITOR-FXD 470UF+50-10% 25VDC AL	28480	0180-2506
A2C205	0160-0170	2	CAPACITOR-FXD .22UF +80-20% 25WVDC CER	28480	0160-0170
A2C206	0180-0374		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A2C207	0180-1735		CAPACITOR-FXD .22UF+-10% 35VDC TA	56289	150D224X9035A2
A2C208	0180-0197		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A2C209	0160-2198	1	CAPACITOR-FXD 20PF +-5% 300WVDC MICA	28480	0160-2198
A2C210	0150-0121	2	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A2C211	0160-0205	1	CAPACITOR-FXD 10PF +-5% 500WVDC MICA	28480	0160-0205
A2C212	0180-0374		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A2C213	0180-1735		CAPACITOR-FXD .22UF+-10% 35VDC TA	56289	150D224X9035A2
A2C214	0180-0197		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
A2C215	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2

Δ8 See note on schematic 1.

Δ10 See note on schematic 5.

See introduction to this section for ordering information

Table 6-3. Replaceable Parts (Cont'd).

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2C216	0180-1715	1	CAPACITOR-FXD 150UF+-10% 6VDC TA	56289	150D157X9006R2
A2C217	0150-0093		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0150-0093
A2C218	0180-0094	2	CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A2C219	0180-0094		CAPACITOR-FXD 100UF+75-10% 25VDC AL	56289	30D107G025DD2
A2C220	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C221	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C222	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C223	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2C224, C225 Δ3	0180-1701		CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
A2CR1	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR2	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR3	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR4	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR5	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR6	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR7	1901-0535	2	DIODE-SCHOTTKY	28480	1901-0535
A2CR101	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR102 Δ2	1902-3048	1	DIODE-ZNR 3.48V 5% DO-7 PD=.4W TC=-.058%	28480	1902-3048
A2CR103	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR104	1901-0535		DIODE-SCHOTTKY	28480	1901-0535
A2CR201	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR202	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR203	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR204	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR205	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR206	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR207	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR208	1901-0040		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A2CR209	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR211	1901-0045		DIODE-PWR RECT 100V 750MA DO-29	28480	1901-0045
A2CR212	1902-0049		DIODE-ZNR 6.19V 5% DO-7 PD=.4W TC=+.022%	28480	1902-0049
	9170-0894	2	CORE-SHIELDING BEAD	02114	56-590-65/4A6
	9170-0894		CORE-SHIELDING BEAD	02114	56-590-65/4A6
A2L201	9100-3807	1	COIL-MLD 110NH 5% Q=50 .155DX.375LG	24226	9572
A2Q1	1854-0094	1	TRANSISTOR NPN SI TO-92	28480	1954-0094
A2Q2	1853-0089	4	TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A2Q3	1853-0089		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A2Q4	1854-0730	20	TRANSISTOR NPN SI TO-92	28480	1854-0730
A2Q5	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A2Q6	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A2Q7	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A2Q8	1854-0215	1	TRANSISTOR NPN SI PD=350MW FT=300MHZ	04713	SPS 3611
A2Q100	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A2Q101	1855-0202	1	TRANSISTOR-JFET DUAL N-CHAN D-MODE SI	17856	E421
A2Q102	1853-0089		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A2Q103	1853-0089		TRANSISTOR PNP 2N4917 SI PD=200MW	07263	2N4917
A2Q201	1853-0016	3	TRANSISTOR PNP SI TO-92 PD=300MW	28480	1853-0016
A2Q202	1854-0210	3	TRANSISTOR NPN 2N2222 SI TO-18 PD=500MW	04713	2N2222
A2Q203	1853-0016		TRANSISTOR PNP SI TO-92 PD=300MW	28480	1853-0016
A2Q204	1854-0210		TRANSISTOR NPN 2N2222 SI TO-18 PD=500MW	04713	2N2222
A2Q205	1853-0016		TRANSISTOR PNP SI TO-92 PD=300MW	28480	1853-0016
A2Q206	1854-0210		TRANSISTOR NPN 2N2222 SI TO-18 PD=500MW	04713	2N2222
A2R1	0683-1335	2	RESISTOR 13K 5% .25W FC TC=-400/+800	01121	CB1335
A2R2	0683-1335		RESISTOR 13K 5% .25W FC TC=-400/+800	01121	CB1335
A2R3	1810-0263	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	28480	1810-0263
A2R4	0683-1825	1	RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
A2R5	1810-0269	2	NETWORK-RES 9-PIN-SIP .1-PIN-SPCG	28480	1810-0269
A2R6	0757-0406	1	RESISTOR 182 1% .125W F TC=0+-100	24546	C4-1/8-T0-182R-F
A2R7	0683-1525	5	RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A2R8	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R9	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A2R10	0683-0335	1	RESISTOR 3.3 5% .25W FC TC=-400/+500	01121	CB3305
A2R11	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A2R12	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A2R13	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A2R14, R15	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R16	0683-8215	1	RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
A2R17	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A2R18	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A2R19	0683-3045	1	RESISTOR 300K 5% .25W FC TC=-800/+900	01121	CB3045
A2R21	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A2R23	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R24	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R25	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R26	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R27	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R28	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035

Δ1, 2 See note on schematic 3.

Δ3 See note on schematic 2.

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2R29	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R31	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R32	1810-0269		NETWORK-RES 9-PIN-SIP .1-PIN-SPCG	28480	1810-0269
A2R33	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R34	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R35	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R36	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R37	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R38	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A2R100	0698-3519	1	RESISTOR 12.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1242-F
A2R101	0683-6215	2	RESISTOR 620 5% .25W FC TC=-400/+600	01121	CB6215
A2R102	0683-6215		RESISTOR 620 5% .25W FC TC=-400/+600	01121	CB6215
A2R103	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A2R104	0683-4735	1	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
A2R105	0683-5125		RESISTOR 5.1K 5% .25W FC TC=-400/+700	01121	CB5125
A2R106	0683-4715		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A2R107	0683-1005		RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A2R108	0683-9105	1	RESISTOR 91 5% .25W FC TC=-400/+500	01121	CB9105
A2R109	0683-3015	1	RESISTOR 300 5% .25W FC TC=-400/+600	01121	CB3015
A2R111	0757-0278	1	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A2R112	0698-4471	1	RESISTOR 7.15K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7151-F
A2R113	0698-4464	1	RESISTOR 887 1% .125W F TC=0+-100	24546	C4-1/8-TO-887R-F
A2R114	0683-1005		RESISTOR 10 5% .25W FC TC=-400/+500	01121	CB1005
A2R115	0683-3025		RESISTOR 3K 5% .25W FC TC=-400/+700	01121	CB3025
A2R116	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A2R117	0757-0280	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R118	0757-0280		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A2R119	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A2R120	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A2R121	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
A2R122	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R123	0683-6815		RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A2R124	0683-3625	1	RESISTOR 3.6K 5% .25W FC TC=-400/+700	01121	CB3625
A2R125	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R126	0683-3615	1	RESISTOR 360 5% .25W FC TC=-400/+600	01121	CB3615
A2R127	0683-3325		RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
A2R130	0683-2225		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A2R201	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R202	0683-2035	3	RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A2R203	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A2R204	0690-1511	1	RESISTOR 150 10% 1W CC TC=0+529	01121	GB1511
A2R205	0683-6815		RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A2R206	0683-1235	3	RESISTOR 12K 5% .25W FC TC=-400/+800	01121	CB1235
A2R207	0757-0442		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R208	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A2R209	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A2R211*	0683-999P		RESISTOR, FXD (PAD VALUE)	28480	0683-999P
A2R212	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R213	0698-4487	1	RESISTOR 25.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2552-F
A2R214	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R215	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R216	0683-2035		RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A2R217	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A2R218	0683-6815		RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A2R219	0683-1235		RESISTOR 12K 5% .25W FC TC=-400/+800	01121	CB1235
A2R221	0683-1345	1	RESISTOR 130K 5% .25W FC TC=-800/+900	01121	CB1345
A2R222	0683-1525		RESISTOR 1.5K 5% .25W FC TC=-400/+700	01121	CB1525
A2R223	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R224	0683-2035		RESISTOR 20K 5% .25W FC TC=-400/+800	01121	CB2035
A2R225	0683-1045		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A2R226	0683-6815		RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A2R227	0683-1235		RESISTOR 12K 5% .25W FC TC=-400/+800	01121	CB1235
A2R228	0683-0475		RESISTOR 4.7 5% .25W FC TC=-400/+500	01121	CB47G5
A2R229	0683-6825		RESISTOR 6.8K 5% .25W FC TC=-400/+700	01121	CB6825
A2R231	0683-1655	1	RESISTOR 1.6M 5% .25W FC TC=-900/+1100	01121	CB1655
A2R232	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R233	0683-2045	1	RESISTOR 200K 5% .25W FC TC=-800/+900	01121	CB2045
A2R234	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
A2R235	0683-2235		RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
A2R236	0683-1225		RESISTOR 1.2K 5% .25W FC TC=-400/+700	01121	CB1225
A2R238	0698-4469	1	RESISTOR 1.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1151-F
A2S1	3101-2094	1	SWITCH ASSEMBLY, ROCKER	28480	3101-2094

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2U1, U2	1820-1558	1	IC-DIGITAL MC3441P TTL* QUAD	04713	MC3441P
A2U3	1820-1491	7	IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U4	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U5	1820-1730	2	IC-DIGITAL SN74LS273N TTL LS OCTL	01295	58039
A2U6	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
A2U7	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U8	1820-1416	1	IC-DIGITAL SN74LS14N TTL LS HEX 1 INV	01295	SN74LS14N
A2U9	1820-0621	1	IC-DIGITAL SN7438N TTL QUAD 2 NAND	01295	SN7438N
A2U11	1820-1199	2	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A2U12	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
A2U13	1820-1197	3	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A2U14	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A2U15	1820-1210	3	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
A2U16	1820-1210		IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
A2U17	1820-0987	1	IC-DIGITAL 93L18PC TTL L 8	07263	93L18PC
A2U18	1820-1730		IC-DIGITAL SN74LS273N TTL LS OCTL	01295	58039
A2U19	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U21	1820-1492	3	IC-DIGITAL SN74LS368N TTL LS HEX 1 INV	01295	SN74LS368N
A2U22	1820-1197		IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
A2U23	1820-1206	2	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A2U24	03437-62503	1	NANOPROCESSOR ASSY(MATCHED SET A2U24-A2R237)	28480	03437-62503
A2U25	1820-1216	3	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A2U26	1820-1216		IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A2U27	1820-1216		IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
A2U28	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U29	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U31	1820-1491		IC-DIGITAL SN74LS367N TTL LS HEX 1	01295	SN74LS367N
A2U32	1820-1194	1	IC-DIGITAL SN74LS193N TTL LS BIN	01295	SN74LS193N
A2U33	1820-1198	1	IC-DIGITAL SN74LS03N TTL LS QUAD 2 NAND	01295	SN74LS03N
A2U34	1820-1470	1	IC-DIGITAL SN74LS157N TTL LS QUAD 2	01295	SN74LS157N
A2U35	1820-0628	2	IC SN74 89N 64-BIT RAM TTL	01295	SN7489N
A2U36	1820-1492		IC-DIGITAL SN74LS368N TTL LS HEX 1 INV	01295	SN74LS368N
A2U37	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A2U38	1820-1492		IC-DIGITAL SN74LS368N TTL LS HEX 1 INV	01295	SN74LS368N
A2U39	1820-0628		IC SN74 89N 64-BIT RAM TTL	01295	SN7489N
A2U41	1816-1023	1	PROGRAM, PROM (BI-POLAR)	28480	1816-1023
A2U42	1816-1026	1	PROGRAM, PROM (BI-POLAR)	28480	1816-1026
A2U43	1816-1027	1	PROGRAM, PROM (BI-POLAR)	28480	1816-1027
A2U44	1816-1024	1	PROGRAM, PROM (BI-POLAR)	28480	1816-1024
A2U45	1820-1273	1	IC-DIGITAL SN74LS28N TTL LS QUAD 2 NOR	01295	SN74LS28N
A2U47	1820-1328	1	IC-DIGITAL MC14526CP CMOS BIN	04713	MC14526CP
A2U48	1820-0978	1	IC-DIGITAL CD4007AE CMOS DUAL	02735	CD4007AY
A2U49	1820-1212	2	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
A2U51	1820-1415	1	IC-DIGITAL SN74LS13N TTL LS DUAL 4 NAND	01295	SN74LS13N
A2U52	1820-0806	1	IC-DIGITAL MC10109P ECL DUAL 4-5 OR-NOR	04713	MC10109P
A2U100	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
A2U101	1820-1729	4	IC-DIGITAL SN74LS259N TTL LS COM	01295	SN74LS259N
A2U102	1820-1729		IC-DIGITAL SN74LS259N TTL LS COM	01295	SN74LS259N
A2U103	1820-1729		IC-DIGITAL SN74LS259N TTL LS COM	01295	SN74LS259N
A2U104	1820-1729		IC-DIGITAL SN74LS259N TTL LS COM	01295	SN74LS259N
A2U105	1820-1279	7	IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U106	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U107	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U108	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U109	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U111	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U112	1820-1279		IC-DIGITAL SN74LS190N TTL LS DECD	01295	SN74LS190N
A2U113	1820-1207	1	IC-DIGITAL SN74LS30N TTL LS 8 NAND	01295	SN74LS30N
A2U114	1820-1144	1	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
A2U115	1820-1210		IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
A2U116	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
A2U117	1820-1425	1	IC-DIGITAL SN74LS132N TTL LS QUAD 2 NAND	01295	SN74LS132N
A2U118	1820-1282	1	IC-DIGITAL SN74LS109N TTL LS DUAL	01295	SN74LS109N
A2U119	1820-1423	1	IC-DIGITAL SN74LS123N TTL LS DUAL	01295	SN74LS123N
A2U121	1820-0693	1	IC-DIGITAL SN74S74N TTL S DUAL	01295	SN74S74N
A2U122	1906-0070	1	DIODE-ARRAY	28480	1906-0070
A2U123	1820-0125	1	IC UA 711C COMPARATOR	07263	711HC
A2U124	1820-1212		IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
A2U201	1826-0345	1	IC 78M12 V RGLTR	07263	UA78M12UC
A2U202	1820-0439	1	IC UA 723C V RGLTR	07263	723PC
A2U203	1826-0346	1	IC LM 358 OP AMP	27014	LM358N
A2Y1	0410-1011	1	CRYSTAL, QUARTZ	28480	0410-1011

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			A2 MISCELLANEOUS		
	0340-0060		TERMINAL-STUD SPCL-FDTHRU PRESS-MTG	98291	FT-E-15
	03437-01211	1	STRAINER CLAMP	28480	03437-01211
	0360-0693	3	BUS BAR	28480	0360-0693
	0360-0694	1	BUS BAR	28480	0360-0694
	0360-0695	3	BUS BAR	28480	0360-0695
	5040-1449		HINGE	28480	5040-1449
XU24	1200–0466		MPU SOCKET	28480	1200–0466
A3	03437-69301	1	FRONT PANEL ASSEMBLY	28480	03437-69301
A3A1	03437-66503	1	P.C. ASSEMBLY	28480	03437-66503
A3A1C1	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A3A1C2	0180-0106	1	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A3A1C3	0150-0121		CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
A3A1DS1	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS2	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS3	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS4	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS5	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS6	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS7	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS8	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS9	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS11	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS12	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS13	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS14	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS15	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS16	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS17	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS18	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS19	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS21	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS22	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1DS23	1990-0486		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	1990-0486
A3A1Q1	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q2	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q3	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q4	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q5	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q6	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q7	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q8	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q9	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q11	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q12	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q13	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q14	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q15	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q16	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1Q17	1854-0730		TRANSISTOR NPN SI TO-92	28480	1854-0730
A3A1R1	1810-0164	1	NETWORK-RES 9-PIN-SIP .15-PIN-SPCG	28480	1810-0164
A3A1R2	0683-8205	8	RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R3	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R4	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R5	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R6	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R7	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R8	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R9	0683-8205		RESISTOR 82 5% .25W FC TC=-400/+500	01121	CB8205
A3A1R10	0683-1025	9	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3A1R11	0683-1025		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A3A1R12	0683-3305	5	RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
A3A1R13	0683-3305		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
A3A1R14	0683-3305		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
A3A1R15	0683-3305		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
A3A1R16	0683-3305		RESISTOR 33 5% .25W FC TC=-400/+500	01121	CB3305
A3A1R17	0683-3915		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A3A1R18	0683-3915		RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A3A1R19	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3A1R21	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3A1R22	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A3A1R23	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3A1R24	0683-1035		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A3A1U1	1816-1025	1	PROGRAM, PROM (BI-POLAR)	28480	1816-1025
A3A1U2	1858-0048	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	02735	CA3082
A3A1U3	1820-1683	1	IC-DIGITAL MC14514CP CMOS	04713	MC14514CP
A3A2	1990-0589	1	DISPLAY MONOLITHIC	28480	1990-0589
A3A3	5060-9436	1	PUSHBUTTON SWITCH	28480	5060-9436
A3A4	03437-00202	1	FRONT SUB-PANEL	28480	03437-00202
			CHASSIS MOUNTED PARTS		
Q1	1853-0059	1	TRANSISTOR PNP 2N3791	04713	2N3791
Q2	1853-0233	1	TRANSISTOR PNP SI PD = 40W FT = 3 MHZ	28480	1853-0233
C1	0180-0459	1	CAPACITOR-FXD 9100UF +75 -10% 12VDC AL	28480	0180-0459
C2	0160-0170		CAPACITOR-FXD .22UF +80 -20% 25WVDC CER	28480	0160-0170
C3, C4	0160-0174	2	CAPACITOR-FXD .47UF +80 -20% 25WVDC CER	28480	0160-0174
CR1, CR2	1901-0592	2	DIODE-PWR RECT 100V 12A DO-4	04713	MR1121R
CR3	1902-0902	1	DIODE, 1N2974A (10V ZENER)	07263	1N2974A
E1, E2	1970-0076	2	SURGE, V-PROTECT	28480	1970-0076
FL1	9135-0035	1	LINE FILTER	28480	9135-0035
J1	1250-0687	2	CONNECTOR-RF TRAXL FEM SGL HOLE RR	28480	1250-0687
J2, J3	1250-0083	2	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	24931	28JR-130-1
J4	1250-0687	2	CONNECTOR-RF TRAXL FEM SGL HOLE RR	28480	1250-0687
M1 03455-89801	~~3160-0266~~	1	FAN-TBAX DCV	28480	3160-0266
S1	3101-1720	1	SWITCH-PB DPDT 4A 250VAC	28480	3101-1720
W2	03437-61604	1	CABLE ASSEMBLY, 6P TRANSFORMER	28480	03437-61604
W3	03437-61605	1	CABLE ASSEMBLY, 4P FAN	28480	03437-61605
W4	03437-61606	1	CABLE ASSEMBLY, 6P HEAT SINK	28480	03437-61606
W5	03437-61601	1	CABLE ASSEMBLY, 10P	28480	03437-61601
	03437-61607	1	CABLE ASSEMBLY, (SERIAL CODE - A1 BOARD)	28480	03437-61607
W6	03437-61603		CABLE ASSEMBLY, (28P)	28480	03437-61603
W7	03437-61612	1	CABLE ASSEMBLY, HP-IB	28480	03437-61612
W8, W9	03437-61610	2	CABLE ASSEMBLY, DBL TRIA	28480	03437-61610
W10, W11	03437-61611	2	CABLE ASSEMBLY, TWIST	28480	03437-61611
			MECHANICAL PARTS		
	03437-01110	1	HEAT SINK	28480	03437-01110
	03437-01201	2	GUARD SUPPORT BRACKET	28480	03437-01201
	03437-01202	2	TRANSISTOR BRACKET	28480	03437-01202
	03437-01203	1	BAFFLE	28480	03437-01203
	03437-01204	1	BRACKET, LINE SWITCH	28480	03437-01204
	03437-04101	1	TOP OK COVER	28480	03437-04101
	03437-04111	1	BOTTOM GUARD COVER	28480	03437-04111
	5060-9843	1	BOTTOM COVER	28480	5060-9843
	03437-04301	1	PANEL, FRONT	28480	03437-04301
	03437-00212	1	PANEL, REAR	28480	03437-00212
	03437-29301	1	WINDOW, RIGHT	28480	03437-29301
	03437-29302	1	WINDOW, LEFT	28480	03437-29302
	03437-61613	1	TRIAX INPUT CABLE (TEST)	28480	03437-61613
	03437-00601	1	SAFETY SHIELD	28480	03437-00601
	2360-0316	10	SCREW-MACH 6-32 .25-IN-LG 100 DEG	28480	2360-0316
	2200-0521	6	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI	28480	2200-0521
	0380-0060	3	SPACER-RND .188LG .114ID .1540D STL	76854	8980-412
			MISCELLANEOUS PARTS		
	03437-90010	1	OPERATING MANUAL	28480	03437-90010
	03437-90002		OPERATING & SERVICE MANUAL	28480	03437-90002
	1200-0634	1	24 PIN SOCKET (A2U41)	28480	1200-0634
	0340-0486	1	INSULATOR-COVER TO- 3 .33 - THK	0011J	A22-2003
	0340-0566	1	INSULATOR-XSTR TO- 66 .011 - THK	28480	0340-0566
	2110-0465	1	FUSEHOLDE-EXTR POST UL/IEC .25 X 1.25 FUSE	28480	2110-0465
	2110-0467	1	NUT, HEX SINGLE CHAMFER 1/2 - 28 THREAD	75915	903-070
	2110-0470	1	FUSEHOLDER-EXTR POST 20A 200V UL/IEC	75915	345003-010
	3150-0300	1	FILTER, AIR	28480	3150-0300
	5001-0438	2	TRIM STRIP	28480	5001-0438
	5040-7201	4	FOOT (STANDARD)	28480	5040-7201
	5040-7203	1	TRIM : TOP 1/2	28480	5040-7203
	5040-7675	1	PUSHROD, SWITCH	28480	5040-7675
	5041-0531	1	KEY CAP-S.M., GRAY	28480	5041-0531
	5041-0309	2	KEY CAP-PTY, GRAY	28480	5041-0309
	5041-0318	8	KEY CAP-PTY, GRAY	28480	5041-0318
	5041-0450	3	KEY CAP-L SEABLU	28480	5041-0450
	5061-0076	1	CABINET ASSY	28480	5061-0076
	5061-0086	1	CABINET ASSY	28480	5061-0086
	5061-0088	1	FR. HANDLE KIT	28480	5061-0088

See introduction to this section for ordering information

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	5060–9831	1	*TOP COVER	28480	5060–9831
	5060–9907	2	*SIDE COVER	28480	5060–9907
	8120–1348	1	CABLE – AC POWER	28480	8120–1348
T1	9100–0698	1	TRANSFORMER (W1 INCLUDED)	28480	9100–0698
	7120–3185	1	LABEL, WARNING	28480	7120–3185

See introduction to this section for ordering information

SECTION VII
CIRCUIT DIAGRAMS

7-1. INTRODUCTION.

7-2. This section contains circuit diagrams, tables describing the 3437A Interrupt requests and logic messages, and an alphabetical listing of 3437A mnemonics.

Table 7-1. Circuit Diagrams.

Title	Designators	Figure	Diagram Number
Functional Block Diagram	–	7 - 1	–
Analog Measurement Circuitry	A1 (0 - 99 Series)	7 - 2	1
Outguard Logic	A2 (0 - 99 Series)	7 - 3	2
Delay Logic	A2 (100 - 199 Series)	7 - 4	3
Display	A3 (0 - 99 Series)	7 - 5	4
Power Supplies	A1/A2 (200-299 Series)	7 - 6	5

Table 7-2. 3437A Logic Messages.

ATL	Addressed to Listen
ATN	Attention
ATT	Addressed to Talk
DAC	Data Accepted
DAV	Data Valid
RFD	Ready for Data
EAI	Enable Attention Interrupt
EOI	End or Identify
IFC	Interface Clear
LOT	Local Lock-Out
NBA	Next Byte Available
SPM	Serial Poll Mode
REM	Remote
REN	Remote Enable

T or F preceeding Mnemonic Indicates Message Status.

Table 7-3. 3437A Interrupt Requests.

Mnemonic	Description	Source
LIFC	Interface Clear	U16 (6)
LREF	Remote False	U13A (3)
LVTG	Valid Trigger	U124 (6)
LATN	Attention	U115 (6)
LSHS	Source Handshake	U15 (8)
LASH	Acceptor Handshake	U16 (8)
LITG	Ignored Trigger	U118A (7)

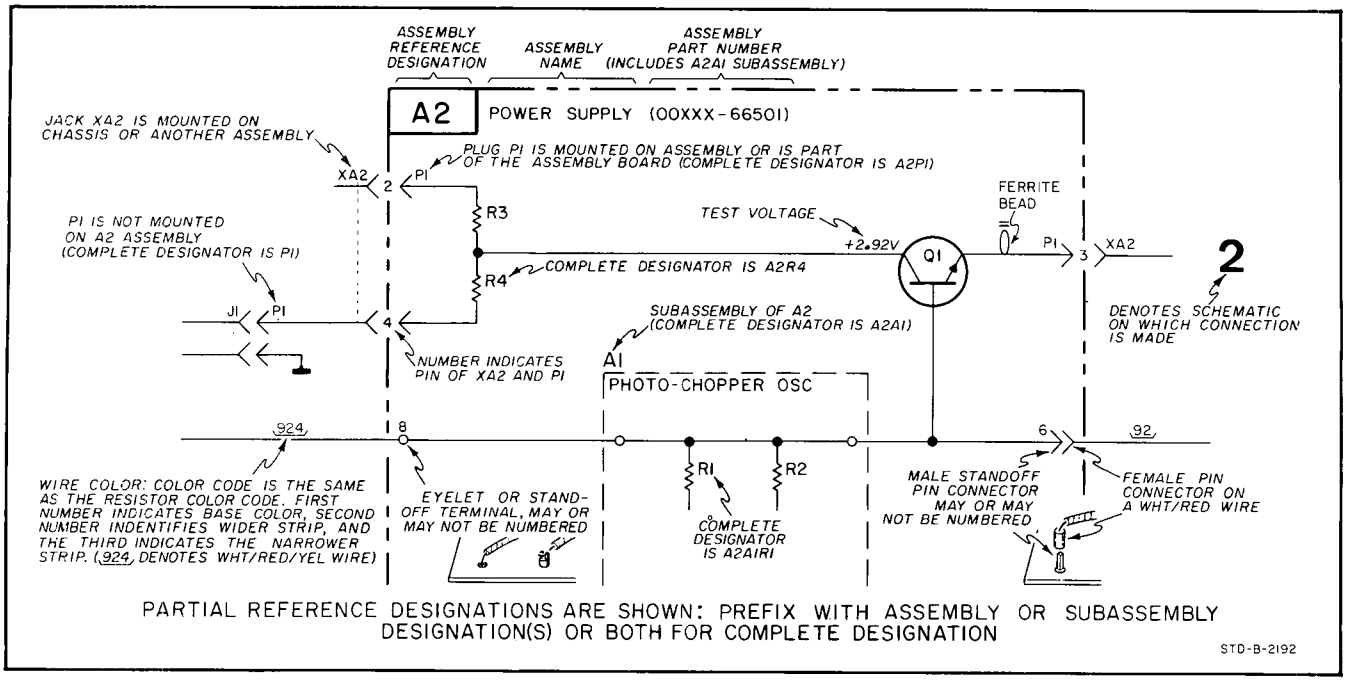
Interrupt Request are Low True.

Table 7-4. 3437A Mnemonics.

Mnemonic	Description	Source
LPADS	Processor Annunciator and Digit Scan	U47
LPATL	Processor Addressed to Listen	U6 (10)
LBATN	Bus Attention	HP-IB (11)
LPATT	Processor Addressed to Talk	U6 (2)
LPDEN	Processor Display Enable	(DS17)/U25 (7)
HPCSD	Processor Coded Serial Data	A1U17 (5)/U18 (5)
HBDAC	Bus Data Accepted	HP-IB (8)
HPDAC	Processor Data Accepted	MPU (32)
LBDAV	Bus Data Valid	HP-IB (6)
LPDAV	Processor Data Valid	MPU (34)
HPEAI	Processor Enable Attention Interrupt	MPU (35)
HPEOI	Processor End or Identify	MPU (37)
LBIFC	Bus Interface Clear	HP-IB (9)
LPKBD	Processor Keyboard Data	Keyboard
LPKBS	Processor Keyboard Scan	U33
LPLOT	Processor Local Lockout	U6 (5)
HPNBA	Processor Next Byte Available	U14C (8)
HPNRG	Processor Number of Readings > 1	U100 (15)
LPNRG	Processor Number of Readings > 1	U100 (14)
LPRBØ	Processor Range Bit Zero	U100 (6)
LPRB1	Processor Range Bit One	U100 (3)
LPREM	Processor Remote	U6 (7)
LBREN	Bus Remote Enable	HP-IB (17)
HBRFD	Bus Ready for Data	HP-IB (7)
HPRFD	Processor Ready for Data	MPU (33)
HPSPM	Processor Serial Poll Mode	U6 (12)
HPSRQ	Processor Service Request	U6 (15)
HPTEN	Processor Trigger Enable	U100 (11)

L or H preceeding Mnemonic indicates Low-True or High-True active logic level.

REFERENCE DESIGNATIONS



PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION

GENERAL SCHEMATIC NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY OR SUBASSEMBLY DESIGNATION(S) OR BOTH FOR COMPLETE DESIGNATION.

2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN MILLIHENRYS

3. DENOTES EARTH GROUND. USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GAUGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OR AC POWER RECEPTACLE.

4. DENOTES FRAME GROUND. USED FOR TERMINALS WHICH ARE PERMANENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.

5. DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY. (PERMANENTLY CONNECTED TO FRAME GROUND).

6. DENOTES ASSEMBLY

7. DENOTES MAIN SIGNAL PATH.

9. DENOTES FEEDBACK PATH.

10. DENOTES FRONT PANEL MARKING.

11. DENOTES REAR PANEL MARKING.

12. DENOTES SCREWDRIVER ADJUST.

13. * AVERAGE VALUE SHOWN, OPTIMUM VALUE SELECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTRUMENT TO ANOTHER. THE METHOD OF SELECTING THESE COMPONENTS IS DESCRIBED IN SECTION V OF THIS MANUAL.

14. DENOTES SECOND APPEARANCE OF A CONNECTOR PIN.

15. 924 DENOTES WIRE COLOR: COLOR CODE SAME AS RESISTOR COLOR CODE. FIRST NUMBER IDENTIFIES BASE COLOR, SECOND NUMBER IDENTIFIES WIDER STRIP, THIRD NUMBER IDENTIFIES NARROWER STRIP. (e.g. 924 = WHITE, RED, YELLOW.)

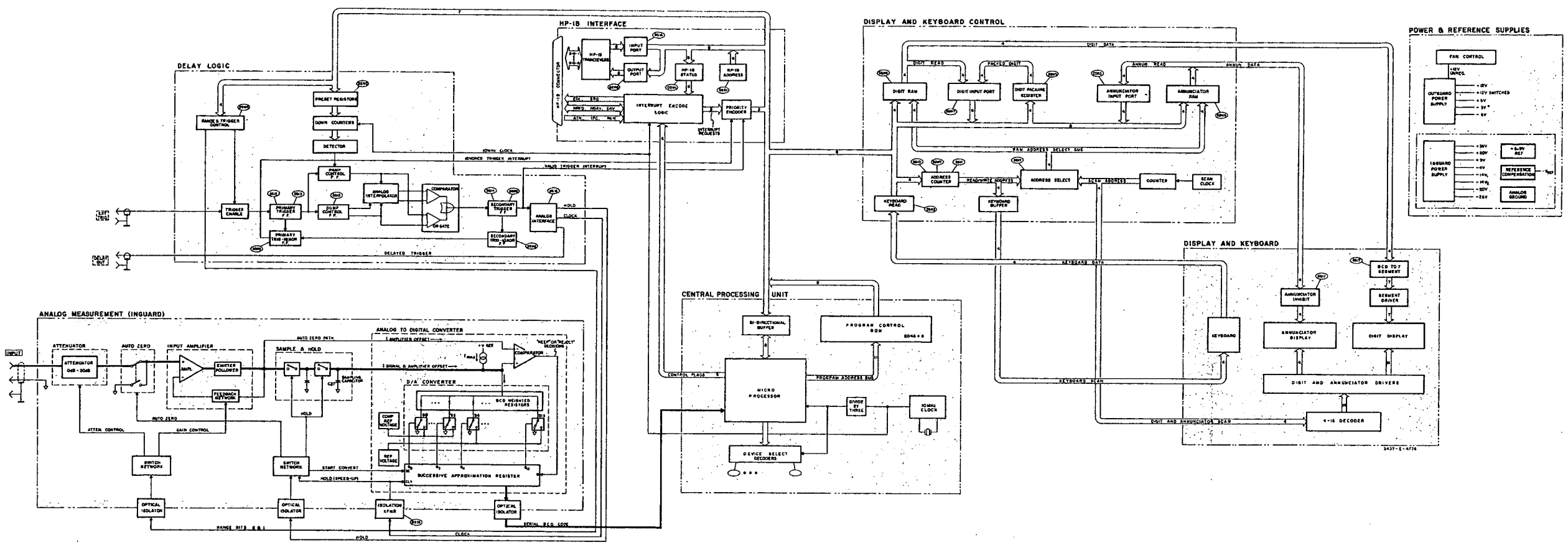
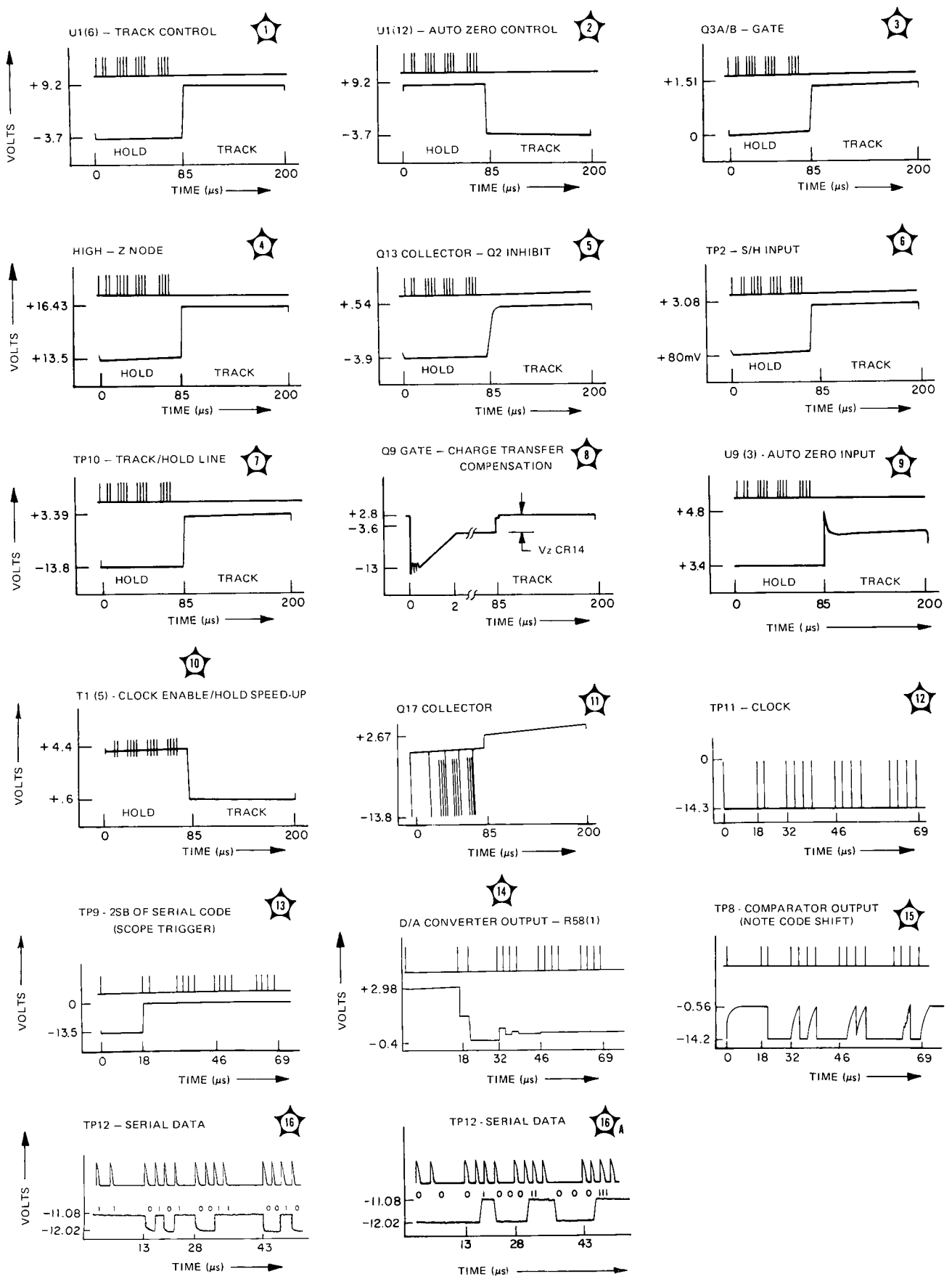
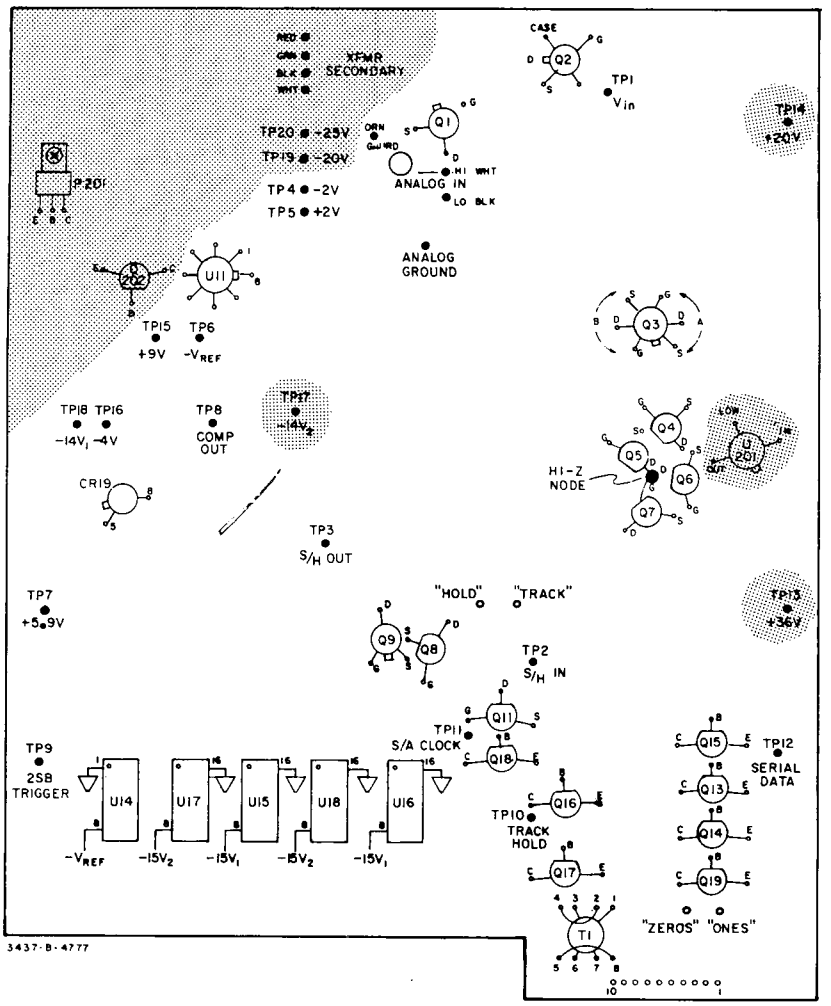


Figure 7-1. 3437A Functional Block Diagram.



p/o Figure 7-2. Analog Circuit Diagram Test Waveforms.



NOTE

1. *DC VOLTAGES WERE MEASURED UNDER THE FOLLOWING CONDITIONS:*

DELAY	*200 µs*
NRDGS	*9999*
RANGE	*1 volt*
TRIGGER	*INTERNAL*
INPUT	*+ 1.532 volts*

2. *CONTROL VOLTAGE (U1 AND U6)*

CLOSED	*+ 9 V (TYPICAL)*
OPEN	*– 4 V (TYPICAL)*

3. *IC SUPPLY VOLTAGE*

PINS	*+ 5 V*	*GND*
16	*16*	*8*
14	*14*	*7*

4. *LOGIC LEVELS (U14 – U18)*

LOW	*– 14 V*
HIGH	*0 V*

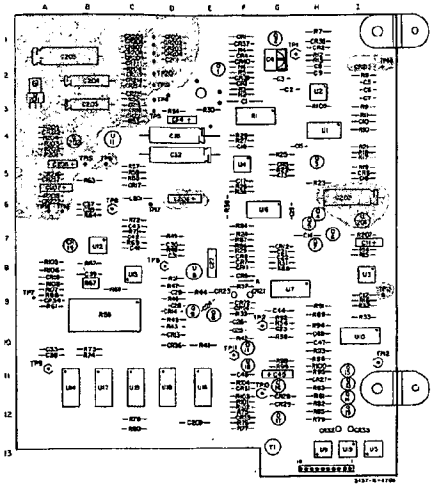
5. *VOLTAGES ARE MEASURED IN RESPECT TO OUTGUARD GROUND.*

6. *WAVEFORMS WERE OBTAINED UNDER THE FOLLOWING CONDITIONS:*

DELAY	*200 µs*
NRDGS	*9999*
RANGE	*1 Volt*
TRIGGER	*INT*
INPUT	*+1.532 VDC*

TRIGGER OSCILLOSCOPE FROM TP9.

p/o Figure 7-2. Analog Board Component Pin-Out.



Δ_1 FOR SERIAL NUMBERS GREATER THAN 1630A00165, C36 WAS CHANGED FROM PART NUMBER 0160-3847 (.01 µF) TO IMPROVE NOISE FILTERING ON THE −14 VOLT SUPPLY. C20* WAS ADDED TO IMPROVE STEP RESPONSE BY SPEEDING UP Q2 TURN-OFF. TP1 WAS REMOVED WITH THIS CHANGE.

Δ_2 FOR SERIAL NUMBERS GREATER THAN 1630A00270, C50 WAS ADDED TO SHUNT NOISE FROM THE INPUT TO U6 (PIN 5).

Δ_3 FOR SERIAL NUMBERS GREATER THAN 1630A00470, C44 WAS CHANGED FROM PART NUMBER 0180-0398 (7 µF) TO A COMPONENT WITH A HIGHER WORKING VOLTAGE.

Δ_4 FOR SERIAL NUMBERS GREATER THAN 1630A00220, Q2 WAS CHANGED FROM PART NUMBER 1855-0368 TO PROVIDE A PINCH-OFF VOLTAGE < −4 VOLTS @ 1 µa CURRENT WITHOUT HAND SELECTION.

Δ_5 FOR SERIAL NUMBERS GREATER THAN 1630A00194, C11 WAS CHANGED FROM PART NUMBER 0180-1701 (5.8 µF) TO FACILITATE QP TEST.

Δ_6 FOR SERIAL NUMBERS GREATER THAN 1630A00135, CR12 WAS CHANGED FROM PART NUMBER 1920-2206 (15 V) TO MAINTAIN LINEAR OPERATION OF THE INPUT AMPLIFIER.

Δ_7 FOR SERIAL NUMBERS GREATER THAN 1630A00670, C60 WAS ADDED. C20* WAS DELETED. R7 WAS CHANGED FROM PART NUMBER 0683-1045 (100 K), AND C25 WAS ADDED TO ELIMINATE STORAGE EFFECTS DESCRIBED IN Δ_1. C20* IS NO LONGER NEEDED.

Δ_8 FOR SERIAL NUMBERS GREATER THAN 1630A00670, R119 WAS ADDED TO ALLOW THE CHANGE IN R91 FROM PART NUMBER 0683-3035 (30 K) AND THE ADDITION OF C81 FOR NOISE PURPOSES.

Δ_9 FOR SERIAL NUMBERS GREATER THAN 1630A00670, R96 WAS ADDED TO EQUALIZE PROPAGATION DELAY TO U1, PINS 6 AND 12.

Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location
C1	3F	C31	8D	CR8	6I	CR35	10D	D11	10F	R31	4I	R51	8D	R81	11H	T1	13G
C2	3G	C32	4D	CR9	6F	CR37	1F	D12	11I	R32	5G	R52	3C	R82	12H	T71	1G
C3	2G	C33	10A	CR10	6F	CR38	1H	D13	11I	R33	5H	R53	3C	R83	11H	TP2	10F
C4	2C	C34	3D	CR11	6F	CR39	1F	D14	11I	R34	7F	R54	3D	R84	6F	TP3	8D
C5	2I	C35	4D	CR12	7G	CR40	1F	D15	11I	R35	4G	R55	6C	R85	12H	TP4	3D
C6	3I	C36	10A	CR13	10D	CR41		Q16	11G	R36	6F	R56	6C	R86	1F	TP5	3C
C7	3H	C37	6B	CR14	9D	CR42		Q17	12G	R37	4F	R57	6C	R87	1F	TP6	5B
C8	2H	C38	6B	CR15	3C	CR43		Q18	11F	R38	4F	R58	9B	R88	6G	TP7	5A
C9	7H	C39	8B	CR16	3C	CR44		Q19	12H	R39	7F	R59	3C	R89	9H	TP8	6B
C10		C40		CR17	8A	CR45		Q20		R40		R60		R90		TP9	11A
C11	7I	C41	7C	CR18	8A	CR46		R1	3F	R41	8D	R61	8A	R91	9H	TP10	11F
C12	9I	C42	7C	CR19	8B	CR47		R2	3F	R42	8I	R62	8B	R92	9G	TP11	10F
C13	9G	C43	7C	CR20		CR48		R3	3F	R43	8I	R63	10H	R93	10H	TP12	7D
C14	7H	C44	9C			CR49		R4	1F	R44	8B	R64	8B	R94	11H	U1	1H
C15	8G	C45	11G	CR21	9F	CR50		R5	2F	R45	8F	R65	8B	R95	11H	U2	2H
C16	9I	C46	11G	CR22	9F	CR51		R6	2F	R46	6A	R66	8A	R96	10H	U3	8I
C17	8F	C47	10H	CR23	9F	CR52		R7	1H	R47	8H	R67	9B	R97		U4	9F
C18	8F	C48	10H	CR24	9F	CR53		R8	2I	R48	10G	R68	9B	R98	11G	U5	12I
C19	8G	C49		CR25	9F	CR54		R9	3I	R49	9F	R69	7C	R99	11G	U6	9D
C20		C50		CR26		CR55		R10	4I	R50		R70		R100		U7	9G
C21	7G	C51		CR27	11H	D1	7E	R11	3I	R51	10E	R71	7C	R101	11F	U8	8D
C22	8G	C52		CR28	11G	D2	1G	R12	1H	R52	10E	R72	8C	R102	11F	U9	13H
C23	10G	C53		CR29	11G	D3	6H	R13	1H	R53	10D	R73	10B	R103	11F	U10	13H
C24	9E	C54		CR30	10G	D4	6H	R14	8I	R54	9E	R74	10B	R104	11F	U11	4C
C25	10F	C55		CR31		D5	6H	R15	8I	R55	9D	R75	12F	R105	9A	U12	7B
C26	10F	C56	1F	CR32	11F	D6	7H	R16	8I	R56	9D	R76	12F	R106	9A	U13	8C
C27	8E	C57	1H	CR33	12H	D7	7H	R17	4I	R57	9D	R77	12F	R107	9A	U14	11A
C28	9D	C58	2F	CR34	9A	D8	8E	R18	4I	R58	7D	R78	12C	R108	9A	U15	11C
C29	9D	C59	1F	CR35	9A	D9	8D	R19	5I	R59	7D	R79	12C	R109	3H	U16	12B
C30	7D	C60	6C	CR36	12F	D10		R20		R60		R80	12C	R110		U17	11D
																U18	11D
																U19	13H

3437-B-4766

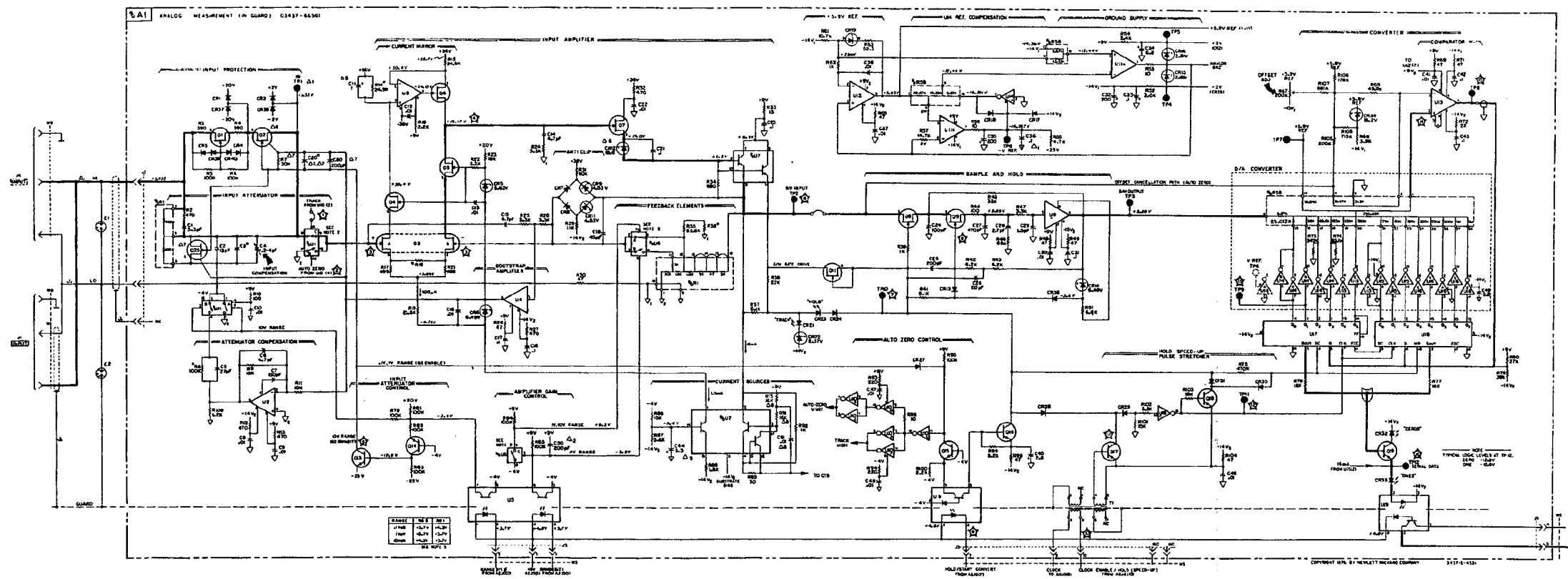


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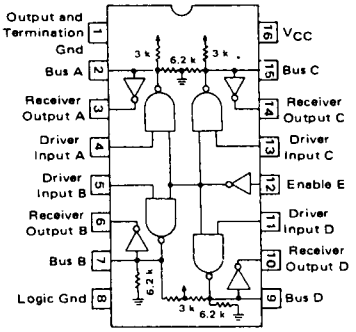
Figure 7-2. Analog Measurement (Inguard) Circuit Diagram and Component Locator.

Rev. A 7-7/7-8

OUTGUARD LOGIC IC FUNCTION TABLES

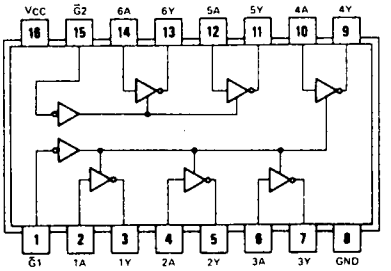
U1 – U2



U21 – U36 – U38

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

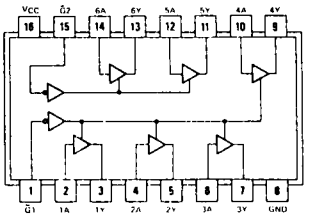
H = high level, L = low level,
X = irrelevant, Z = high-impedance



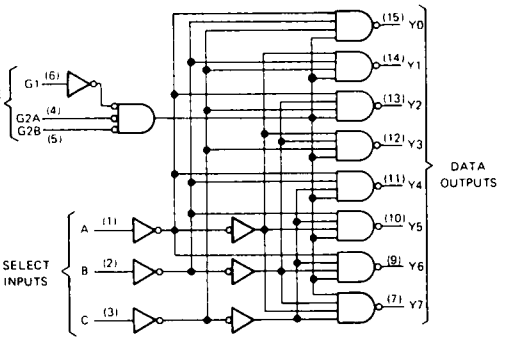
U3 – U4 – U7 – U19 – U28 – U29 – U31

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

H = high level, L = low level,
X = irrelevant, Z = high-impedance



U25 – U26 – U27



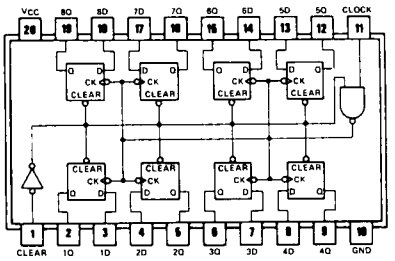
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

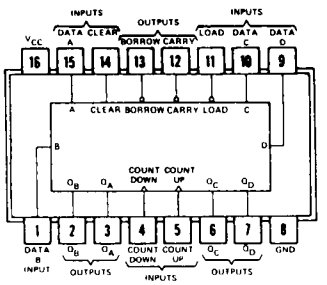
U5 – U18

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.



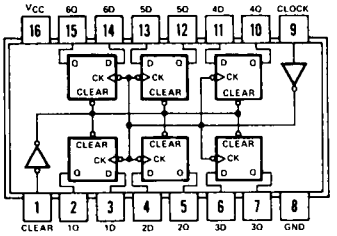
U32



logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

U6

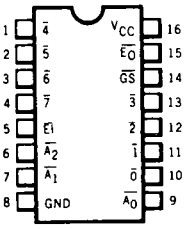
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$ ↑
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$



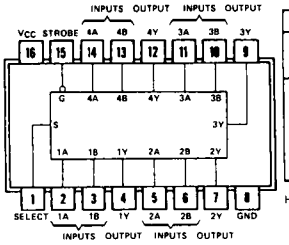
U17

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



U34



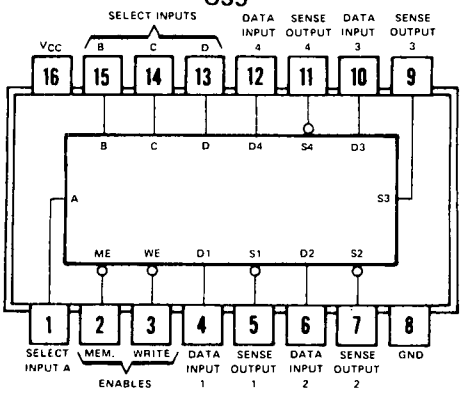
positive logic:
Low level at S selects A inputs
High level at S selects B inputs

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

OUTGUARD LOGIC IC FUNCTION TABLES

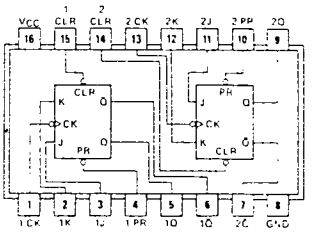
U35



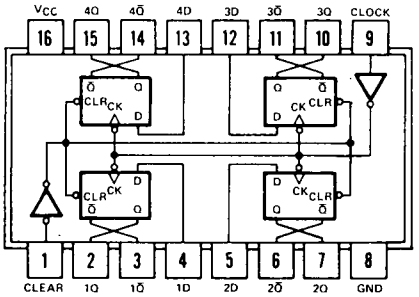
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

U49

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	Q_0



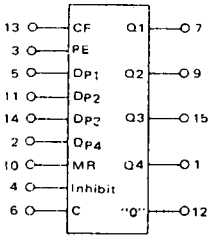
U37



INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

U47

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
↗	0	0	0	Count-1
X	1	0	0	No Count
1	↘	0	0	Count-1
X	X	1	0	Preset
X	X	X	1	Reset

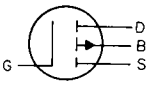


V_{DD} = Pin 16
V_{SS} = Pin 8

Count	Output			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

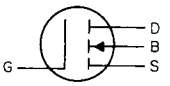
U48 CHARACTERS

PMOS (ENHANCEMENT)



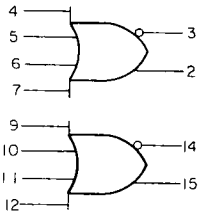
A NEGATIVE VOLTAGE APPLIED TO THE GATE WITH RESPECT TO THE SOURCE ESTABLISHES A PATH FOR HOLE CONDUCTION.

NMOS (ENHANCEMENT)



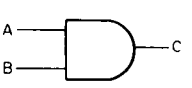
A POSITIVE VOLTAGE APPLIED TO THE GATE WITH RESPECT TO THE SOURCE ESTABLISHES A PATH FOR ELECTRON CONDUCTION.

U52

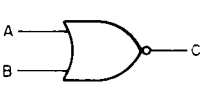


Vcc_1 = 1
Vcc_2 = 2
VEE = 8

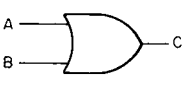
GENERAL



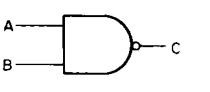
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



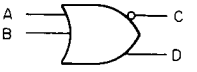
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



A	B	C	D
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

NOTE

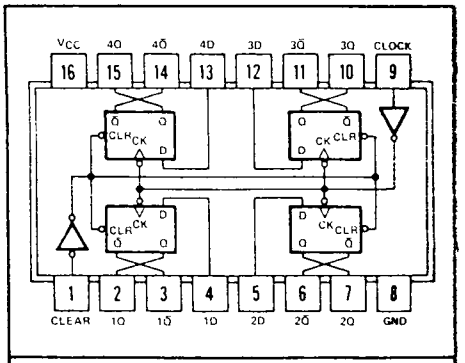
IC SUPPLY VOLTAGE

PINS	*+5*	*GND*
24	*24*	*12*
20	*20*	*10*
16	*16*	*8*
14	*14*	*7*

OUTGUARD LOGIC IC FUNCTION TABLES

U100

(TOP VIEW)



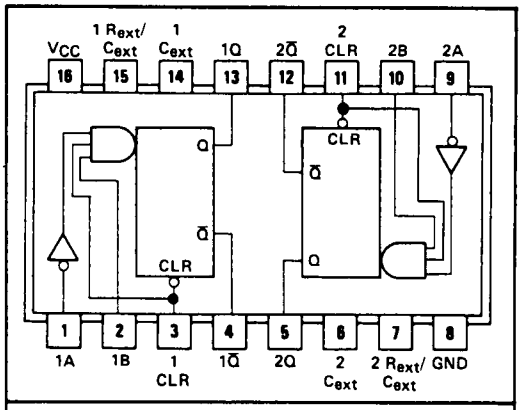
positive logic: see function table

(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

U119

(TOP VIEW)



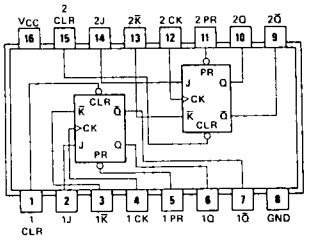
logic: see function table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

U118

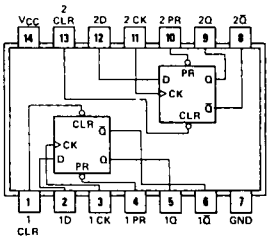
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K̄	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\bar{Q}_0$



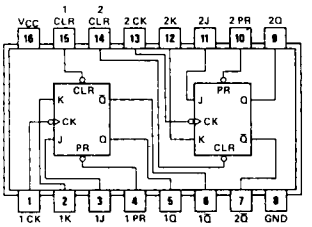
U121

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

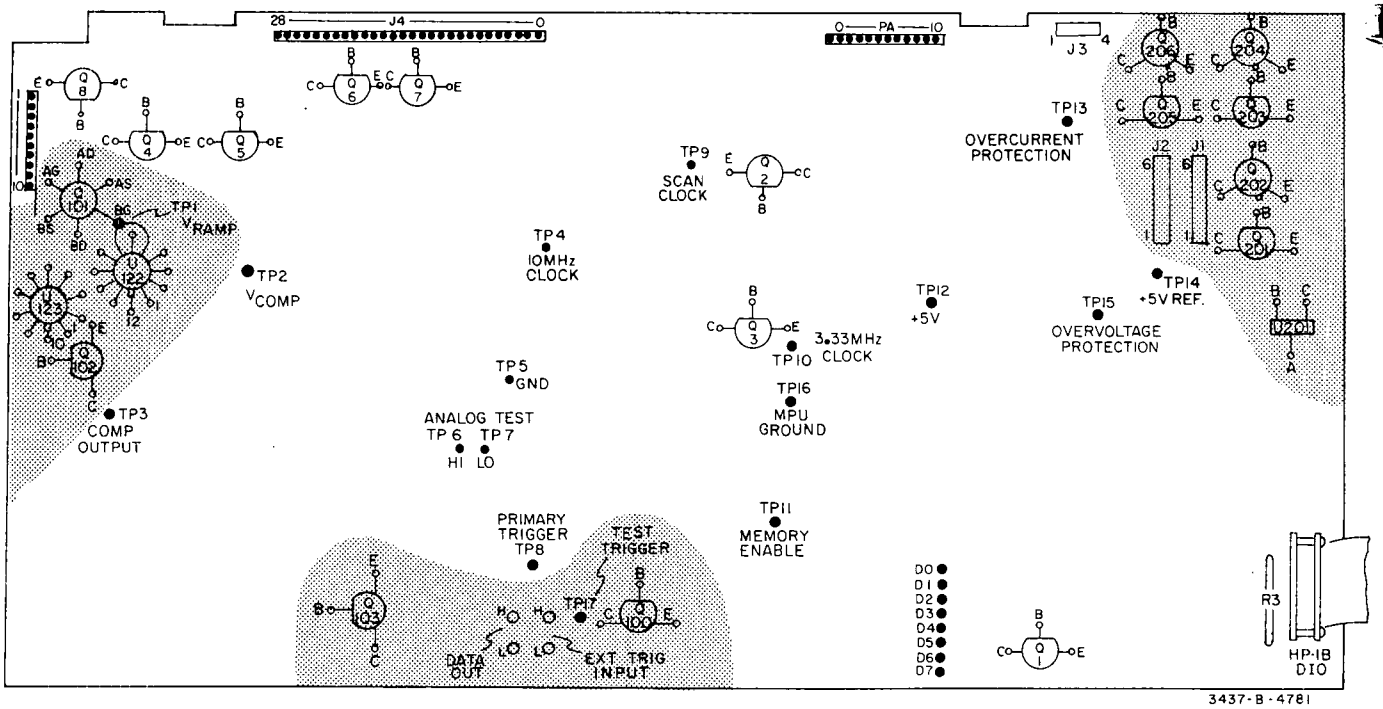


U124

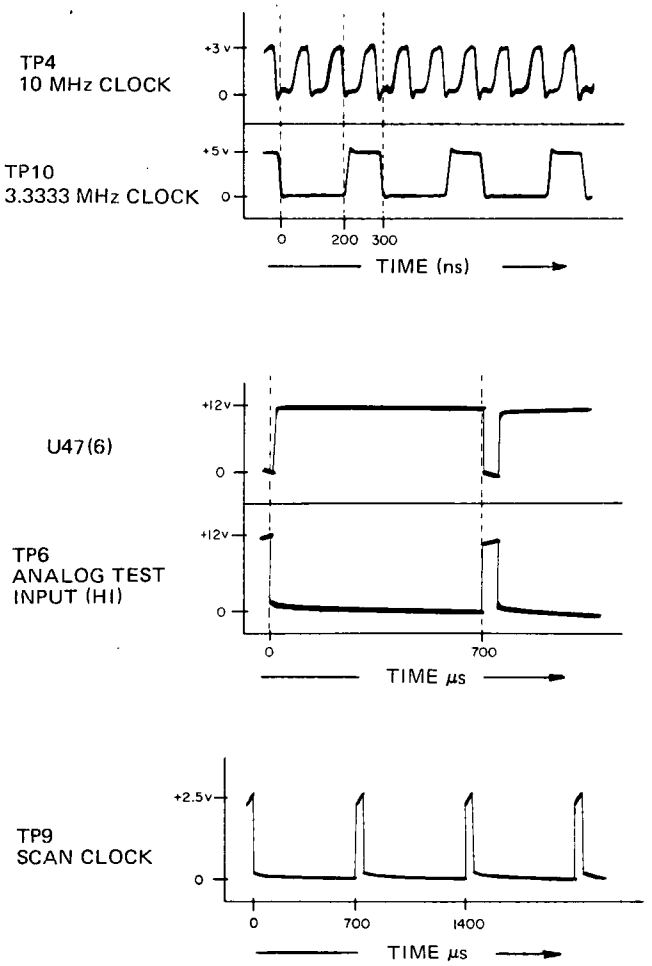
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



TRANSISTOR AND TEST POINT PIN–OUT (TOP VIEW)



TEST WAVEFORMS (TYPICAL VALUES)



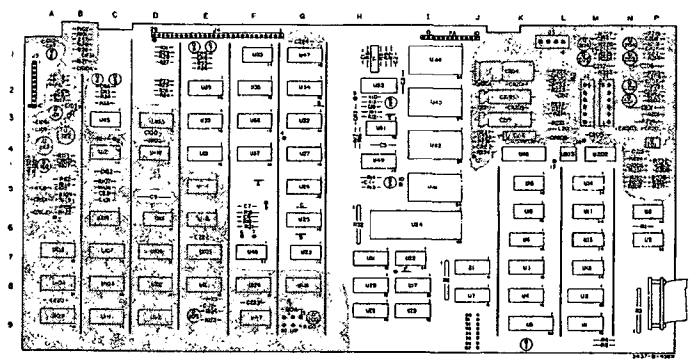
NOTE

All designators are prefixed A2 unless otherwise noted.

Device Select Outputs

From A2	To A2
DSR1 U26 - 14	U7 1 & 15/U3 - 1
DSR2 U26 - 13	U21 - 1
DSR3 U26 - 12	U38 - 1
DSR5 U26 - 10	U124A - 4
DSR6 U26 - 9	U118 - 1/U124B - 14
DSR7 U26 - 7	U36 - 1 & 15/U38 - 5
DSWØ U27 - 15	U5 - 11
DSW1 U27 - 14	U6 - 9
DSW2 U27 - 13	U101-14/U102-14/U103-14/U104-14
DSW3 U27 - 12	U37 - 9
DSW4 U27 - 11	U100 - 9
DSW5 U27 - 10	U39 - 3
DSW6 U27 - 9	U35 - 3
DSW7 U27 - 7	U32 - 11
DS1Ø U25 - 15	U32 - 5
DS11 U25 - 14	U32 - 4
DS12 U25 - 13	U119B - 9/U121A - 4
DS13 U25 - 12	U118B - 11
DS14 U25 - 11	U124A - 15
DS15 U25 - 10	R127 & C113
DS16 U25 - 9	U3 - 15/U4 - 1 & 15
DS17 U25 - 7	U34 - 1/U45 - 3,6,8,11/A3U1 - 14

Δ3 FOR SERIAL NUMBERS ABOVE 1630A00135 C225 WAS ADDED TO U28, U29, AND U31 PINS 16 TO GROUND TO IMPROVE POWER SUPPLY BYPASSING.



Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location
C1	1H	R6	1H	R38	1B	U21	4E
C2	1I	R7	1I	S1	7J	U22	7I
C3	2I	R8	1H			U23	7G
C4	5H	R9	1H	TP4	4G	U24	6I
		R10	2H	TP5	5F	U25	6G
C5	4H			TP6	6F	U26	5G
C6	6F	R11	3H	TP7	6F	U27	4G
C7	5F	R12	3H				
C8	5D	R13	2H	TP9	2H	U28	9H
		R14	5H	TP10	5I	U29	8H
CR1	2H	R15	5H	TP11	7I	U31	7H
CR2	2H			TP16	5I	U32	3G
CR3	2C	R16	4H			U33	1F
CR4	2C	R17	4H	U1	9M		
		R18	6F	U2	8M	U34	2G
CR5	1E	R19	6F	U3	7K	U35	2F
CR6	1E	R21	6F	U4	8K	U36	3F
CR7	1A			U5	9K	U37	4F
		R23	2D			U38	3E
Q1	9K	R24	2D	U6	8K		
Q2	1H	R25	2D	U7	8J	U39	2E
Q3	5H	R26	2D	U8	6P	U41	5I
Q4	2C	R27	1D	U9	6P	U42	4I
				U11	5M	U43	2I
Q5	2C	R28	1D			U44	1I
Q6	1E	R29	1D	U12	7M		
Q7	1E	R31	1D	U13	6M	U45	3C
Q8	1A	R32	6H	U14	5M	U47	1C
		R33	2C	U15	5K	U48	7F
R1	8P			U16	5K	U49	4H
R2	9M	R34	2C				
R3	8N	R35	1E	U17	8I	U51	3H
R4	9M	R36	1E	U18	4K	U52	2H
R5	8J	R37	1B	U19	9I	Y1	1H

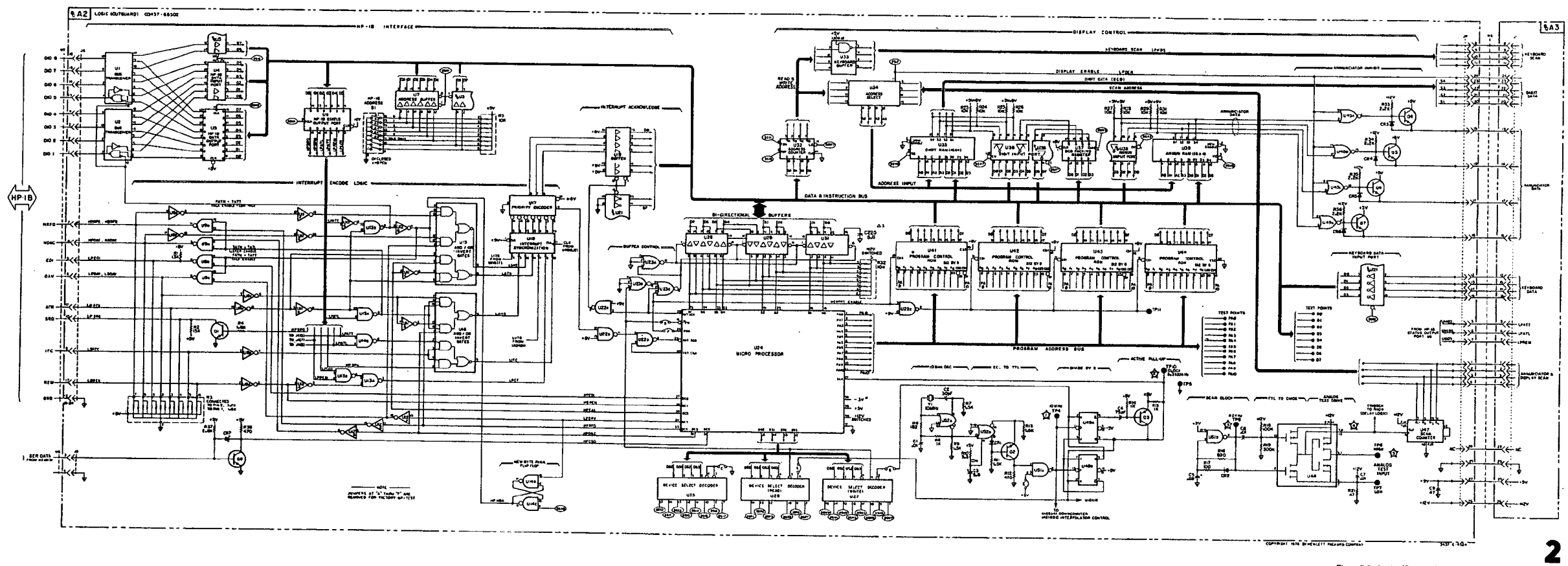
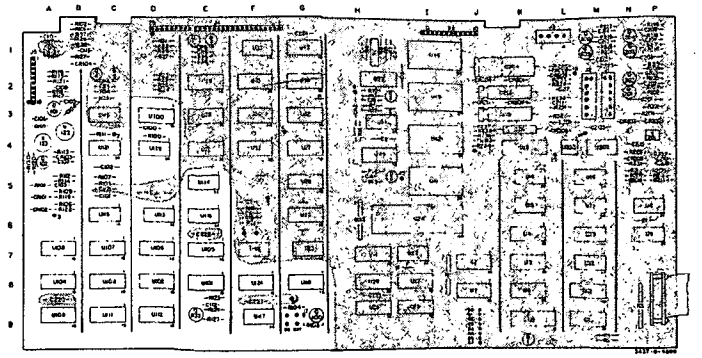


Figure 7-3. Logic (Outguard) Circuit Diagram and Component Locator.

Ref Desig	Location	Ref Desig	Location
C100	3D	R119	5A
C101	5C	R120	6A
C102	4C	R121	2A
C103	5B	R122	6A
C104	3B	R123	9E
C105	3B	R124	9E
C106	3A	R125	9E
C107	4B	R126	1B
C108	2B	R127	1B
C109	3A	R130	5A
C110	1A	TP1	3B
C112	9E	TP2	4C
C113	1B	TP3	6A
CR101	5A	TP8	8G
CR102	6A	TP17	9G
CR103	4B	U100	3D
CR104	1B	U101	8E
Q100	9G	U102	8D
Q101	3A	U103	8C
Q102	4A	U104	8A
Q103	9E	U105	7E
R100	4D	U106	7D
R101	1B	U107	7C
R102	1B	U108	7A
R103	9G	U109	9A
R104	9G	U111	9C
R105	5C	U112	9D
R106	5B	U113	6D
R107	5C	U114	5E
R108	5A	U115	6C
R109	5B	U116	6E
R111	4C	U117	9F
R112	5B	U118	8G
R113	4B	U119	4D
R114	5B	U121	4C
R115	2A	U122	4B
R116	2A	U123	4A
R117	2A	U124	8F
R118	2A		



Δ1 FOR THE FOLLOWING SERIAL NUMBERS AND ABOVE.

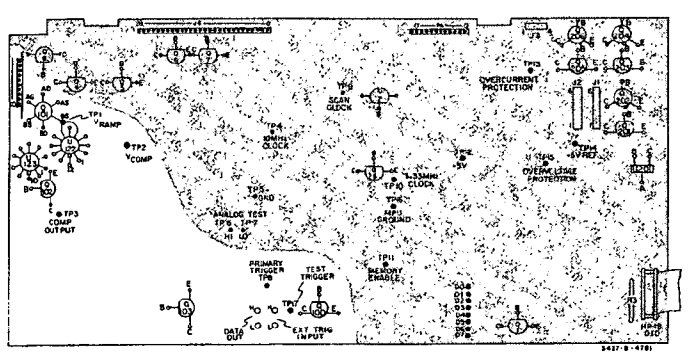
1630A00168
1630A00171
1630A00181
1630A00182
1630A00185
1630A00187
1630A00192
1630A00194

THE ANODE OF CR104 WAS MOVED FROM THE OTHER SIDE OF R127 II C113 TO ENSURE THE INTEGRITY OF THE FIRST CLOCK PULSE.

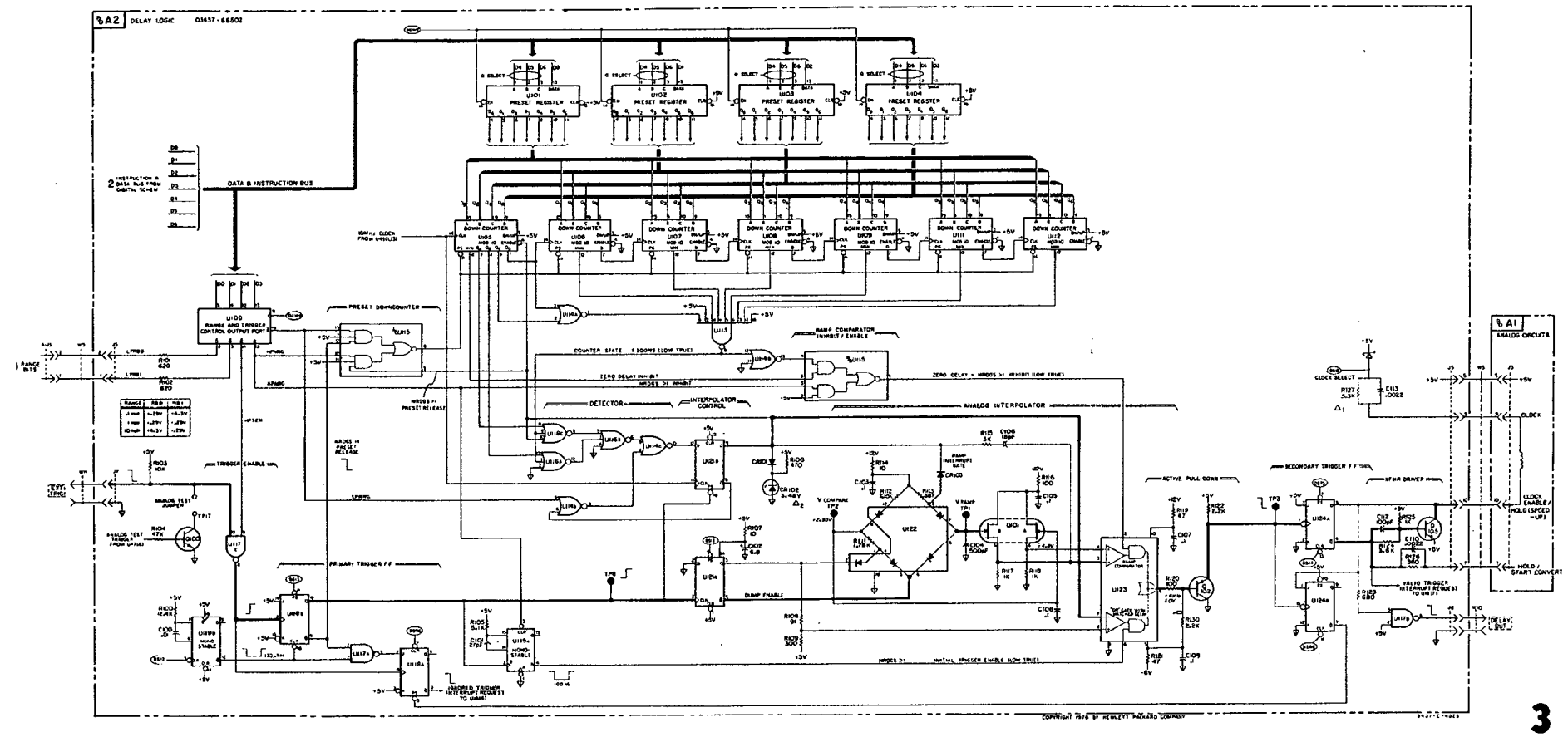
Δ2 FOR SERIAL NUMBERS ABOVE 1630A00520 CR102 WAS CHANGED FROM PART NUMBER 1902-3030 (3.01 V) TO PREVENT UNWANTED SINKING OF CURRENT THROUGH CR103.

U123 (Ramp/"OR" Comparator) Function Table

Mode	Inputs						Output
	V_{Ramp} & V_{Comp}	U121AQ	U121BQ	Inhibit (Low True)	Initial Trigger (Low True)		
	U123 Pin No. 3 & 4	6	7	2	8		9
Normal	V_{Comp} / V_{Ramp}	Clear	Set	Hi	Hi		
Zero - Delay	X		Set	Lo	Hi		
N > 1 Initial Trigger	X	X	X	Lo			
N > Subsequent Outputs	X	Clear		Lo	Hi		

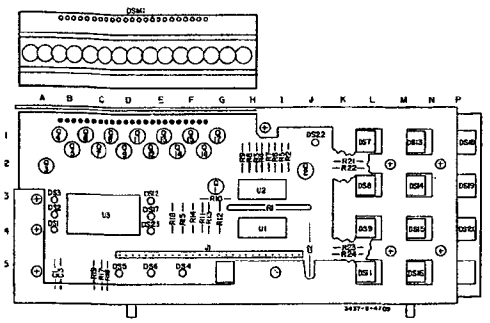


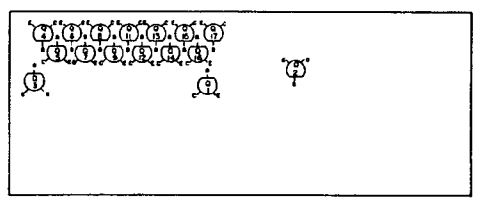
Rev. A



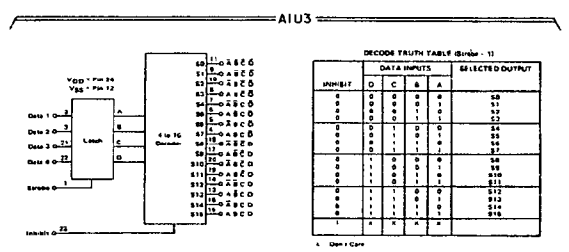
3

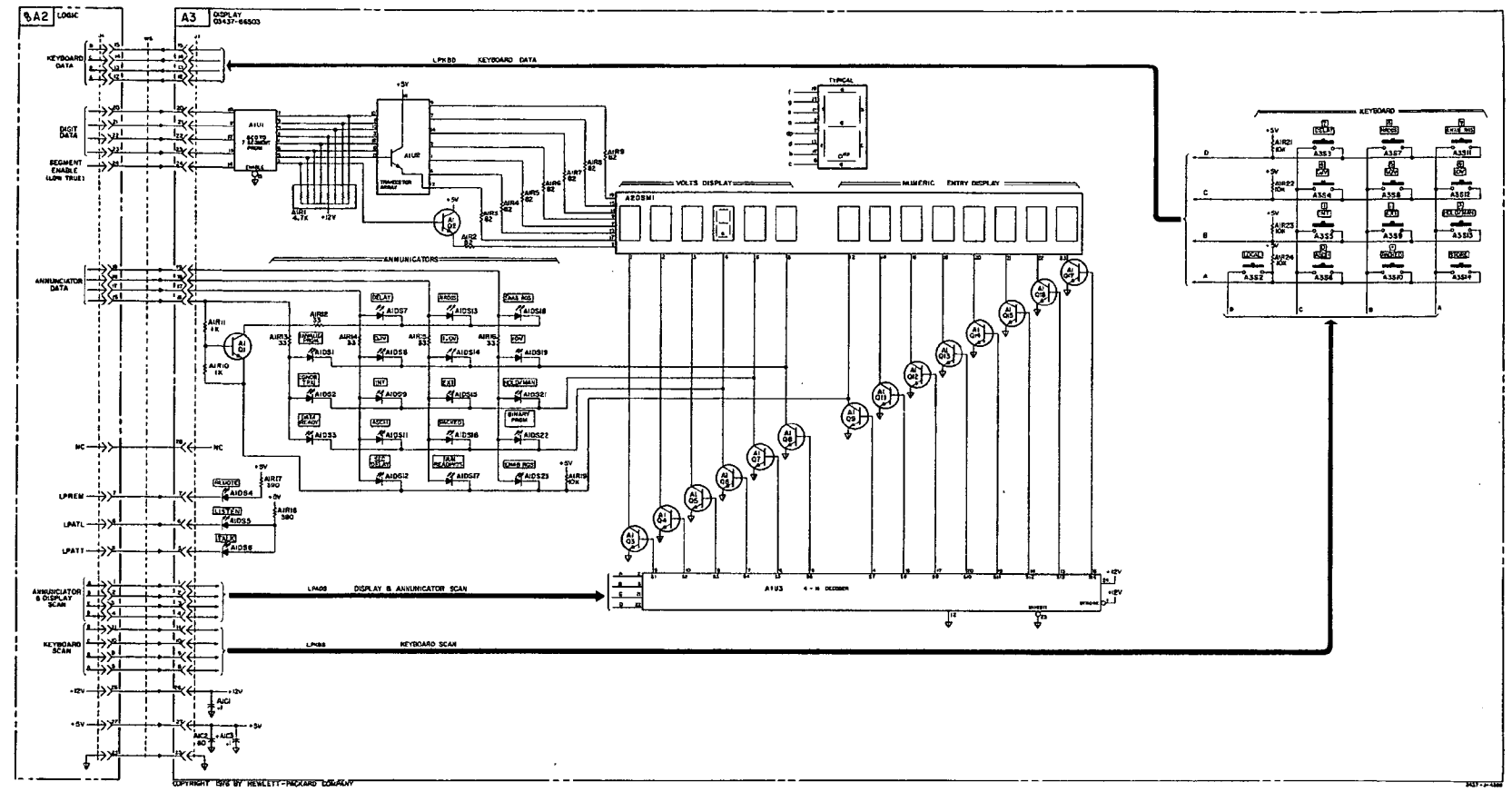
Figure 7-4. Delay Logic Circuit Diagram and Component Locator.
Rev. A 7-15/7-16





Ref Desig	Location	Ref Desig	Location	Ref Desig	Location	Ref Desig	Location
C1	5B	DS15	4M	Q9	1D	R10	3G
C2	4J	DS16	5M	Q11	1D	R11	4F
C3	5B	DS17	3E	Q12	1E	R12	4G
DS1	4B	DS18	1P	Q13	1E	R13	4G
DS2	3B	DS19	2P	Q14	1F	R14	4F
DS3	3B	DS21	4P	Q15	1F	R15	4F
DS4	5F	DS22	1J	Q16	1G	R16	4E
DS5	5D	DS23	4E	Q17	1G	R17	5C
DS6	5E	Q1	2G	R1	3I	R18	5C
DS7	1L	Q2	2J	R2	2I	R19	5C
DS8	2L	Q3	2A	R3	2H	R21	2K
DS9	4L	Q4	1B	R4	2H	R22	2K
DS11	5L	Q5	1B	R5	2I	R23	4K
DS12	3E	Q6	1C	R6	2I	R24	4K
DS13	1M	Q7	1C	R7	2I		
DS14	2M	Q8	1D	R8	2H	U1	4H
				R9	2H	U2	2H
						U3	3C

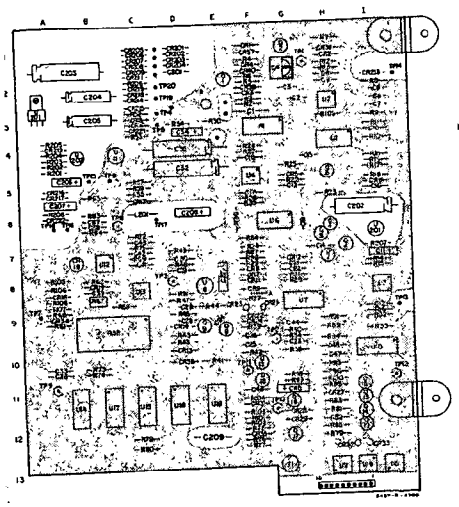


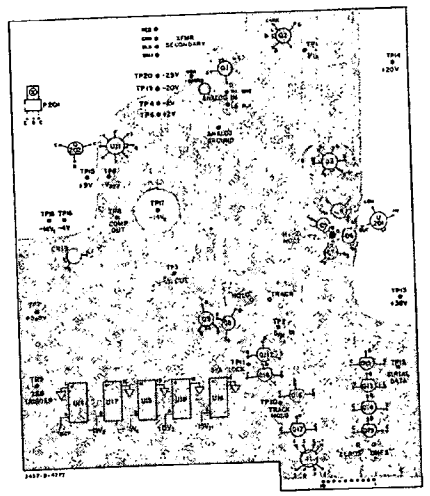


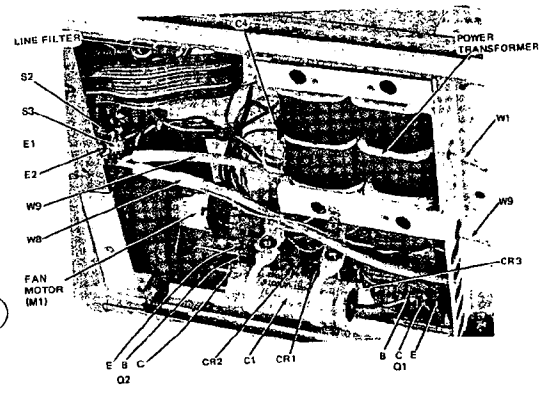
4

Figure 7-5. Display Circuit Diagram and Component Locator.

Ref Desig	Location	Ref Desig	Location
C201	2D	CR218	2C
C202	6I	CR219	2C
C203	1A	CR221	3C
C204	2B	CR222	6A
C205	3B	L201	6C
C206	5A	Q201	3A
C207	5A	Q202	4B
C208	6D	R201	5A
CR201	1D	R202	4A
CR202	1D	R203	4A
CR203	1D	R204	4A
CR204	1D	R205	4A
CR205	1C	R206	2C
CR206	1C	R207	7I
CR207	1C	R208	6A
CR208	1C	TP13	6I
CR209	2C	TP14	2I
CR211	2C	TP15	5B
CR212	4A	TP16	6B
CR213	2I	TP17	6C
CR214	2C	TP18	6A
CR215	3C	TP19	2D
CR216	5A	TP20	2D
CR217	5A	U201	6I

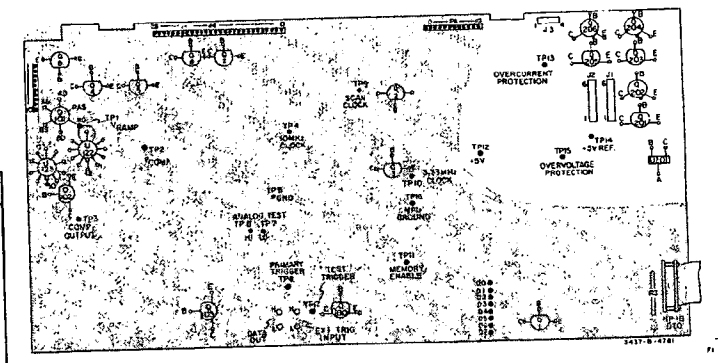




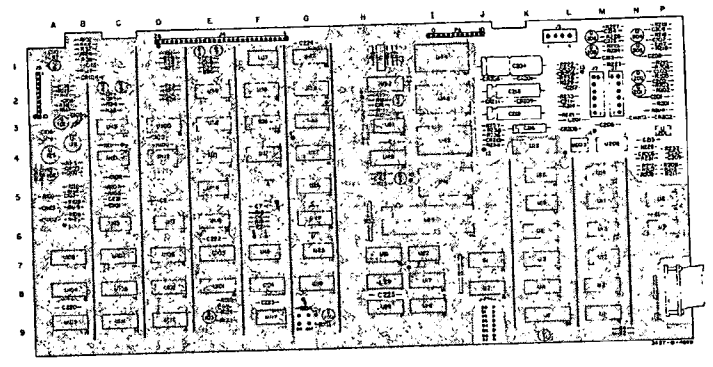


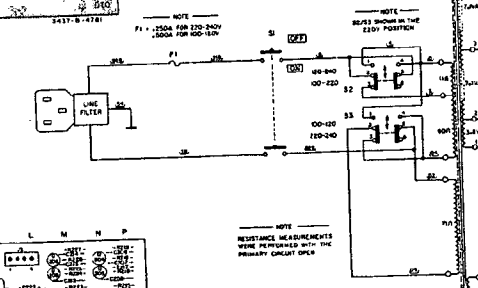
Ref Desig	Location	Ref Desig	Location
C201	2P	R201	3P
C202	2P	R202	2P
C203	2P	R203	2P
C204	1K	R204	3P
C205	3M	R205	2P
C206	1P	R206	2P
C207	1P	R207	5N
C208	1P	R208	5P
C209	4P	R209	6N
C210	4P	R211	5P
C211	2L	R212	5N
C212	1M	R213	5P
C213	1M	R214	3L
C214	1M	R215	1P
C215	4N	R216	1P
C216	4K	R217	1P
C217	2L	R218	1P
C218	2K	R219	1P
C219	3K	R221	3L
C220	5A	R222	1L
C221	5C	R223	1M
C222	6E	R224	1M
C223	9F	R225	1M
C224	1G	R226	1M
		R227	1M
CR201	2K		
CR202	3P	R228	4N
CR203	3N	R229	2L
CR204	2J	R231	4N
CR205	4N	R232	4P
		R233	2L
CR206	2L		
CR207	2L	R234	4J
CR208	3L	R235	2L
CR209	3K	R236	4J
		R237	3J
CR211	2J	R238	3J
CR212	4J		
L201	3L	TP12	4J
Q201	2N	TP13	1L
Q202	2N	TP14	3M
Q203	1N	TP15	4L
Q204	1N	U201	4P
Q205	1M	U202	4M
Q206	1M	U203	4L

Rev. A



Δ_{10} FOR SERIAL NUMBERS GREATER THAN 1530A00670 C204, C205, AND R208 CHANGED FROM PART NUMBER 0683-0049 (20 µF) 0180-0049 (20 µF) AND 0683-3025 (3 K) RESPECTIVELY TO INCREASE THE −25 VOLT SUPPLY OUTPUT CURRENT CAPABILITY REQUIRED WITH THE LOWER R7 DESCRIBED IN Δ_7.





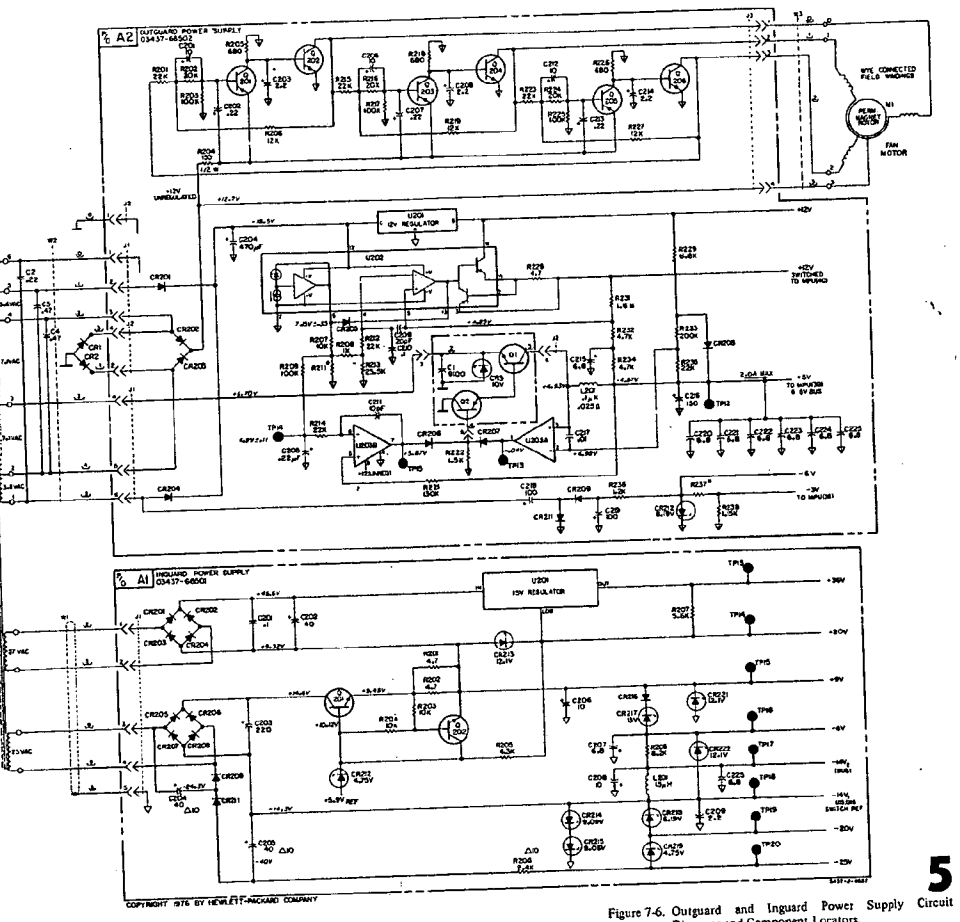


Figure 7-6. Outguard and Inguard Power Supply Circuit Diagrams and Component Locators.
Rev. A 7-19/7-20

SECTION VIII
MANUAL CHANGES

8-1. INTRODUCTION.

8-2. This section contains information required to adapt this manual to serial numbers preceding the serial number indicated on the title page. Since this manual applies to all instruments manufactured to date, separate backdating information is not required.

8-3. Backdating information has been integrated into the Replaceable Parts List in Section VI and the curcuit diagram in Section VII using the Δ symbols. This symbology conforms to the following convention:

Δ_N Where N = A Number

This symbol denotes a component value change or a changed part readily noticeable as a change on the schematic or in a servicing procedure. The description appear near the schematic.

Δ_A Where A = A Letter

This symbol denotes a component part number or vendor change not readily noticeable on the schematic or in a servicing procedure. The description appears beneath the Replaceable Parts List.

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SERVICE NOTE

SUPERSEDES
NONE

P.C. 09–14555
09–14682
09–14423
09–14478
09–14846
09–14175

hp- MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: As Stated Below

CHANGE TO IMPROVE INSTRUMENT ACCURACY

Introduction.

This Service Note discusses a series of changes to the 3437A System Voltmeter to improve the accuracy of some specifications.

A. For serial numbers 1630A00521 and above.

To improve the delay internal accuracy on the 3437A when used as a delay generator, replace CR102 on the 03437-66502 Assembly. Change it from part number 1902-3030 to part number 1902-3048.

B. For serial numbers 1630A00136 and above.

To improve full-scale input on the .1 V range, change diode CR213 on the 03437-66501 Assembly from 1902-0029 to 1902-3183. Also change diode CR12 from 1902-3205 to 1902-3235.

C. All serial numbers where applicable.

To eliminate oscillation of A1U13 and improve instrument accuracy, pins 5 and 6 of A1U13 can be shorted together. To do this, drill a small hole, near pins 5 and 6 and insert an eyelet in the hole so it contacts the P.C. pads of pins 5 and 6. Solder the eyelets to the pads.

D. All serial numbers above 163000271.

To improve accuracy on the .1 V range. Add A1C50, a 200 pF capacitor. part number 0140-0198 in parallel with A1R85 by removing A1R85 and inserting two pins into the pads where R85 was, then solder A1R85 and A1C50 to these two pins. The part number for the pins 0360-1716.

E. All serial numbers above 1630A00166.

To improve the 1 V step response add A1C20 in parallel with A1R7. Remove A1R7 and add 2 pins (part number 0360-1716) to the place where A1R7 was, then solder A1R7 and A1C20 (starred value) to the pins. C20 is a starred value and can be either 18pF, 30 pF or 47 pF.

	Part Number
18 pF	0160-2322
30 pF	0160-2199
47 pF	0160-2307

The proper value of C20 is determined during 1 V step response test in the manual and is chosen to assure compliance with the spec.

F. All serial numbers above 1630A00166.

Change to correct a production error on the 03437-66502 Assembly. Lift out one end of A2R127 and the anode end of A2CR104. Install a pin (part number 0360-1716) in the pad for R127. Then solder R127 and CR104 to the pin.

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SERVICE NOTE

P.C. None

SUPERSEDES
NONE

-hp- 3437A SYSTEM VOLTMETER

Serial Number: All

STATIC PROTECTION OF ANALOG BOARD

CAUTION

The Analog Board 03437-66501(A1 assembly) contains static sensitive FET's and is shipped in conductive foam to prevent static charge buildup damage.

When replacing a bad analog board with a good one, be sure to exercise care in handling the new board. Take all necessary grounding precautions normal with handling static sensitive devices. This is best done by grounding an unplugged instrument's chassis, bleeding static charge from the body by touching the gounded instrument, and then unpacking the new A1 assembly for installaition.

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1/77–09

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P.C. 09–16075

SUPERSEDES
NONE

-hp- PART NUMBER 03437-69800

SERVICE KIT FOR 3437A SYSTEMS VOLTMETER

Serial Numbers: All

I. INTRODUCTION.

The 03437-69800 is a service kit designed to facilitate on-site isolation and repair of failures in the -hp- Model 3437A Systems Voltmeter. The kit contains three pretested PC Assemblies, which can be substituted for PC assemblies in a malfunctioning unit. The kit contains several selected miscellaneous components, as well as some special test fixtures to be used in the performance tests. Also included in the Service Kit is the special ROM needed for Signature Analysis Troubleshooting in the 3437A. A verification program cartridge which uses the 9825A Calculator to check out the 3436A is also included.

II. KIT APPLICATION.

PC assemblies suspected of being faulty can be replaced with the known good ones supplied with the kit. Component level repair can also be effected on the faulty board by using Signature Analysis and the individual components supplied with the kit.

III. TROUBLESHOOTING.

Refer to 3437A Operating and Service Manual for troubleshooting procedures which can be used to help repair the instrument.

IV. SERVICE KIT PARTS LIST.

The items listed in Table 1 are contained in the 03437-69800 Service Kit.

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Table 1. Parts List.

Qty.	Designator	-hp- Part No.	Description
1	A1	03437-66501	PC Assy - Analog
1	A2	03437-66502	PC Assy - Digital
1	A3	03437-69301	Front Panel Assembly
1	A1Q3	03437-62501	Matched Set - Transistors
1	A1R1 & A1R8*	03437-62502	Matched Set - Resistors
1	A2U24	03437-62503	Nanoprocessor Assy
1		03437-61613	Triax Input Cable
1		10100C	50 Ohm Terminator
1		1816-1025	Bipolar PROM
1		1820-0621	TTL BUF 7438N
1		1820-0981	IC - DGTL 4016
1		1820-1145	CMOSCVTRCD4049AE
1		1820-1210	IC SN74LS51
1		1820-1216	IC SN74LS138
3		1820-1279	TTL CNTR747S190N
1		1820-1416	TTL TRGR 74LS14N
3		1820-1491	IC SN74LS367N
2		1820-1558	LIN TRCVRMC3441P
1		1820-1683	CMOS4LTCHMC14514
1		1820-1729	TTL LATCH74LS259
1		1853-0233	SXTR - PNP SP8442
1		1854-0071	SXTR - NPN SPS5103
2		1854-0565	XSTR NPN SI
5		1854-0730	XSTR - MPS6531
1		1855-0081	JFET - NCHAN1N5245
1		1855-0242	FET - SINGLEFN3967
1		1855-0368	JFET - NCHANFN2861
2		1901-0040	DIO - SI .05A 30 V
2		1901-0376	DIO - SI 35 V
1		1990-0444	PHOTO - ISO
5		1990-0486	L.E.D.
1		1990-0584	OPT - ISLR ILD74
1		1990-0589	DSPLY MONOLITHIC
1		34113A	P.T.T. INTFC
1		34114A	P.T.S. INTFC
1		34115A	DSA TEST ROM
1		03437-10001	3437A/9825A Test Csst
1		03437-64501	Carrying Case Assy
2		5060-9436	PB - SWITCH
1		9100-3881	XFMR - PULSE
10		1460-1489	Jumper Clips
1		P-03437-69800-1	Service Kit Part Note
5		1540-0249	Plastic Box

Accessory Box Lists.

Box 1

1 ea.	1990-0589
1 ea.	9100-3881
2 ea.	5060-9436

Box 2

10 ea.	Jumper Clips
1 ea.	10100C
1 ea.	34113A
1 ea.	34114A

Box 3

1 ea.	34115A
1 ea.	1816-1025
1 ea.	1820-1683
1 ea.	03437-62502
1 ea.	03437-62503

Box 4

3 ea.	1820-1279
1 ea.	1990-0584
1 ea.	1990-0444
1 ea.	1820-1210
1 ea.	1820-1145
1 ea.	1820-0621
1 ea.	1820-1729
1 ea.	1820-1216
1 ea.	1820-1416
1 ea.	1820-0981
2 ea.	1820-1558
3 ea.	1820-1491

Box 5

5 ea.	1990-0486
1 ea.	1855-0071
1 ea.	1855-0081
1 ea.	1855-0368
5 ea.	1854-0730
1 ea.	03437-62501
1 ea.	1855-0242
2 ea.	1901-0040
2 ea.	1901-0376
2 ea.	1854-0565
1 ea.	1853-0233

03437-69800

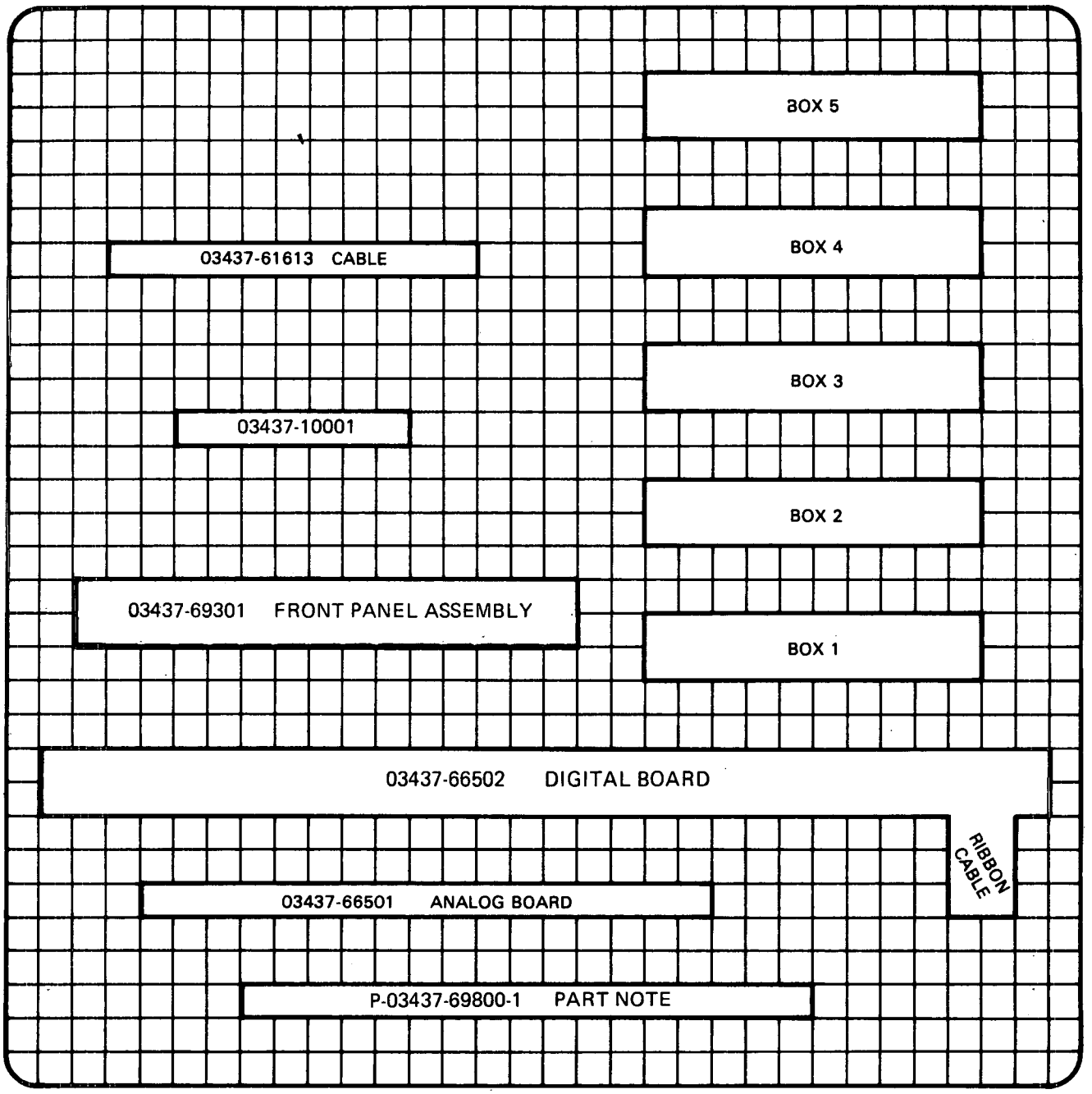

Figure 1. Service Kit Layout.

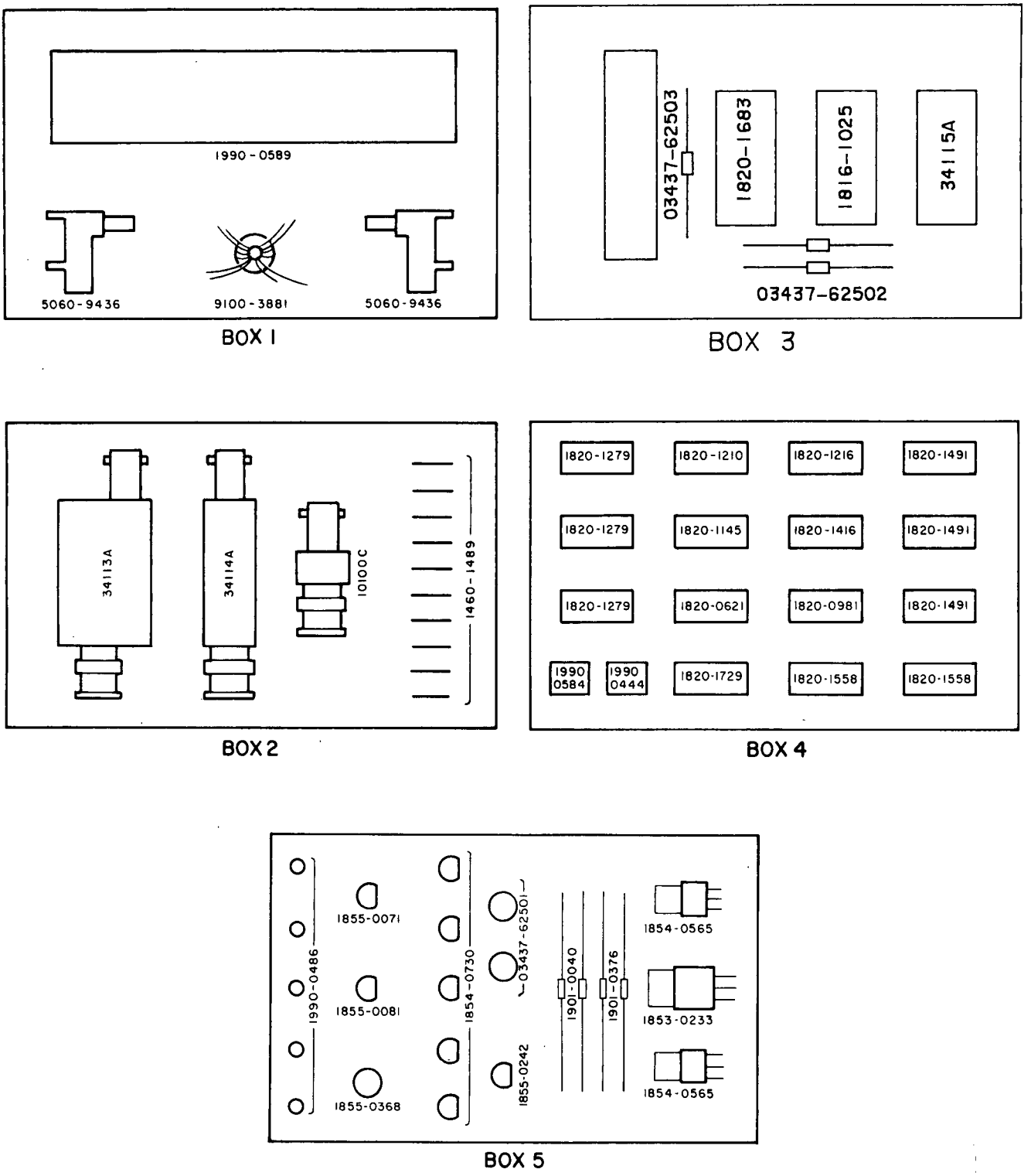

Figure 2. Individual Component Layout.

```
0: "SVM Op Ve Ck-3437A Systems Voltmeter Oper. Verif. Check":
1: prt "****************";spc ;prt "***3437A SVM***"
2: prt "  Oper. Verif.","     Check","     100476";spc 2
3: dim A[10];fxd 0
4: time 5000
5: on err "Time out"
6: cll ´init´;clr "svm"
7: "Program Code Check":
8: fmt "F1E0ST1R1D.0000000SN0000S";wrt "svm";0→I;0→H;100→K;gsb "check"
9: fmt "F1E1ST1R1D.1111111SN1111S";wrt "svm";1→I;21→H;101→K;gsb "check"
10: fmt "F2E2ST2R2D.2222222SN2222S";wrt "svm";2→I;42→H;102→K;gsb "check"
11: fmt "F1E3ST3R3D.3333333SN3333S";wrt "svm";3→I;63→H;103→K;gsb "check"
12: fmt "F1E4ST1R1D.4444444SN4444S";wrt "svm";4→I;104→H;104→K;gsb "check"
13: fmt "F1E5ST1R1D.5555555SN5555S";wrt "svm";5→I;125→H;105→K;gsb "check"
14: fmt "F1E6ST1R1D.6666666SN6666S";wrt "svm";6→I;146→H;106→K;gsb "check"
15: fmt "F1E7ST1R1D.7777777SN7777S";wrt "svm";7→I;167→H;107→K;gsb "check"
16: fmt "D.8888888SN8888S";wrt "svm";8→I;210→H;110→K;gsb "check"
17: fmt "D.9999999SN9999S";wrt "svm";9→I;231→H;111→K;gsb "check"
18: "Binary Program Mode Check":
19: fmt "R3T1D.1234567SN8900SE4S";wrt "svm"
20: cll ´lsvm´(A,B)
21: cll ´psvm´(A,B)
22: cll ´lsvm´(A,B)
23: gto +2;if A#33035069103;prt "SVM returned",A,"representing";gto +1
24: prt "bytes 4 thru 7.";spc ;gto "Fail"
25: gto +2;if B#198137000;prt "SVM returned",B,"representing";gto +1
26: prt "bytes 1 thru 3";gto "Fail"
27: if flg0;gto "Fail"
28: "Pass":cll ´END´;prt "SVM Passed","Oper. Verif.","Check";spc 2;end
29: "Fail":cll ´END´;prt "SVM Failed","Oper. Verif.","  Check";spc 2;end
30: "check":rds("svm")→A;bit(3,A)→A
31: if A#1;gto +4
32: prt "SVM initiated","Service Request"
33: prt "indicating that","it received an","invalid progam"
34: prt "during Learn";fmt "Test #",f3.0;wrt 16,I;spc ;sfg 0
35: wtb "svm",66;for J=1 to 7;dtordb("svm")→A[J];next J
36: if A[2]#H;sfg 2
37: if A[3]#H;sfg 2
38: if A[4]#K;sfg 3
39: if A[5]#H;sfg 3
40: if A[6]#H;sfg 3
41: if A[7]#H;sfg 3
```

Figure 3. Program Listing.

```
42: if I#0;gto +2
43: gto +10;if A[1]=205;gto +11
44: if I>7;gto +8
45: jmp 1
46: gto +7;if A[1]=225;gto +8
47: gto +6;if A[1]=53;gto +7
48: gto +5;if A[1]=276;gto +6
49: gto +4;if A[1]=305;gto +5
50: gto +3;if A[1]=325;gto +4
51: gto +2;if A[1]=345;gto +3
52: if A[1]=365;gto +2
53: sfg 1
54: if flg1;cfg 1;sfg 0;prt "Binary Byte 1 Error";gto "BP-Fail#"
55: if flg2;cfg 2;sfg 0;prt "Binary Byte 2 & 3  NRDGS Error";gto "BP-Fail
56: if flg3;cfg 3;sfg 0;prt "Binary Byte 4 to 7 DELAY Error";gto "BP-Fail#"
57: ret
58: "BP-Fail#":prt "Learn Test #",I;spc ;for Q=1 to 7
59: fmt "Byte",x,fl.0,x,f3.0;wrt 16,Q,A[Q];next Q;spc 2;cfg 2,3;ret
60: "Time out":prt "HP-IB problem,","SVM did not"
61: prt "respond within","5 sec.";spc
62: prt "Problem in";fmt "line #",f4.0;wrt 16,erl;spc ;prt "Remove"
63: prt "all bus","instr. except","SVM & calulator.","Rerun Check.";spc 2;end
64: "lsvm":
65: wtb "svm",66;3→p10
66: rdb(724)→pp10;p10+1→p10;if p10<10;gto -0
67: p9+1e3p8+1e6p7+1e9p6→p1;p5+1e3p4+1e6p3→p2
68: ret
69: "psvm":
70: int(p1/1e9)→p6;int((p1-1e9p6)/1e6)→p7;int((p1-1e9p6-1e6p7)/1e3)→p8
71: p1-1e9p6-1e6p7-1e3p8→p9;int(p2/1e6)→p3;int((p2-1e6p3)/1e3)→p4
72: p2-1e6p3-1e3p4→p5
73: wtb "svm",66,p3,p4,p5,p6,p7,p8,p9
74: ret
75: "init":
76: if p0=0;rem 7;clr 7
77: fmt f;dev "dvm",722,"svm",724,"ptr",715
78: dev "scn",709,"scn1",710,"scn2",711,"scn3",712
79: wtb "ptr",27,69
80: ret
81: "END":
82: dsp "Test Complete";cli 7;clr 724;ret
*28988
```

Figure 3. Program Listing (cont'd).

P.C. 09–16073

SUPERSEDES
NONE

-hp- PART NUMBER 03437-69900

PRODUCT SUPPORT PACKAGE FOR 3437A SYSTEMS VOLTMETER

Serial Numbers: All

I. INTRODUCTION.

The 03437-69900 is a field Product Support Package (PSP) designed to help facilitate on-site isolation and repair of failures in the -hp- Model 3437A System Voltmeter by the use of disgnostic aids. The package contains various diagnostic aids including a special ROM needed for Signature Analysis, as well as special test fixtures to be used in the performance tests. A verification program cartridge which uses the 9825A Calculator to check out the 3437A is also included.

II. PSP APPLICATION.

By using the above mentioned diagnostic aids along with the proper components and PC assemblies,component and board level repair can be effected. The components and PC assemblies used most often in these repairs are listed as the recommended Field Service Inventory (FSI) in Section V. The PSP is packaged in the same carrying case assembly used for the complete customer service kit. This allows the case to be filled with the appropriate PC assemblies and components from the FSI to repair the 3437A at the customer's site. See Figure 1.

III. TROUBLESHOOTING.

Refer to 3437A Operating and Service Manual for troubleshooting procedures which can be used to help repair the instrument.

IV. PSP PARTS LISTS.

Table 1. Parts List.

Qty.	-hp- Part No.	Description
1 ea.	03437-61613	Triax Input Cable
1 ea.	10100C	50 Ohm Terminator
1 ea.	34113A	P.T.T. Interface
1 ea.	34114A	P.T.S. Interface
1 ea.	34115A	D.S.A. Test ROM
1 ea.	03437-10001	3437A/9825A Test Crtdg.
5 ea.	1540-0249	Plastic Box
10 ea.	1460-1489	Jumper Clips
1 ea.	P-03437-69900-1	Part Note
1 ea.	03437-64501	Carrying Case Assy

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03437-69800

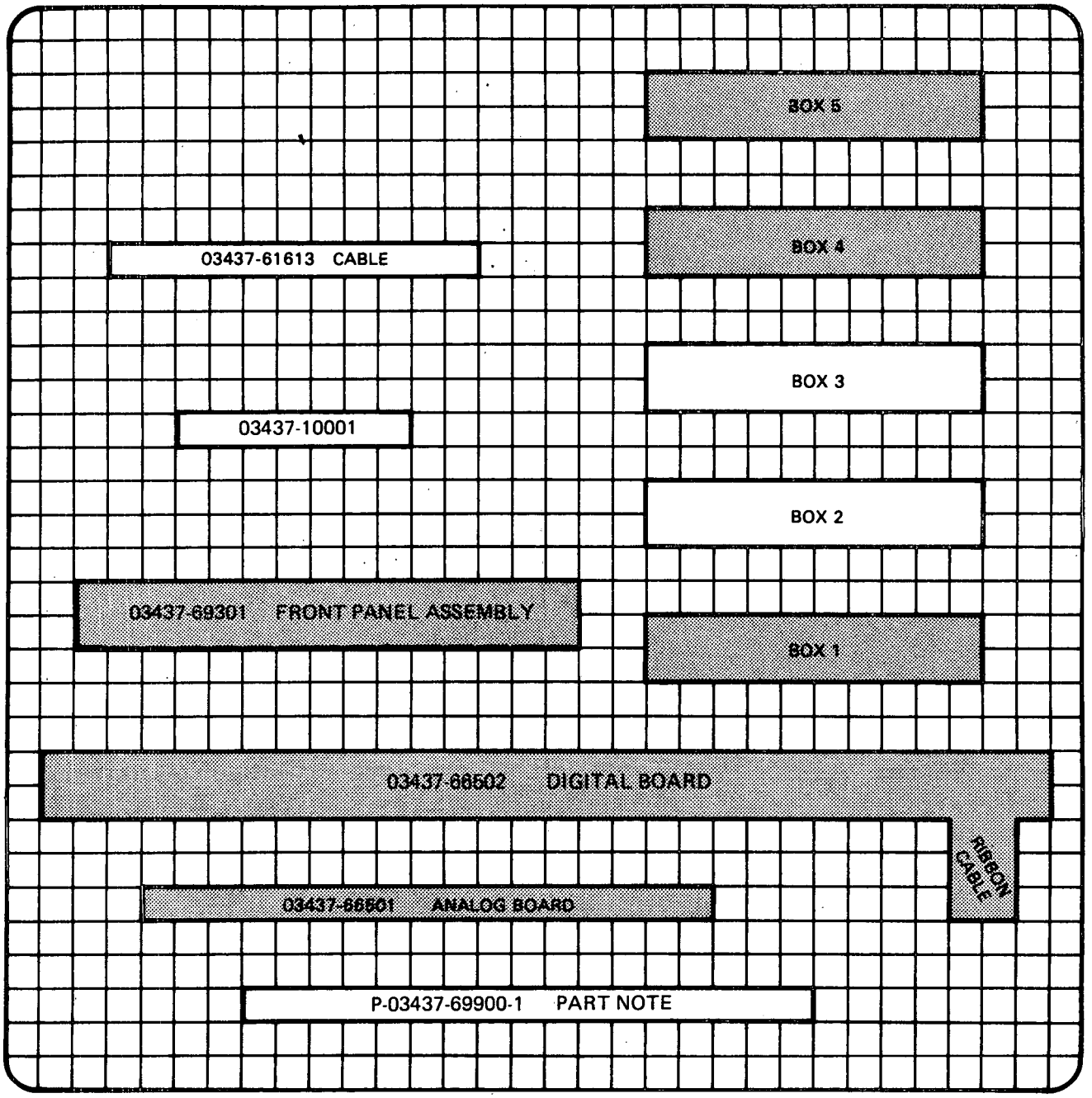


Figure 1. PSP Layout.

NOTE 1: PARTS IN SHADED AREAS ARE NOT SUPPLIED IN THE PSP, SEE FSI RECOMMENDATIONS SECTION V.

V. FIELD SERVICE INVENTORY.

The following lists is the recommended level of Field Service Inventory for the -hp- Model 3437A Systems Voltmeter.

Table 2. FSI Recommendation.

Designator	-hp- Part No.	Description	Qty.
A1	03437-66501	PC Assy - Analog	1
A2	03437-66502	PC Assy - Digital	1
A3	03437-69301	Front Panel Assy	1
A3A1	03437-66503	PC Assy - Display Driver	1
A1Q3	03437-62501	Matched Set - Transistors	1
A1R1 & A1R8*	03437-62502	Matched Set - Resistors	1
A2U24	03437-62503	Nanoprocessor Assy	1
	1816-1025	Bipolar Prom	1
	1820-0621	TTL BUF 7438N	1
	1820-0981	IC - DGTL 4016	1
	1820-1145	CMOSCVTR CD4049AE	1
	1820-1210	IC SN74LS51	1
	1820-1216	IC SN74LS138	1
	1820-1279	TTL CNTR 747S190N	3
	1820-1416	TTL TRGR 74LS14N	1
	1820-1491	IC SN74LS367N	3
	1820-1558	LIN TRCVRMC3441P	2
	1820-1683	CMOS 4LTCH MC 14514	1
	1820-1729	TTL LATCH 74LS259	1
	1853-0233	SXTR - PNP SP8442	1
	1854-0071	SXTR - NPN SPS5103	1
	1854-0565	XSTR - NPN SI	2
	1854-0730	XSTR - MPS6531	5
	1855-0081	JFET - NCHANIN5245	1
	1855-0242	FET - SINGLEFN3967	1
	1855-0368	JFET - NCHANFN2861	1
	1901-0040	DIO-SI .05A 30 V	2
	1901-0376	DIO-SI 35 V	2
	1990-0444	PHOTO - ISO	1
	1990-0486	L.E.D.	5
	1990-0584	OPT - ISLR ILD74	1
	1990-0589	DSPLY MONOLITHIC	1
	5060-9436	PB - SWITCH	2
	9100-3881	XFMR - PULSE	1

Accessory Box Lists.

Box 1

1 ea.	1990-0589
1 ea.	9100-3881
2 ea.	5060-9436

Box 2

10 ea.	Jumper Clips
1 ea.	10100C
1 ea.	34113A
1 ea.	34114A

Box 3

1 ea.	34115A
1 ea.	1816-1025
1 ea.	1820-1683
1 ea.	03437-62502
1 ea.	03437-62503

These parts are supplied in this PSP. For the remaining components see FSI Recommendations Section V.

Box 4

3 ea.	1820-1279
1 ea.	1990-0584
1 ea.	1990-0444
1 ea.	1820-1210
1 ea.	1820-1145
1 ea.	1820-0621
1 ea.	1820-1729
1 ea.	1820-1216
1 ea.	1820-1416
1 ea.	1820-0981
2 ea.	1820-1558
3 ea.	1820-1491

Box 5

5 ea.	1990-0486
1 ea.	1855-0071
1 ea.	1855-0081
1 ea.	1855-0368
5 ea.	1854-0730
1 ea.	03437-62501
1 ea.	1855-0242
2 ea.	1901-0040
2 ea.	1901-0376
2 ea.	1854-0565
1 ea.	1853-0233

NOTE: Plastic Boxes are supplied in this PSP to allow components from FSI to be added to the PSP to repair the 3437A at the customer's site.

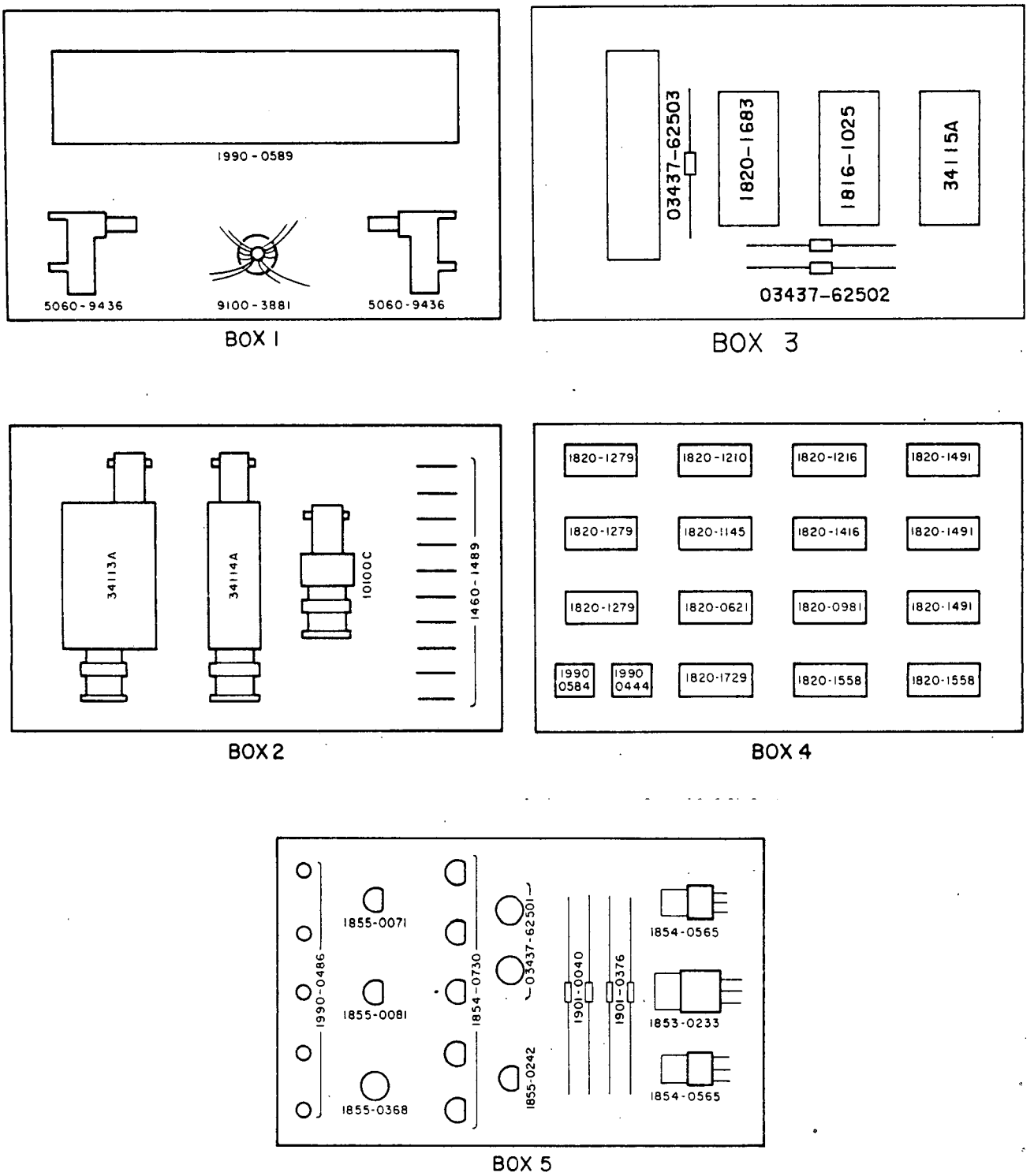


Figure 2. Individual Component Layout.

```
0: "SVM Op Ve Ck-3437A Systems Voltmeter Oper. Verif. Check":
1: prt "****************";spc ;prt "***3437A SVM***"
2: prt "  Oper. Verif.","     Check","     100476";spc 2
3: dim A[10];fxd 0
4: time 5000
5: on err "Time out"
6: cll ´init´;clr "svm"
7: "Program Code Check":
8: fmt "F1E0ST1R1D.0000000SN0000S";wrt "svm";0→I;0→H;100→K;gsb "check"
9: fmt "F1E1ST1R1D.1111111SN1111S";wrt "svm";1→I;21→H;101→K;gsb "check"
10: fmt "F2E2ST2R2D.2222222SN2222S";wrt "svm";2→I;42→H;102→K;gsb "check"
11: fmt "F1E3ST3R3D.3333333SN3333S";wrt "svm";3→I;63→H;103→K;gsb "check"
12: fmt "F1E4ST1R1D.4444444SN4444S";wrt "svm";4→I;104→H;104→K;gsb "check"
13: fmt "F1E5ST1R1D.5555555SN5555S";wrt "svm";5→I;125→H;105→K;gsb "check"
14: fmt "F1E6ST1R1D.6666666SN6666S";wrt "svm";6→I;146→H;106→K;gsb "check"
15: fmt "F1E7ST1R1D.7777777SN7777S";wrt "svm";7→I;167→H;107→K;gsb "check"
16: fmt "D.8888888SN8888S";wrt "svm";8→I;210→H;110→K;gsb "check"
17: fmt "D.9999999SN9999S";wrt "svm";9→I;231→H;111→K;gsb "check"
18: "Binary Program Mode Check":
19: fmt "R3T1D.1234567SN8900SE4S";wrt "svm"
20: cll ´lsvm´(A,B)
21: cll ´psvm´(A,B)
22: cll ´lsvm´(A,B)
23: gto +2;if A#33035069103;prt "SVM returned",A,"representing";gto +1
24: prt "bytes 4 thru 7.";spc ;gto "Fail"
25: gto +2;if B#198137000;prt "SVM returned",B,"representing";gto +1
26: prt "bytes 1 thru 3";gto "Fail"
27: if flg0;gto "Fail"
28: "Pass":cll ´END´;prt "SVM Passed","Oper. Verif.","Check";spc 2;end
29: "Fail":cll ´END´;prt "SVM Failed","Oper. Verif.","  Check";spc 2;end
30: "check":rds("svm")→A;bit(3,A)→A
31: if A#1;gto +4
32: prt "SVM initiated","Service Request"
33: prt "indicating that","it received an","invalid progam"
34: prt "during Learn";fmt "Test #",f3.0;wrt 16,I;spc ;sfg 0
35: wtb "svm",66;for J=1 to 7;dtordb("svm")→A[J];next J
36: if A[2]#H;sfg 2
37: if A[3]#H;sfg 2
38: if A[4]#K;sfg 3
39: if A[5]#H;sfg 3
40: if A[6]#H;sfg 3
41: if A[7]#H;sfg 3
```

Figure 3. Program Listing.

```
42: if I#0;gto +2
43: gto +10;if A[1]=205;gto +11
44: if I>7;gto +8
45: jmp I
46: gto +7;if A[1]=225;gto +8
47: gto +6;if A[1]=53;gto +7
48: gto +5;if A[1]=276;gto +6
49: gto +4;if A[1]=305;gto +5
50: gto +3;if A[1]=325;gto +4
51: gto +2;if A[1]=345;gto +3
52: if A[1]=365;gto +2
53: sfg 1
54: if flg1;cfg 1;sfg 0;prt "Binary Byte 1 Error";gto "BP-Fail#"
55: if flg2;cfg 2;sfg 0;prt "Binary Byte 2 & 3  NRDGS Error";gto "BP-Fail
56: if flg3;cfg 3;sfg 0;prt "Binary Byte 4 to 7 DELAY Error";gto "BP-Fail#"
57: ret
58: "BP-Fail#":prt "Learn Test #",I;spc ;for Q=1 to 7
59: fmt "Byte",x,f1.0,x,f3.0;wrt 16,Q,A[Q];next Q;spc 2;cfg 2,3;ret
60: "Time out":prt "HP-IB problem,","SVM did not"
61: prt "respond within","5 sec.";spc
62: prt "Problem in";fmt "line #",f4.0;wrt 16,er1;spc ;prt "Remove"
63: prt "all bus","instr. except","SVM & calulator.","Rerun Check.";spc 2;end
64: "lsvm":
65: wtb "svm",66;3→p10
66: rdb(724)→pp10;p10+1→p10;if p10<10;gto -0
67: p9+1e3p8+1e6p7+1e9p6→p1;p5+1e3p4+1e6p3→p2
68: ret
69: "psvm":
70: int(p1/1e9)→p6;int((p1-1e9p6)/1e6)→p7;int((p1-1e9p6-1e6p7)/1e3)→p8
71: p1-1e9p6-1e6p7-1e3p8→p9;int(p2/1e6)→p3;int((p2-1e6p3)/1e3)→p4
72: p2-1e6p3-1e3p4→p5
73: wtb "svm",66,p3,p4,p5,p6,p7,p8,p9
74: ret
75: "init":
76: if p0=0;rem 7;clr 7
77: fmt f;dev "dvm",722,"svm",724,"ptr",715
78: dev "scn",709,"scn1",710,"scn2",711,"scn3",712
79: wtb "ptr",27,69
80: ret
81: "END":
82: dsp "Test Complete";cli 7;clr 724;ret
*28988
```

Figure 3. Program Listing (cont'd).

SERVICE NOTE

P.C. None

SUPERSEDES
NONE

-hp- 3437A SYSTEMS VOLTMETER

Serial Numbers: All

"CARE AND FEEDING OF 3437's"
OR
APPLICATION AND PROGRAMMING CONSIDERATIONS

APPLICATION AND PROGRAMMING CONSIDERATIONS

Applications — Points to remember

No Noise Immunity. A reading taken by the 3437A indicates the input voltage level at the point in time when the reading is triggered. There is no rejection of line related noise. This may surprise you when you measure a "dc" source.

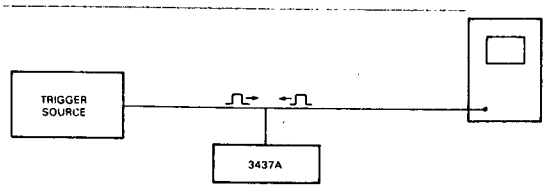
Input Bandwidth. The 3 dB bandwidth specs are:

10 V Range - 1.0 mHz
1 V Range - 1.3 mHz
.1 V Range - 40 kHz

The 3437A is excellent for digitizing *low frequency* waveforms or measuring pure sinusoids at higher frequencies. However, the front end will not pass high frequency components of a waveform. This may prevent the 3437A from accurately digitizing some waveforms.

External Trigger. The 3437A is edge triggered off the negative edge of the external trigger pulse. If the pulse rings (due to unterminated source), an "Ignore Trigger" may result because the 3437A tries to trigger off the ringing. Also be careful of reflections of trigger pulse from unterminated scope input:

This set-up can cause "Ignore Trigger":



To prevent reflections:

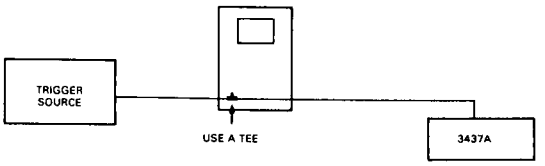


Figure 1. Proper Scope Connection.

RAS/dlh/WN

09/06-09

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"Require Service Status" (RQS)

Three status conditions of the 3437 can cause it to pull SRQ on the BUS. Which one(s) actually pull(s) SRQ is determined by the service request mask, ENAB RQS. The three status conditions which may pull SRQ are:

Data Ready. Delays of up to 1 second in a measurement burst of 9999 readings are programmable on the 3437. Rather than tying the BUS up for all this time (up to 2 hrs. 47 min.) the 3437 is programmed to pull SRQ when a measurement is ready to be output.

Ignore Trigger. The 3437 failed to output a reading in response to one or more triggers it received (internal or external).

Local. Reading is taken and output to display. Minimum time between readings 110 μ sec.

Remote. Reading is taken and output to the BUS. When outputting to an infinitely fast listener the minimum delay time between readings is 169 μ sec (1/5900). For a real listener, the rate is:

$$\frac{5900}{5900 + \text{(Listen Rate)}} \text{(Listen Rate)}$$

Invalid Program. You tried to program the 3437A with a code it does not understand.

You can enable any one or combination of the above conditions to pull SRQ by entering the proper number into ENAB RQS (Service Request Mask). Each possible service request condition corresponds to a number: 1, 2 or 4. An ENAB RQS of 4 enables Data Ready to pull SRQ, 6 enables Data Ready and Ignore Trigger (4 & 2), 7 enables Data Ready, Ignore Trigger and Invalid Program.

When SRQ is pulled, the controller is generally programmed to do a serial poll and a status byte is returned to the controller defining which RQS STATUS condition exists.

Programming — Hints

Missing Readings.

Depending on how the 3437A is programmed to trigger, it may appear the 3437A is not outputting all the readings in a burst. The following 9825 program demonstrates this:

```
0:  dim A(1000) - dimension array to take in readings.

1:  wtb 734, "R3N1000SD.004ST3" - programs 3437A to 10 V range, 1000 reading
burst, 4 ms delay, hold/man trigger.

:-  intermediate lines performing various operations.
:

10: for I = 1 to 1000 - set up loop to take in readings.

11: red 725, A(I) - input each 3437A reading into 9825 and store it in array.

12: next I - ends loop.

13: end.
```

If you run the above program the calculator may hang up. Pressing STOP and checking the value of I, you may discover only 997 readings were entered into A(I). Therefore, the calculator is waiting for three more readings. However, the 3437A has finished its burst. What gives?

In line 1 the T3 program code triggered the 3437A to immediately start its burst. It wasn't until line 11 that the 3437A was addressed to talk and the calculator to listen. During the time it took to execute the intermediate lines, 2-9, three readings were taken and output to the 3437A display. Result - only 997 readings were handshook to the calculator and it sits in the for-next loop waiting for 3 more.

The solution is to use the T1 trigger mode in line 1. This way the 3437A burst will be triggered by ATN going false the first time through line 11. No readings will be lost.

Fast Data Transfer.

To speed up data transfer the following program could be used.

0: dim A (1000); wtb 725, "R3N1000D.004ST1" - dimensions array and sets up 3437A.

1: red 725 - addresses 3437A to talk (ATN remains true).

2: for I = 1 to 1000 - sets up loop.

3: red 731, A(I) - 731 is an unassigned adress. The 3437A remains addressed to talk from line 2 and is triggered by ATN going false as the calculator tries to read from 731. The reading is input into A(I).

4: next I - ends loop.

5: end.

Fastest Data Transfer - But be careful!!

For even faster data transfer (allowing smaller delays to be programmed without causing an Ignore Trigger) the transfer, tfr, statement can be used.

The tfr (transfer) statement can be used to output a burst at high speed to the 9825A by using the following subprogram:

0: dim A(100) - dimension array.

1: buf "io", 701, 3 sets up buffer in calculator to receive 100 readings in ASCII format.

2: wtb 735, "R3N100SD.0005ST1" - programs 3437A.

3: tfr 725, "io" - transfers readings to buffer at high rate.

4: fmt f, z - free format, suppresses check for CR LF.

5: for I = 1 to 100.

6: red "io", A(I) - transfers readings from buffer to array.

7: next I.

However, be aware that due to internal timing in the calculator I/O, it will take longer to accept the first reading than subsequent readings (up to 3 X as long). The result is that with a sufficiently short delay programmed, the 3437A may ignore its second trigger and indicate an Ignore Trigger. (See Figure 2.)

As shown in Figure 2, the transfer statement can still be used effectively by setting up the system to trigger the burst 2 delay periods earlier and increasing the number of readings by 2. The first reading taken into the 9825A is thrown away. The first reading stored (#3 in the lower diagram) is the first reading you wanted in the first place. However, you will still get an ignore trigger indication (the second trigger was ignored) and you will have to be confident your delay was long enough that no other triggers were ignored.

Unable to gain front panel control (9825A Controller).

If the 3437A is outputting a burst of readings to the 9825A and the STOP key on the 9825A is pressed, the 3437A will indicate Ignore Trigger and stop outputting readings. Now if the LOCAL button on the 3437A is pressed you will regain local control. The 3437A will not sample except once each time one of the trigger buttons is pushed. Why?

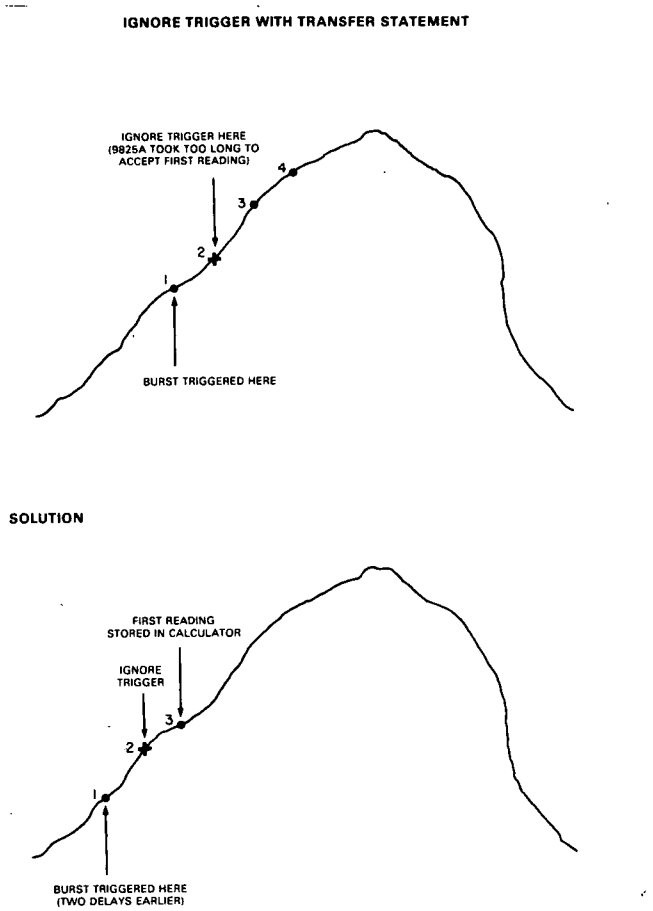

Figure 2. Trigger Ignore Due to Transfer Statement.

The STOP key on the 9825A *does not* pull IFC on the BUS. Therefore the 9825A is still addressed to listen, the 3437A is addressed to talk and is waiting for the 9825A to accept the remaining readings in the burst. Under these circumstances the 3437A will not go into local control.

To go into local from the middle of an output burst two alternatives exists:

1. Hit RESET on the 9825A. (Due to a bug in early 9825A's each time RESET was pressed there was a chance of indiscriminately changing memory bits. There was a chance of even destroying the entire program. This bug is supposed to be fixed. However, it seems like a good idea to use RESET only as a last resort.)

2. A preferred solution is to execute the following command on the 9825A:

cli 7 - programs IFC

then hit the LOCAL button then the INT button on the 3437A (The above solution is necessary for early 9825A. A field modification on the 9825A I/O cards involving a ROM swap will allow you to make the 3437A go to local using only software commands. The program line would be:

cli; lcl 725

SERVICE NOTE

P.C. 09-18110

SUPERSEDES
NONE

-hp- MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: All

SERVICING STICKY FRONT PANEL PUSHBUTTONS

The following procedure can be performed to service any front panel pushbutton which may stick due to rubbing against the enclosed LED:

a. Heat the LED's solder connections with a low temperature tip.

b. Push the button in and out several times.

This will straighten out the LED and relieve any pressure which it may be exerting on the pushbutton.

If this procedure does not improve the pusbutton's operation and the 3437A's serial number is below 1630A02271, the LED can be replaced with part number 1990-0665. 1990-0065 is electrically identical to the instrument's LED, however it is physically smaller, reducing the possibility of sticky switches.

1990-0665 is the recommended replacement for A3A1 DS7 - DS9, DS11, DS13 - DS16, DS18, DS19, and DS21.

If any LED is changed, the Replaceable Parts list in the 3437A Operating and Service Manual should be corrected.

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P.C. 09-18542
09-18864
09-19089

SUPERSEDES
3437A-4

3437A SYSTEM VOLTMETER

Serial Numbers: 1630A02599 and Below

RECOMMENDED REPLACEMENT FOR A2U124

When replacing A2U124, an -hp- Part Number 1820-0629 should be used. In addition R120, R122 and R130 should be changed to the values listed in the table below.

Reference Designator	Old Value	New Value	New -hp- Part No.
A2R120	200 Ω	402 Ω	0698-4453
A2R122	2.2 kΩ	1.1 kΩ	0757-0424
A2R130	4.42 kΩ	2.2 kΩ	0683-2225
A2U124	---	---	1820-0629

If these components are replaced, the Replaceable Parts List in your 3437A's Operating and Service Manual should be revised.

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P.C. 09-19824

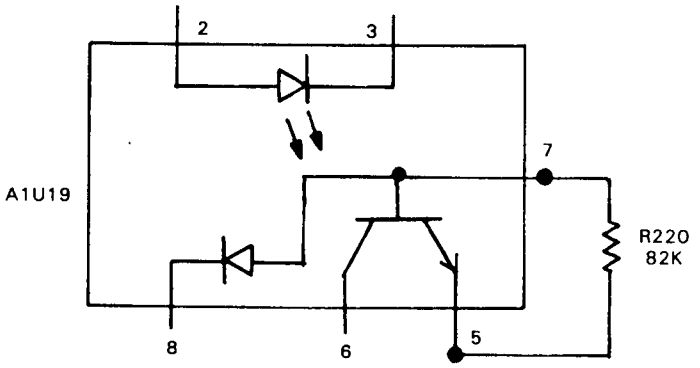
SUPERSEDES
NONE

-hp- MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: 1630A03891 and Below

REDUCING DATA PROPAGATION DELAY

If the 3437A samples data before it has changed from the previous value, add a 82KΩ resistor (p/n 0683-8235) from pin 5 to pin 7 of A1U19.



If this change is made, the Replaceable Parts List in your 3437A's Operating and Service Manual should be revised.

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3437A-6A
SERVICE NOTE

SUPERSEDES
3437A-6

3437A SYSTEM VOLTMETER

Serial Numbers: 1630A03530 and Below

NANOPROCESSOR REPLACEMENT

The new version of the nanoprocessor (p/n 1820-1692) has a fixed back gate voltage of −5 volts which allows R237 (p/n 0757-0408) to be fixed value of 243Ω.

Reference Designator	Old -hp- Part No.	New -hp- Part No.
A2U24	03437-62503	1820-1692
A2R237	—	0757-0408

When the new version of the nanoprocessor (lot code 0103 and above) is installed in a 3437A the unit will not power up correctly unless the changes listed in the table below are made.

Reference Designator	Old Value	New Value	New -hp- Part No.
A2R207	10KΩ	6.04KΩ	0698-3497
A2R208	1KΩ	8.87KΩ	0698-4202
A2R212	22KΩ	Wire Jumper 22GA	8159-0005
A2R213	25.5KΩ	8.87KΩ	0698-4202
A2R232	4.75KΩ	4.99KΩ	0698-3279
A2R234	4.7KΩ	4.99KΩ	0698-3279
CR205*	---	---	Remove
A2R250**	---	11KΩ	0757-0443

*Note: Be sure to remove CR205
**Note: Be sure to add A2R250

The resistor A2R250 can be added to the board by the following procedure:

a. Lift the grounded end of A2C215 (see Figure 1), insert a post, and resolder A2C215 to the post.

I/-/WN 4/81-09/BRS

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b. Lift the end of A2R231 that is connected to A2R232 (see Figure 1), insert a post and resolder A2R231 to the post.

c. Add A2R250 by soldering one end to each post (see Figure 1).

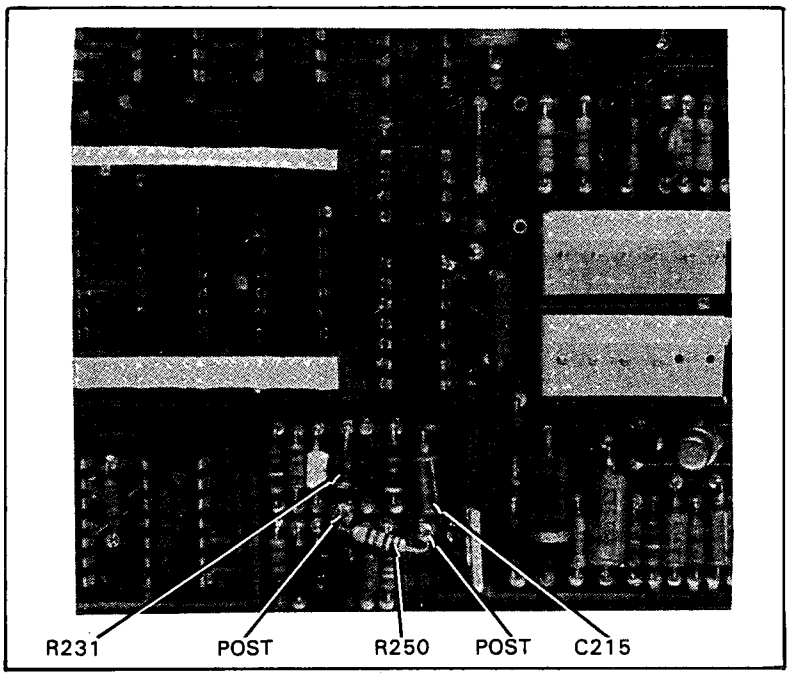

Figure 1. Adding A2R250 (P/N 0757-0443).

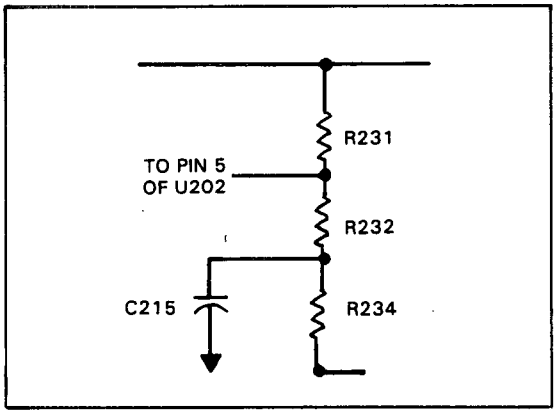

Figure 2. Old Schematic. (Outguard Power Supply)

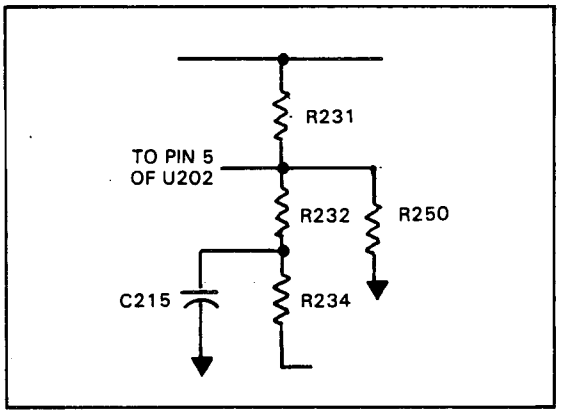

Figure 3. New Schematic. (Outguard Power Supply)

After making these modification, revise the Replaceable Parts List and the power supply schematic in your 3437A's Operating and Service Manual.

SUPERSEDES
P-03437-69900-1

03437-69900

-hp- MODEL 3437A SYSTEM VOLTMETER

Serial Numbers: All

PRODUCT SUPPORT PACKAGE FOR 3437A SYSTEMS VOLTMETER

1. INTRODUCTION

The 03437-69900 is a field Product Support Package (PSP) designed to help facilitate on-site isolation and repair of failures in the -hp- Model 3437A System Voltmeter by the use of diagnostic aids. The package contains various diagnostic aids including a special ROM needed for Signature Analysis, as well as special test fixtures to be used in the performance tests. A verification program cartridge which uses the 9825A Calculator to check out the 3437A is also included.

II. PSP APPLICATION

By using the above mentioned diagnostic aids along with the proper components and PC assemblies, component and board level repair can be effected. The components and PC assemblies used most often in these repairs are listed as the recommended Field Service Inventory (FSI) in Section V. The PSP is packaged in the same carrying case assembly used for the complete customer service kit. This allows the case to be filled with the appropriate PC assemblies and components from the FSI to repair the 3437A at the customer's site. See Figure 1.

III. TROUBLESHOOTING

Refer to 3437A Operating and Service Manual for troubleshooting procedures which can be used to help repair the instrument.

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IV. PSP PARTS LISTS

Table 1. Parts List

Qty.	-hp- Part Number	Description
1 ea.	03437-61613	Triax Input Cable
1 ea.	10100C	50 Ohm Terminator
1 ea.	34113A	P.T.T. Interface
1 ea.	34114A	P.T.S. Interface
1 ea.	34115A	D.S.A. Test ROM
1 ea.	03437-10001	3437A/9825A Test Crtdg.
5 ea.	1540-0249	Plastic Box
10 ea.	1460-1489	Jumper Clips
1 ea.	3437A-7	Service Note
1 ea.	03437-64501	Carrying Case Assembly

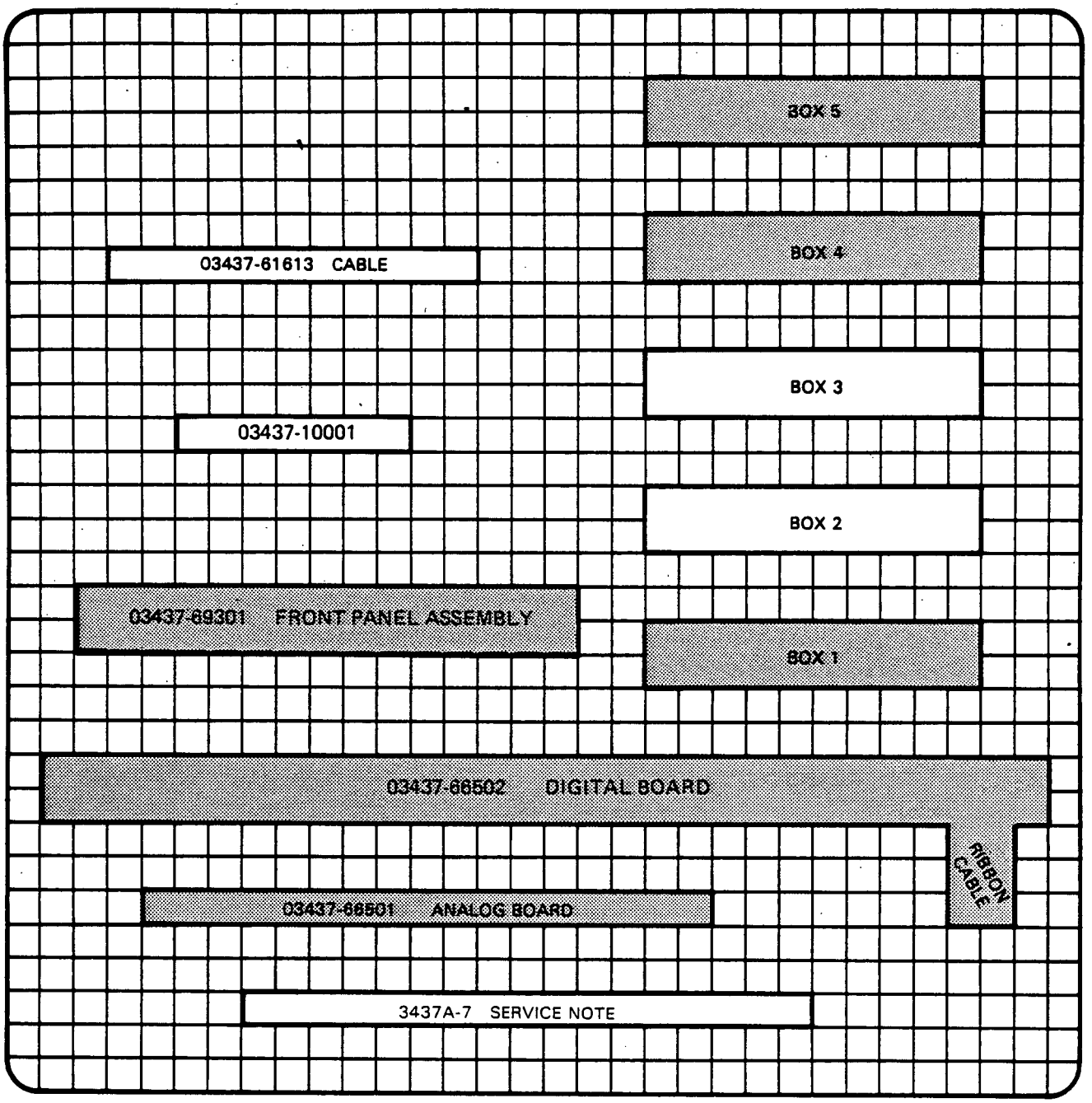
V. FIELD SERVICE INVENTORY

The following list is the recommended level of Field Service Inventory for the -hp- Model 3437A Systems Voltmeter.

Table 2. FSI Recommendation

Designator	-hp- Part Number	Description	Qty.
A1	03437-66501	PC Assembly - Analog	1
A2	03437-66502	PC Assembly - Digital	1
A3	03437-69301	Front Panel Assembly	1
A1Q3	03437-62501	Matched Set - Transistors	1
A1R1 and A1R8*	03437-62502	Matched Set - Resistors	1
A2U24	1820-1692	Nanoprocessor Assembly	1
A3U1	1816-1025	Bipolar Prom	1
A2U9	1820-0621	TTL BUF 7438N	1
A1U1	1820-0981	IC - DGTL 4016	1
A1U10	1820-1145	CMOSCVTR CD4049 AE	1
A2U15	1820-1210	IC SN74LS51	1
A2U25	1820-1216	IC SN74LS138	1
A2U105	1820-1279	TTL CNTR 747S190N	3
A2U8	1820-1416	TTL TRGR 74LS14N	1
A2U19,U31	1820-1491	IC SN74LS367N	3
A2U1	1820-1558	LIN TRCVRMC3441P	2
A3U3	1820-1683	CMOS 4LTCH MC 14514	1
A2U101,U104	1820-1729	TTL LATCH 74LS259	1
A1Q13,Q18,A2Q100	1854-0071	XSTR -NPN SPS5103	1
A1Q201	1854-0565	XSTR - NPN SI	2
A3Q1-Q17,A2Q4-Q7	1854-0730	XSTR - MPS6531	5
A1Q4,Q5,Q7	1855-0081	JFET - NCHANIN5245	1
A1Q1	1855-0242	FET - SINGLEFN3967	1
A2CR2	1901-0040	DIO-SI .05A 30 V	2
A1CR1,CR38	1901-0376	DIO-SI 35 V	2
A1U9	1990-0444	PHOTO - ISO	1
A3A1	1990-0486	L.E.D.	5
A1U5	1990-0732	OPTO ISLR 20 ma	1
A3A2	1990-0589	DSPLY MONOLITHIC	1
A3A1S1	5060-9436	PB - SWITCH	2
A1T1	9100-3881	XFMR - PULSE	1

03437-69900



NOTE 1: PARTS IN SHADED AREAS ARE NOT SUPPLIED IN THE PSP, SEE FSI RECOMMENDATIONS SECTION V.

Figure 1. PSP Layout

Accessory Box Lists

Box 1

1 ea.	1990-0589
1 ea.	9100-3881
2 ea.	5060-9436

Box 2

10 ea.	Jumper Clips
1 ea.	10100C
1 ea.	34113A
1 ea.	34114A

These parts are supplied in this PSP. For the remaining components see FSI Recommendations Section V.

Box 3

1 ea.	34115A
1 ea.	1816-1025
1 ea.	1820-1683
1 ea.	03437-62502
1 ea.	1820-1692

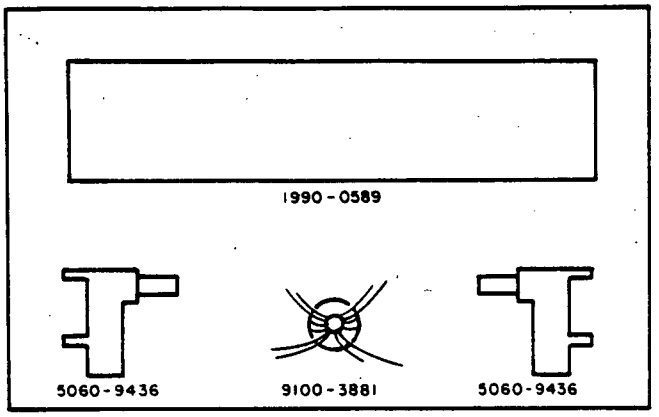
Box 4

3 ea.	1820-1279
1 ea.	1990-0732
1 ea.	1990-0444
1 ea.	1820-1210
1 ea.	1820-1145
1 ea.	1820-0621
1 ea.	1820-1729
1 ea.	1820-1216
1 ea.	1820-1416
1 ea.	1820-0981
2 ea.	1820-1558
3 ea.	1820-1491

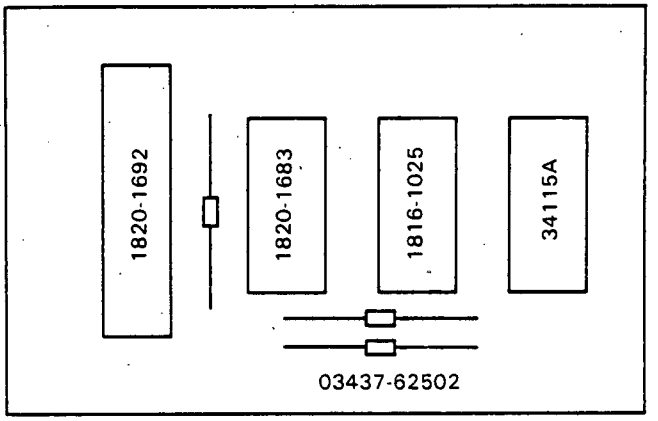
Box 5

5 ea.	1990-0486
1 ea.	1855-0071
1 ea.	1855-0081
5 ea.	1854-0730
1 ea.	03437-62501
1 ea.	1855-0242
2 ea.	1901-0040
2 ea.	1901-0376
2 ea.	1854-0565
1 ea.	1853-0233

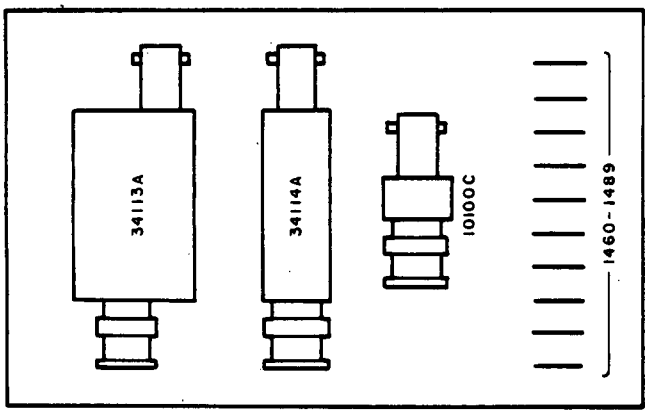
NOTE: Plastic boxes are supplied in this PSP to allow components from FSI to be added to the PSP to repair the 3437A at the customer's site.



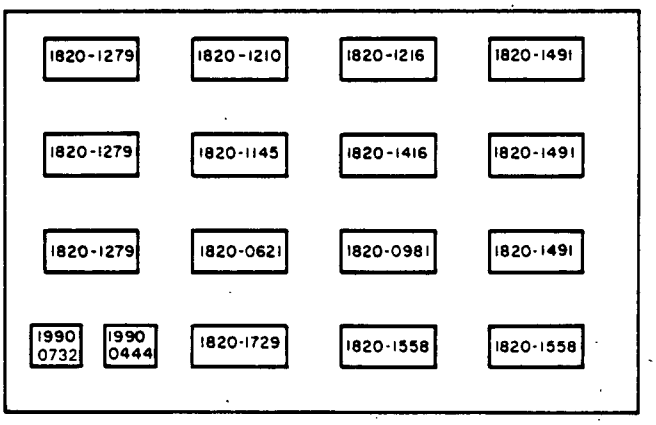
BOX 1



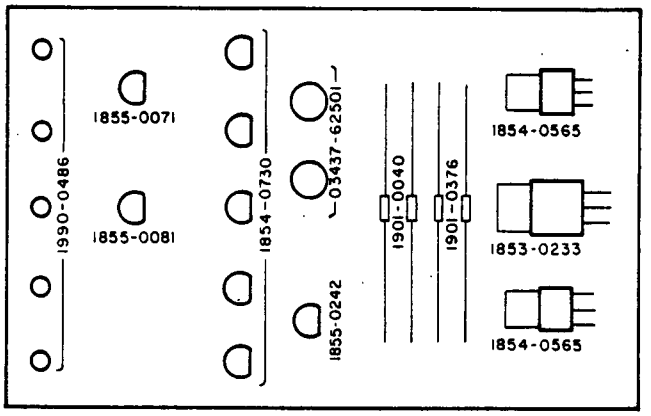
BOX 3



BOX 2



BOX 4



BOX 5

Figure 2. Individual Component Layout

```
 0: "SVM Op Ve Ck-3437A Systems Voltmeter Oper. Verif. Check":
 1: prt "****************";spc ;prt "***3437A SVM***"
 2: prt "  Oper. Verif.","     Check","     100476";spc 2
 3: dim A[10];fxd 0
 4: time 5000
 5: on err "Time out"
 6: cll ´init´;clr "svm"
 7: "Program Code Check":
 8: fmt "F1E0ST1R1D.0000000SN0000S";wrt "svm";0→I;0→H;100→K;gsb "check"
 9: fmt "F1E1ST1R1D.1111111SN1111S";wrt "svm";1→I;21→H;101→K;gsb "check"
10: fmt "F2E2ST2R2D.2222222SN2222S";wrt "svm";2→I;42→H;102→K;gsb "check"
11: fmt "F1E3ST3R3D.3333333SN3333S";wrt "svm";3→I;63→H;103→K;gsb "check"
12: fmt "F1E4ST1R1D.4444444SN4444S";wrt "svm";4→I;104→H;104→K;gsb "check"
13: fmt "F1E5ST1R1D.5555555SN5555S";wrt "svm";5→I;125→H;105→K;gsb "check"
14: fmt "F1E6ST1R1D.6666666SN6666S";wrt "svm";6→I;146→H;106→K;gsb "check"
15: fmt "F1E7ST1R1D.7777777SN7777S";wrt "svm";7→I;167→H;107→K;gsb "check"
16: fmt "D.8888888SN8888S";wrt "svm";8→I;210→H;110→K;gsb "check"
17: fmt "D.9999999SN9999S";wrt "svm";9→I;231→H;111→K;gsb "check"
18: "Binary Program Mode Check":
19: fmt "R3T1D.1234567SN8900SE4S";wrt "svm"
20: cll ´lsvm´(A,B)
21: cll ´psvm´(A,B)
22: cll ´lsvm´(A,B)
23: gto +2;if A#33035069103;prt "SVM returned",A,"representing";gto +1
24: prt "bytes 4 thru 7.";spc ;gto "Fail"
25: gto +2;if B#198137000;prt "SVM returned",B,"representing";gto +1
26: prt "bytes 1 thru 3";gto "Fail"
27: if flg0;gto "Fail"
28: "Pass":cll ´END´;prt "SVM Passed","Oper. Verif.","Check";spc 2;end
29: "Fail":cll ´END´;prt "SVM Failed","Oper. Verif.","  Check";spc 2;end
30: "check":rds("svm")→A;bit(3,A)→A
31: if A#1;gto +4
32: prt "SVM initiated","Service Request"
33: prt "indicating that","it received an","invalid progam"
34: prt "during Learn";fmt "Test #",f3.0;wrt 16,I;spc ;sfg 0
35: wtb "svm",66;for J=1 to 7;dtordb("svm")→A[J];next J
36: if A[2]#H;sfg 2
37: if A[3]#H;sfg 2
38: if A[4]#K;sfg 3
39: if A[5]#H;sfg 3
40: if A[6]#H;sfg 3
41: if A[7]#H;sfg 3
```

Figure 3. Program Listing

```
42: if I#0;gto +2
43: gto +10;if A[1]=205;gto +11
44: if I>7;gto +8
45: jmp I
46: gto +7;if A[1]=225;gto +8
47: gto +6;if A[1]=53;gto +7
48: gto +5;if A[1]=276;gto +6
49: gto +4;if A[1]=305;gto +5
50: gto +3;if A[1]=325;gto +4
51: gto +2;if A[1]=345;gto +3
52: if A[1]=365;gto +2
53: sfg 1
54: if flg1;cfg 1;sfg 0;prt "Binary Byte 1 Error";gto "BP-Fail#"
55: if flg2;cfg 2;sfg 0;prt "Binary Byte 2 & 3  NRDGS Error";gto "BP-Fail
56: if flg3;cfg 3;sfg 0;prt "Binary Byte 4 to 7 DELAY Error";gto "BP-Fail#"
57: ret
58: "BP-Fail#":prt "Learn Test #",I;spc ;for Q=1 to 7
59: fmt "Byte",x,f1.0,x,f3.0;wrt 16,Q,A[Q];next Q;spc 2;cfg 2,3;ret
60: "Time out":prt "HP-IB problem,","SVM did not"
61: prt "respond within","5 sec.";spc
62: prt "Problem in";fmt "line #",f4.0;wrt 16,erl;spc ;prt "Remove"
63: prt "all bus","instr. except","SVM & calulator.","Rerun Check.";spc 2;end
64: "lsvm":
65: wtb "svm",66;3→p10
66: rdb(724)→pp10;p10+1→p10;if p10<10;gto -0
67: p9+1e3p8+1e6p7+1e9p6→p1;p5+1e3p4+1e6p3→p2
68: ret
69: "psvm":
70: int(p1/1e9)→p6;int((p1-1e9p6)/1e6)→p7;int((p1-1e9p6-1e6p7)/1e3)→p8
71: p1-1e9p6-1e6p7-1e3p8→p9;int(p2/1e6)→p3;int((p2-1e6p3)/1e3)→p4
72: p2-1e6p3-1e3p4→p5
73: wtb "svm",66,p3,p4,p5,p6,p7,p8,p9
74: ret
75: "init":
76: if p0=0;rem 7;clr 7
77: fmt f;dev "dvm",722,"svm",724,"ptr",715
78: dev "scn",709,"scn1",710,"scn2",711,"scn3",712
79: wtb "ptr",27,69
80: ret
81: "END":
82: dsp "Test Complete";cli 7;clr 724;ret
*28988
```

Figure 3. Program Listing (Cont'd)

HP 3437A System Voltmeter
HP 3455A Digital Voltmeter

Replacement Fan Installation Note

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03455-90020

Manual Part Number: 03455-90020
Microfiche Part Number: 03455-99020

Printed: JANUARY 1996 Edition 1
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Introduction

This *Installation Note* describes the procedure to install a replacement fan in the HP 3437A System Voltmeter and HP 3455A Digital Voltmeter. One set of instructions is included for both instruments since they use the same replacement fan kit and the installation procedures are similar.

Installation Procedure

1. Remove the top and bottom covers from the instrument.

2. To remove the old fan, loosen the two screws used to secure the fan to the chassis frame. Note that four wires connect the fan to the main circuit board in the instrument. Remove the plastic connector from the circuit board and then pull the four wires from the connector (press down on the connector tabs with a small screwdriver to release the wires). *Save the connector for use with the replacement fan.*

3. The original fan was an ac-powered fan with special transistor drive circuitry implemented on the main circuit board. The replacement fan is a dc-powered fan and requires that you disable the original transistor drive circuitry as described below.

   For the HP 3437A (*see diagram on following page*):

   - Remove Resistor R204 (150Ω).

   - Remove Drive Transistor Q202.

   - For serial numbers below 2516A09074 (or 03437-66502 Rev G or before), install a 22Ω 2W resistor (included with fan kit) between the collector and emitter holes of the transistor previously removed.

     - or -

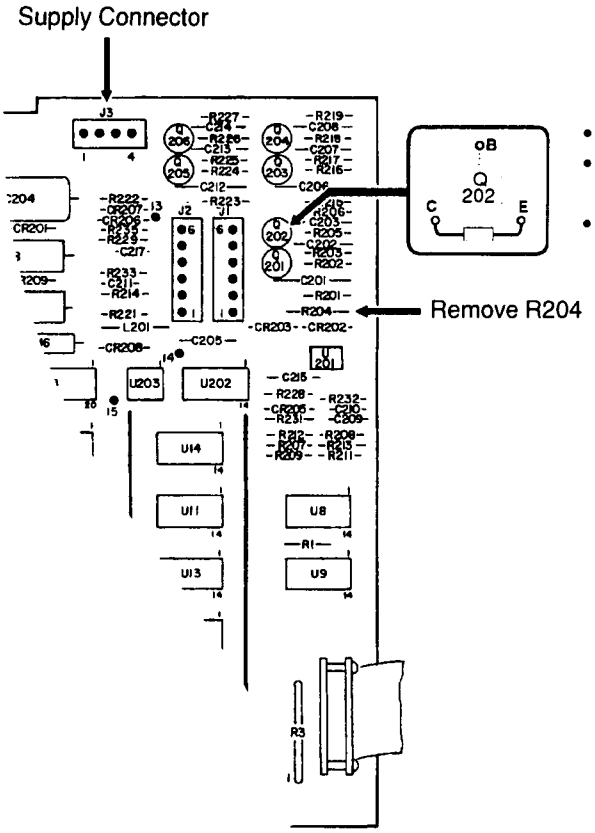
   - For serial numbers 2516A09075 and above, install a shorting jumper (included with fan kit) between the collector and emitter holes of the transistor previously removed.

   For the HP 3455A (*see diagram on following page*):

   - Remove Resistor R12 (150Ω).

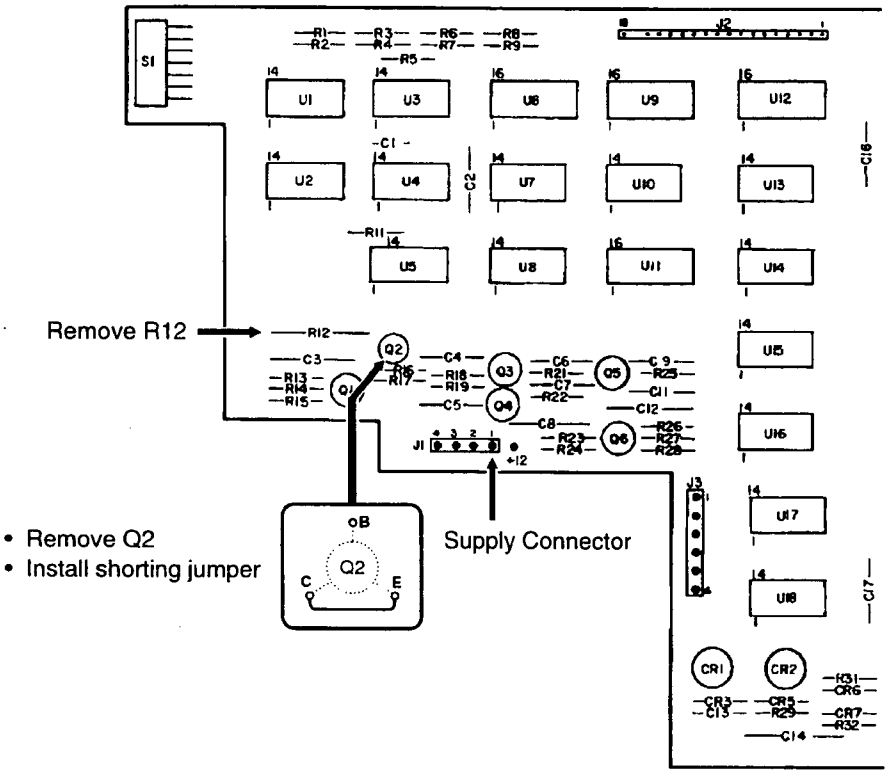
   - Remove Drive Transistor Q2.

   - Install a shorting jumper (included with fan kit) between the collector and emitter holes of the transistor previously removed.



- Remove Q202
- For serial numbers < 2516A09074, install 22Ω 2W resistor
- For serial numbers > 2516A09074, install shorting jumper

03437-66502 Circuit Board



- Remove Q2
- Install shorting jumper

03455-66501 Circuit Board

4. Install the replacement fan in the chassis frame using the two screws provided. Install the fan in the same location as the original fan. Be sure to install the fan so that the direction of air flow is *into* the instrument (the direction of air flow is noted with an arrow on the fan assembly). For easier access to the fan, you can remove the air filter located on the outside of the chassis frame by removing the two screws.

5. The replacement fan has two supply wires, one red and one black. Each wire has a lug to mate with the plastic connector removed from the original fan. Insert the red and black wires into the connector as shown below. Attach the connector to the circuit board (refer to the diagrams on the previous page for correction orientation of the connector on the circuit board).

6. This completes installation of the replacement fan.

   To verify that you have installed the fan properly, look to see if the fan is running when power is applied to the instrument. The fan should be circulating air into the instrument. If the fan does not appear to be working, verify that you have made the correct modifications to the transistor drive circuitry and the supply wires are connected properly as shown above.

7. Replace the top and bottom covers on the instrument.

original 1 Black
2 Brown
3 Red
4 Orange

S E R V I C E N O T E

SUPERSEDES: None

HP 3437A System Voltmeter

Serial Numbers: 0000A00000 / 9999A99999

Fan Replacement Kit available for defective cooling fan

Duplicate Service Notes: 3455A-30

To Be Performed By: HP-Qualified Personnel

Parts Required:

HP P/N	Description
03455-89801	Replacement Fan Kit

Situation:

The part number 3160-0266 has been discontinued by the part manufacturer. Effectively immediately for use in the HP 3437A (& HP 3455A) a new kit , P/N 03455-89801, will be used in its place.

Continued

DATE: June 1996

ADMINISTRATIVE INFORMATION

SERVICE NOTE CLASSIFICATION:

INFORMATION ONLY

AUTHOR:	ENTITY:	ADDITIONAL INFORMATION:
RM	0940	

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Solution/Action:

If the fan, "M1", fails, replace with new replacement fan kit((P/N 03455-89801). Some modification is required (see Replacement Fan Installation Note included in the kit).

Kit Contents:

- Replacement Fan W/Lugs
- Mounting and Support Hardware
- Replacement Fan Installation Note

Change Notes

MANUAL CHANGES

-hp- MODEL 3437A

SYSTEM VOLTMETER

Manual Part Number 03437-90003

ERRATA

Change all "DSA" references in the manual to "SA".

Page 1-2, Table 1-1 (Specifications). Change the Static Accuracy (90 Day and 1 Year Limits) to the following:

Static Accuracy (90 days, 23°C ±5°C)

10 Volt Range ±(0.05% of Reading + 1.6 Digits)
1 Volt Range ±(0.03% of Reading + 1.6 Digits)
.1 Volt Range ±(0.06% of Reading + 1.8 Digits)

Static Accuracy (1 year, ±23°C ±5°C)

10 Volt Range ±(0.05% of Reading + 2.0 Digits)
1 Volt Range ±(0.03% of Reading + 2.0 Digits)
.1 Volt Range ±(0.06% of Reading + 2.2 Digits)

Page 3-11, Paragraph 3-56-c. Change the information under step e as follows:

FUNCTION . . . . . .
RANGE 100
DIAL 10
DC OFFSET 2.5V
OUTPUT LEVEL . . . . . MINIMUM

Page 3-11, Paragraph 3-56-d. Change TIME/DIV in step d from 100μS to 200μS.

Page 5-2, Paragraph 5-11-e. Change step e as follows:

e. Adjust the 3310A output level, and the oscilloscope's trigger, intensity, and vertical position to obtain a display as illustrated in Figure 5-3.

Page 5-4, Figure 5-4 (Bandwidth Test Set-Up). Add the following note to the figure.

The Thermal Converter is assumed to be calibrated.

Page 5-14, Paragraph 5-65-a. Change the RANGE in step a from .1V to 1V.

Page 5-25/5-26, Flowchart A. Change Note 1 on the apron page as follows:

1. THE ANNUNCIATORS AND DIGIT DISPLAY VERIFICATION (SA TEST-8) CAN BE PERFORMED, IF THE SA ROM IS INSTALLED (SEE PARAGRAPH 5-96), IN LIEU OF CHECKING THE OUTGUARD CLOCKS (10 MHz AND SCAN) AND POWER SUPPLY VOLTAGES. A SUCCESFUL TEST E-8 VERIFIES THESE NETWORKS TO BE FUNCTIONING PROPERLY.

Page 5-47/5-48. Change the table on the page to the following:

SA Test	Digit Display	Annunciator Display
1	"0"s	Talk = ON All Others = Low Intensity
2*	Alternating "2","-"	Data Ready, Invalid Prgm, Listen/Talk, Remote, 1.0V, Int, Sec Delay, Hold/Man, Packed = ON. All Others = OFF
3**	"0"s	Talk/Listen = ON All Others = Low Intensity
4	"4"s	ON
5	"5"s	ON
6	"6"s	ON
7*	"7"s	ON
8	Alternating "-",".","0-9"	ON

*Cycle power when leaving test.
**Cycle power before entering test.

Performance Test Card. Change the Static Accuracy limits for the .1V and 10V Ranges as follows:

A. .1 Volt Range ±0.06% of reading + 1.8 digits
C. 1 Volt Range ±0.05% of reading + 1.6 digits

Table 6-3 (Replaceable Parts). Do the following changes in the table.

A1R115 0683-1635 RESISTOR: Fixed 16K 5% 1/4W

Table 6-3 (Replaceable Parts). Add the following to the table.

F1 2110-0012 FUSE: .500A for 100V or 120V operation
F1 2110-0004 FUSE: .250A for 220V or 240V operation
1250-0595 Triax to BNC Adapter

Schematic 1 Changes.

Connect the bottom of E2 to chassis ground instead of guard.

Change the reference designator of the resistor connected to R91 from R15 to R115.

Change the value of R109 to 3.3K.

Connect the bottom of R67 to −14V.

Connect the top of R49 to −14V

Connect U10E as shown in Figure C-1.

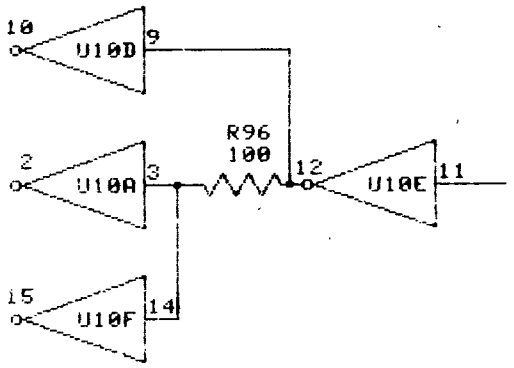

Figure C-1. U10E Connections (Schematic 1)

Component Locator for A1 Assembly. Use component locator shown in Figure C-2.

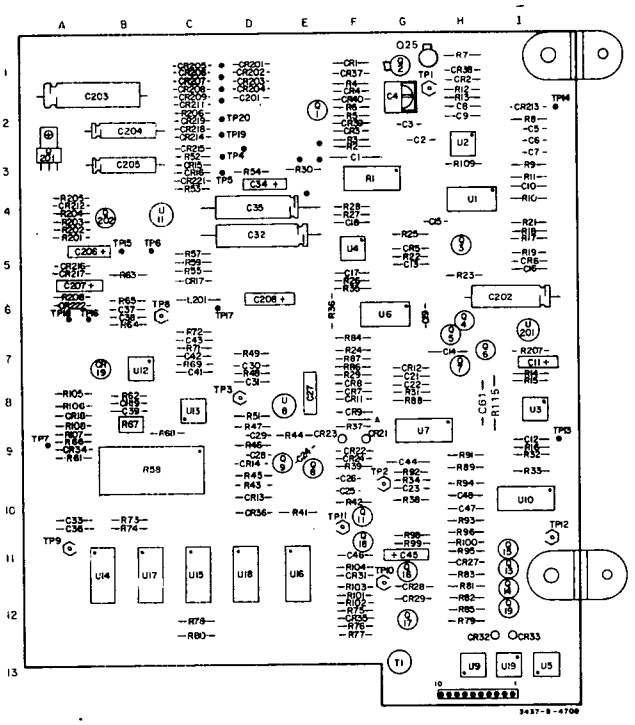

Figure C-2. Component Locator for A1 Assembly

Schematic 3 Changes. Add reference designation "CR104" to diode connected to R127 and C113.

Schematic 4 Changes.

Connect pin 9 of R1 to +12V and change the value of R1 to 2.5k ohms.

Connect pin 16 of U1 to +5V.

Schematic 5 Changes. Connect C218 to CR201 instead of CR204.

CHANGE NO. 1. Applies to All Serial Numbers

Table 6-3. Do the following changes in the table.

A1C4	0121-0128	CAPACITOR: Variable 1.4-9.2pF
A1R35*	0698-4448	RESISTOR: Fixed 53.6k .01 1/8W
A1R35*	0698-3499	RESISTOR: Fixed 40.2k .01 1/8W
A1R109	0683-3225	RESISTOR: Fixed 3300
A1R127	0683-1025	RESISTOR: Fixed 1000
A2U48	1820-1503	IC: MC14007BCP
A2XU24	1200-0569	MPU SOCKET
A3DS7-DS9	1990-0486	LED: Solid State Red
S1	3101-2216	SWITCH: DPDT 4A 250VAC
	5061-0074	CABINET ASSEMBLY

Schematic 1 Changes.

Change C104 to: 1.4-9.2pF.

Change R35 to: R35* 53.6k.

Change R109 to: 3.3k.

Change R127 to: 1000.

CHANGE NO. 2. Applies to Serial Numbers 1630A01371 and Above

Table 6-3. Add the following to the table.

A1C210	0160-3558	CAPACITOR: Fixed .1μF .20 50V
A1C211	0160-3558	CAPACITOR: Fixed .1μF .20 50V

Schematic 5 Changes. Add C210 (.1μF) between pins 1 and 2 of A1J1 and C211 (.1μF) between pins 3 and 4 of A1J1.

CHANGE NO. 3. Applies to Serial Numbers 1630A01491 to 1630A06705

Table 6-3. Change the part number of A2U32 to 1820-0912 (74L193N).

Page 7-13/7-14, Flowchart 2. Change the signatures in step 36 (on apron page) to the following:

U34	Signature
3	P363
6	C6F0
10	F8P1
13	0220

CHANGE NO. 4. Applies to Serial Numbers 1630A02261 and Above

Table 6-3 (Replaceable Parts). Change the part number of A2U124 to 1820-0629(74S112N).

CHANGE NO. 5. Applies to Serial Numbers 1630A02261 to 1630A02360

Table 6-3 (Replaceable Parts). Change the part number and value of A2R130 to 0698-4442 (4420 ohms).

Schematic 3 Changes. Change the value of R130 to 4420 ohms.

CHANGE NO. 6. Applies to Serial Numbers 1630A02261 to 1630A02630

Table 6-3 (Replaceable Parts). Change the part number and value of A2R120 to 0757-0407 (200 ohms).

Schematic 3 Changes. Change the value of R120 to 200 ohms.

CHANGE NO. 7. Applies to Serial Numbers 1630A02361 to 1630A02630

Table 6-3 (Replaceable Parts). Change the part number and value of A2R130 to 0757-0424 (1100 ohms).

Schematic 3 Changes. Change the value of R130 to 1100 ohms.

CHANGE NO. 8. Applies to Serial Numbers 1630A02631 to 1630A04920

Table 6-3 (Replaceable Parts). Change the part number and value of A2R130 to 0683-2225 (2200 ohms).

Schematic 3 Changes. Change the value of R130 to 2200 ohms.

CHANGE NO. 9. Applies to Serial Numbers 1630A02631 and Above

Table 6-3 (Replaceable Parts). Change the part number and value of A2R120 to 0698-4453 (402 ohms).

Schematic 3 Changes. Change the value of R120 to 402 ohms.

CHANGE NO. 10. Applies to Serial Numbers 1630A03891 and Above

Table 6-3 (Replaceable Parts). Do the following changes in the table.

Add the following:

A2CR250 to CR253	1901-0039	DIODE: Switching 50V
A2R250	0757-0443	RESISTOR: Fixed 11k .01 1/8W
A2R251	0690-2211	RESISTOR: Fixed 220 .1 1W
A2R252	0690-2211	RESISTOR: Fixed 220 .1 1W

Change the following:

A2R207	0698-3497	RESISTOR: Fixed 6.04k .01 1/8W
A2R208	0698-4202	RESISTOR: Fixed 8.87k .01 1/8W
A2R213	0698-4202	RESISTOR: Fixed 8087k .01 1/8W
A2R232	0698-3279	RESISTOR: Fixed 4.99k .01 1/8W
A2R234	0698-3279	RESISTOR: Fixed 4.99k .01 1/8W

Delete the following:

A2CR205	1901-0040	DIODE: SI
A2R212	0683-2235	RESISTOR: 22k .05 1/4W

Schematic 3 Changes. Refer to Figure C-3 for the changes.

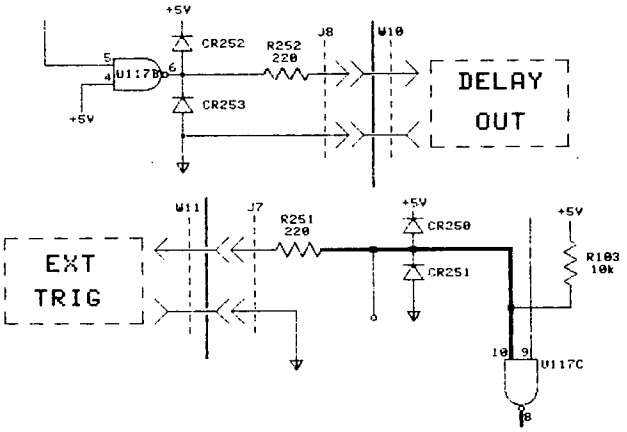

Figure C-3. Schematic 3 Changes (Change No. 10)

Schematic 5 Changes. Do the following changes.

Remove CR205 and replace it with a short.

Remove R212 and replace it with a short.

Connect an 11k ohm resistor (R205) between pin 5 of U202 and common.

Change the values of the following resistors.

R207 - 6.04k
R208 - 8.87k
R213 - 8.87k
R232 - 4.99k
R234 - 4.99k

CHANGE NO. 11. Applies to Serial Numbers 1630A03891 and Above

Table 6-3 (Replaceable Parts). Do the following changes in the table.

Add the following:

A1R220	0683-8235	RESISTOR: Fixed 82k

Change the following:

A2R237	0757-0408	RESISTOR: Fixed 243 .01 1/8W
A2U24	1820-1692	NANOPROCESSOR

Schematic 1 Changes. Refer to Figure C-4 for the changes.

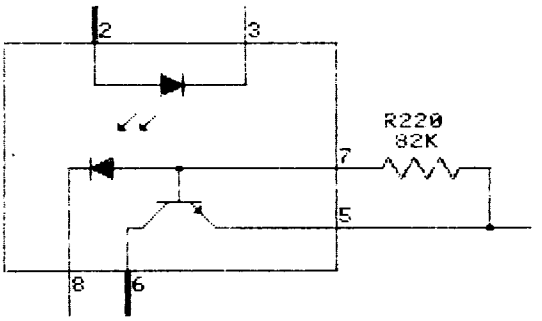

Figure C-4. Schematic 1 Changes (Change No. 11)

Schematic 5 Changes. Do the following changes.

Change R237 from a star value to 243 ohms.

Add the following note to the apron page.

NOTE

A 243 ohm resistor has to be selected for R237 if A2U24 (Nanoprocessor) with part number 1820-1692 is used for replacement.

CHANGE NO. 12. Applies to Serial Numbers 1630A04921 and Above.

Table 6-3 (Replaceable Parts). Change the part number and value of A2R130 to 0698-4435 (2.49k ohms).

Schematic 3 Changes. Change the value of R130 to 2490 ohms.

CHANGE NO. 13. Applies to Serial Numbers 1630A06495 and Above.

Schematic 5 Changes. Change the wiring on the voltage selector switches as shown in Figure C-5.

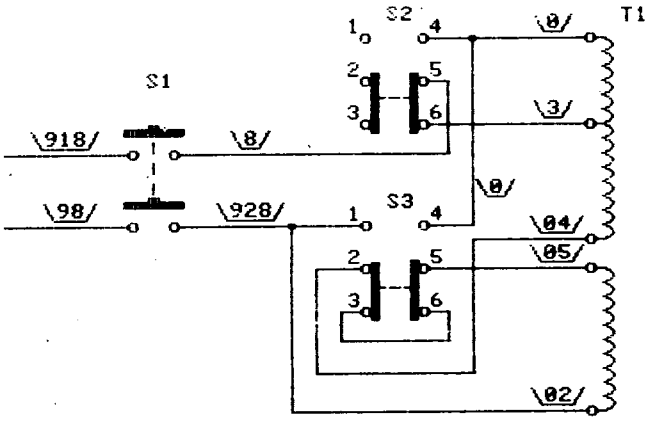

Figure C-5. Schematic 5 Changes (Change No. 13)

CHANGE NO. 14. Applies to Serial Numbers 1630A06666 and Above

Table 6-3 (Replaceable Parts). Change the part number of A1U5 to 1990-0732.

Schematic 1 Changes. Change the U5 opto isolator as shown in Figure C-6.

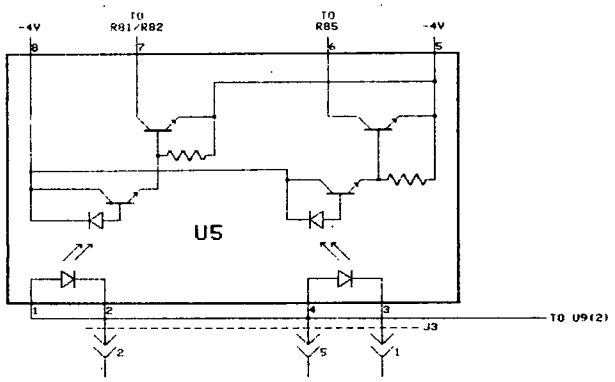

Figure C-6. Schematic 1 Changes (Change No. 14)

CHANGE NO. 15. Applies to Serial Numbers 1630A06706 and Above

Table 6-3 (Replaceable Parts). Change the part number of A2U32 to 1820-01114.

Schematic 2 Changes. Refer to Figure C-7 for the changes.

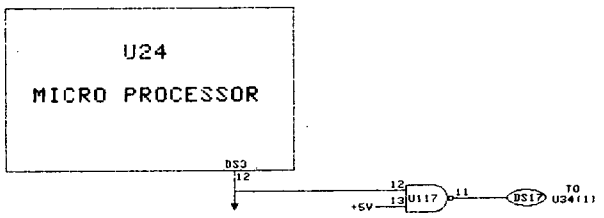

Figure C-7. Schematic 2 Changes (Change No. 15)

CHANGE NO. 16. Applies to Serial Prefix 2516 and Above

Title Page. Add the following caution to the title page.

CAUTION

Your instrument may have either metric or English hardware. **DO NOT** *intermix the different hardware or damage to the instrument may result. Follow the cautions in the manual that pertain to the different hardware. Contact your local HP Office if more information is needed.*

Section I, Paragraph 1-14. Change the paragraph to the following:

1-14. The following options are available for the HP 3437A.

Option	-hp- Part Number (Prefix 1630 and Below)	Description	-hp- Part Number (Prefix 2516 and Above)
907	5060-9835	Front Handle Kit	5061-9435
908	5020-8802	Rack Adapter Kit	5021-5802
908	2510-0192	Rack Mount Kit	0515-1331

CAUTION

Your instrument may have either metric or English hardware. **DO NOT** *intermix the different hardware or damage to the instrument's frame and cabinet may result. For instruments with with serial prefix 2516 and above, use metric handle/rack mounting hardware, as listed above. For instruments with serial prefix 1630 and below, use English handle/rack mounting hardware also as listed above. Contact your local HP Office if more information is needed.*

Section VI, Table 6-3 (Replaceable Parts). Do the following changes in the table.

Reference Designation	HP Part Number	Qty	Description
Change:			
	5060-9843	1	Bottom Cover (For Serial Prefix 1630 and Below)
	5061-0088	1	Fr. Handle Kit (For Serial Prefix 1630 and Below)
	5060-9831	1	*Top Cover (For Serial Prefix 1630 and Below)
	5060-9907	2	*Side Cover (For Serial Prefix 1630 and Below)
Add:			
	5061-9443	1	Bottom Cover (For Serial Prefix 2516 and Above)
	5061-9688	1	Fr. Handle Kit (For Serial Prefix 2516 and Above)
	5061-9431	1	*Top Cover (For Serial Prefix 2516 and Above)
	5061-9507	2	*Side Cover (For Serial Prefix 2516 and Above)

MANUAL CHANGES

-hp- MODEL 3437A

SYSTEM VOLTMETER

Manual Part Number 03437-90012

CHANGE NO. 1. Applies to Serial Prefix 2516 and Above

Title Page. Add the following caution to the title page.

CAUTION

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CAUTION

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CHANGE NO. 2. Applies to All Serial Numbers

Add the attached "DECLARATION" to the manual.

MANUAL CHANGES

MODEL 3437A

SYSTEM VOLTMETER

Manual Part No. 03437-90010

► New or Revised Item

ERRATA.

Page 1-2, Table 1-1. Refer to Voltage Measurement Characteristics - Dynamic Accuracy.

Change:

	Range	Step Input	mV Within Final Value	Time
From	10 volt	10 volt	±20 mV	7.5 μs
To	10 volt	10 volt	±30 mV	7.5 μs
From	1 volt	1 volt	±2 mV	1.5 μs
To	1 volt	1 volt	±3 mV	1.5 μs
From	1 volt	.1 volt	±200 mV	25 μs
To	.1 volt	.1 volt	±200 mV	25 μs

Refer to Common Mode Rejection Ratio.

Change to read: ⩾75 dB (1 kΩ unbalance in low input lead @ 60 Hz).

Page 1-2, Table 1-2. Refer to Humidity Range. Change > 95% to < 95%.

Page 2-1, Paragraph 2-13. Change 55° C to 50° C.

MANUAL CHANGES

HP MODEL 3437A

SYSTEM VOLTMETER

Manual Part Number 03437-90012

CHANGE NO. 1. Applies to Serial Prefix 2516 and Above

Title Page. Add the following caution to the title page.

CAUTION

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CAUTION

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CHANGE NO. 2. Applies to All Serial Numbers

Add the attached "DECLARATION" to the manual.

HEWLETT PACKARD

Herstellerbescheinigung

Hiermit wird bescheinigt, daβ das Gerät/System HP 3437A in Übereinstimmung mit den Bestimmungen von Postverfügung 1046/84 funkentstört ist.

Der Deutschen Bundespost wurde das Inverkehrbringen dieses Gerätes/Systems angezeigt und die Berechtigung zur Überprüfung der Serie auf Einhaltung der Bestimmungen eingeräumt.

Zusatzinformation fur Meβ- und Testgeräte

Werden Meβ- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Meβaufbauten verwendet, so ist vom Betreiber sicherzustellen, daβ die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that the equipment HP 3437A is in accordance with the Radio Interference Requirements of Directive FTZ 1046/84. The German Bundespost was notified that this equipment was put into circulation, the right to check the series for compliance with the requirements was granted.

Additional Information for Test- and Measurement Equipment

If Test- and Measurement Equipment is operated with unscreened cables and/or used for measurements on open set-ups, the user has to assure that under operating conditions the Radio Interference Limits are still met at the border of his premises.

Inter Office Service Memo

ENGLEWOOD

RODENBAUGH BERNARD C

3437A-2-77

INTER-OFFICE SERVICE MEMO

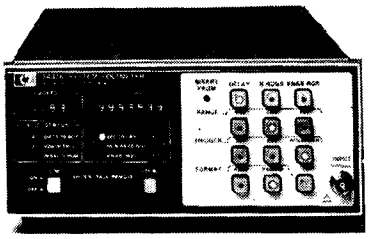
Date: February 18, 1977

TO: All Service Offices

FROM: R. Alan Snyder, Loveland Instrument Division

SUBJECT: 3437A Product Support Plan

I. DESCRIPTION.



The -hp- 3437A Systems Voltmeter is a high-speed HP–IB compatible 3½ digit voltmeter with sampling speeds of more than 5000 readings per second.

The -hp- 3437A uses the sample and hold/successive approximation technique, by using some new circuit innovations, it is able to achieve higher speed capability. This voltmeter is designed around a new control microprocessor which provides many added features over traditionally designed instruments. This includes such things as programmable delay between readings, multiple readings in a burst mode, displayed HP–IB status, and a troubleshooting mode.

RAS/kkz

2/77-09

HEWLETT hp PACKARD

Major Specifications.

Ranges:

Ranges	Max. Display	Overload Reading
10 V	± 19.98	± 99.99
1 V	± 1.998	± 9.999
0.1 V	± 1.998	± .9999

Performance:

Static Accuracy (90 days, 23° C ± 5° C):

10 V Range: ± 0.05% of reading ± 1.6 digits
1 V Range: ± 0.03% of reading ± 1.6 digits
0.1 V Range: ± 0.06% of reading ± 1.8 digits

Static Accuracy (1 year 23° C ± 5° C):

10 V Range: ± 0.05% of reading ± 2 digits
1 V Range: ± 0.03% of reading ± 2 digits
0.1 V Range: ± 0.06% of reading ± 2.2 digits

Static Accuracy Temperature Coefficient (0° C–50° C):
± 0.002% of reading/° C ± 0.05 digits/° C

Delay:

N Rdgs = 0 or 1
DELAY (Setting): 0 to .9999999 sec. in .1 μs steps
N Rdgs > 1 (Remote and a zero delay listener)
ASCII DELAY (Setting): 277.8 μsec to .9999999 sec in .1 μs steps
Packed DELAY (Setting): 175.4 μsec to .9999999 sec in .1 μs steps

Number of Readings (N Rdgs)*

N Readings: 0** to 9.999
*Readings are not internally stored.
**For N = 0 the 3437A operates in delay mode only.

Input Bandwidth (3 dB)

10 V Range: 1.0 MHz
1 V Range: 1.1 MHz
0.1 V Range: 40 kHz

II. REPAIR STRATEGY.

The -hp- 3437A circuit boards A1, A2, and A3 will be covered by the Blue Stripe Exchange program; but where rapid turn around time is not a major factor, component level repair can be performed. To facilitate both component level repair and rapid board level repair for the Systems customer, a Service Kit containing a complete set of boards, miscellaneous key components and instrument verification software for the 9825A Calculator will be available. To further enhance success of component level repair the 3437A has Logic Signature Analysis capability, (formerly Data Stream Analysis). The use of the Logic Tracer from Santa Clara Division will provide an extra measure of repairability.

A trio of accessory items is also available. The 34113A and 34114A are performance interface devices and are necessary to perform the full performance test on the -hp- 3437A. The 34115A is a special test ROM which when used in place of one of the -hp- 3437A's program ROMs will allow one of the L.S.A.. function in the 3437A to assist in digital troubleshooting. These three accessories are available separately or as part of the 44037A Service Kit for the -hp- 3437A.

III. SERVICE TRAINING.

Service Aspects of the -hp- 3437A will be covered in the Spring Factory Seminars. On-site seminars can be arranged if the need arises.

IV. DOCUMENTATION.

All -hp- 3437A's are being delivered with a complete Operating and Service Manuals, including schematics, a very thorough troubleshooting section describing the use of the L.S.A. technique and some simple unique applications.

V. BASIC SERVICE INFORMATION.

A. The calculated MTBF (Mean Time Between Failures) is 5000 hours.

B. When handling the boards in the 3437A, exercise care to avoid static discharge which could damage sensitive components.

VI. PARTS STOCKING RECOMMENDATION.

Parts stocking recommendations have been prepared for the 3437A, and the parts are in stock at CPC and PCE.

Any comments or questions regarding the 3437A and its Service Support Plan should be directed to LID Customer Service.

INTER-OFFICE SERVICE MEMO

Date: February 24, 1977

SUPERSEDES
3437A-1-77

TO: Field Service Technicians

FROM: R. Alan Snyder, Loveland Instrument Division

SUBJECT: Noisy Fan Replacement

Due to a change in the manufacturing process of the 3437A Cooling Fan, we are recommending that instruments with serial numbers below 1630A00135 undergoing service have this fan replaced Warranty Only (WO). The part number is 3160-0266 and has a longer lifetime than the originally installed fan. Customers having warranty repair done for any reason should be given a new fan whether or not they have experienced fan problems.

RAS/kkz

2/77–09

HEWLETT hp PACKARD

DSA TEST ROM
OPERATING NOTE

I. INTRODUCTION.

The DSA test ROM is used to force the 3437A Microprocessor to execute test routines that result in the generation of repetitive data patterns throughout the logic circuitry. The data patterns are then characterized (4-bit alphanumeric code) by the -hp- Model 5004A Logic Tracer and are referred to as test signatures.

The test signatures are compared to the signatures documented in the 3437A Operating and Service Manual. Corresponding signatures indicate the 3437A is operating properly, while non-corresponding signatures indicate an instrument failure

II. OPERATION.

Since the 3437A uses more than 2000 (of the possible 2048) words of program instruction for normal instrument operaion, an additional ROM (DSA test ROM) is required to implement the DSA technique. When troubleshooting the logic circuits, the program control ROM that is socket mounted (U41) is replaced with the DSA test ROM. Complete troubleshooting instructions are documented in the 3437A Operating and Service Manual.

NOTE

Insure that the DSA test ROM (when installed) is orientated the same as U41; otherwise the test ROM may be damaged.

III. PARTS LIST.

Description	-hp- Part No.
DSA Test ROM	34115A

34115-90000 (Microfiche Part No. 34115-90050) 1/77-09

Printed in U.S.A.

HEWLETT hp PACKARD

For more information, call your local HP Sales Office or East (201) 265-5000 • Midwest (312) 255-9800 • South (404) 434-4000 West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, 1217 Meyrin-Geneva

PERFORMANCE-TEST TRIGGER INTERFACE
OPERATING NOTE

I. INTRODUCTION.

The performance-test trigger interface illustrated in Figure 1) level shifts the dc component of the -hp- Model 180A Oscilloscope main gain output so that the output waveform occurs within the specified range of the 3437A external trigger input (Figure 2).

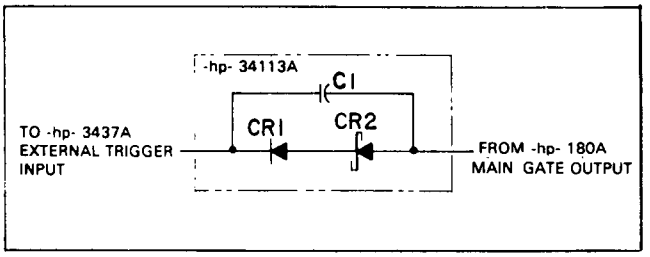


Figure 1. Performance Test Trigger Interface.

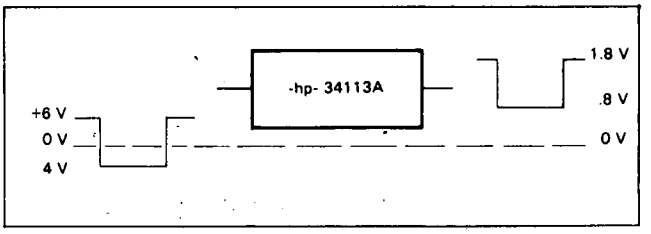


Figure 2. Trigger Interface Implementation.

II. OPERATION.

The Model 34113A Trigger Interface is required for the 3437A dynamic accuracy performance test. Complete operating instructions are contained in the 3437A Operating and Service Manual.

III. PARTS LIST.

The following parts are contained in the Model 34113A:

Description	-hp- Part No.
C1	0160-3847
CR1	1901-0040
CR2	1901-0535
Casting	10014-20102
Housing	10014-24102
BNC Connector	1250-1233
	1250-0083

34113-90002(Microfiche Part No. 34113-90052) 8/77-09

Printed in U.S.A.

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For more information, call your local HP Sales Office or East (201) 265-5000 • Midwest (312) 255-9800 • South (404) 434-4000
West (213) 877-1282. Or, write: Hewlett-Packard, 1501 Page Mill Road, Palo Alto, California 94304. In Europe, 1217 Meyrin-Geneva