HEWLETT-PACKARD

HP 82939A

SERIAL INTERFACE INSTALLATION AND THEORY OF OPERATION MANUAL

HP 82939A
Serial Interface
Installation and Theory of Operation Manual

June 1981

82939-90001 Rev. B 6/81

Printed in U.S.A.

Contents

Figures

Tables

Section 1

General Information

Introduction

The HP 82939A Serial Interface provides serial data communications between the Hewlett-Packard Series 80 computer and a data communications device. All references to the HP-85 computer contained herein should be expanded to denote all HP Series 80 computers.

This section contains a background on data communications, description of the RS-232C standard, description of the HP-85 implementation of the RS-232C standard, specifications, options and cable functions.

Succeeding sections contain installation information and theory of operation.

Background on Data Communications

Data Comm is the means by which data is transmitted from one point to another. A computer can be hooked directly to a remote terminal using special transmission lines, but for long distances, this becomes impractical. Although common telephone lines can be used, there is one drawback – telephone lines are made for analog signals (e.g., the voice), not digital signals like those generated by a computer. A modem*, or a signal converter, must be used for converting signals from digital to analog and vice versa.

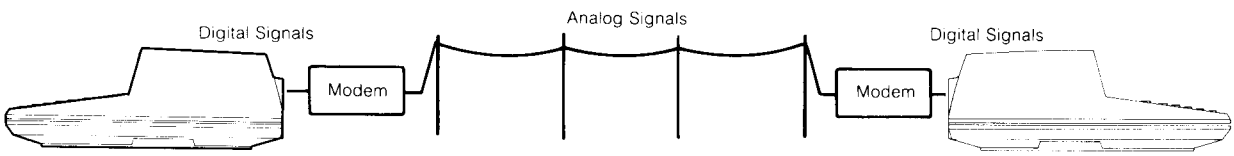


Figure 1-1. Modem Conversion Process

* "Modem" is a contraction of the words modulator and demodulator.

The modem converts outgoing digital signals to analog form and incoming analog signals to digital form (Figure 1-1). Since there are many different ways to do these conversions, it is important that data converted to analog is re-converted to the correct digital form. So, the modem on one end of the telephone line must understand, or be compatible with, the modem on the other end.

Modems are classified as asynchronous or synchronous, by mode, by data rate and by modulation technique.

Asynchronous transmission is often referred to as START-STOP. This is because the data is sent serially one character at a time along with start and stop bits. These start and stop bits are used to separate characters and to synchronize the receiver with the transmitter for each character since the modem itself does not provide clocking information. When the signal elements or bits of a character travel in sequence over the line, it is called a serial transmission. With the start and stop bits added, this is called serial start-stop or serial asynchronous, meaning each character is individually synchronized. This type of transmission is normally used at data rates up to 2,400 bits per second.

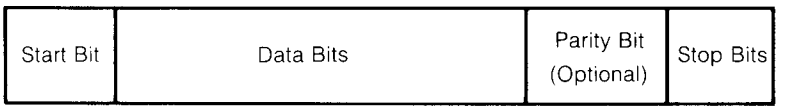


Figure 1-2. Asynchronous Mode Transmission

Modems can operate in three different modes:

- Simplex, where data is sent only or received only,
- Half-duplex, where data can be both sent and received, but not simultaneously,
- Full-duplex, where data can be simultaneously transmitted and received.

Half-duplex is normally used for high-speed batch transmission where fewer line turn-arounds are needed and full channel capacity (bandwidth) is needed for transmission in one direction. Full-duplex is often used for timesharing, even though it seldom occurs that data is truly being transmitted and received simultaneously. The one case where simultaneous transmission does occur is when a "break" is sent to the timeshare computer. One reason for full-duplex timesharing is to provide transmission error checking by having the computer "echo" or re-transmit each character input from the terminal.

The most commonly referenced operational characteristic of a modem is its speed or data rate expressed in bits per second (bps) or baud. For simple low-speed modulation techniques, one bit per second into a modem may equal one baud on the analog side. However, at higher data rates with more complex modulation techniques, it is possible to encode more than one bit per signal change (or baud) on the telephone line. In this case, bits per second (into the modem) and baud (on the telephone line) are two different units.

RS-232C

One of the standards adopted by the EIA for use with data communications was the Electronic Industries Association RS-232C, Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange. The RS-232C is the most common data communications protocol in use today. The International Telegraph and Telephone Consultative Committee, or CCITT, Standards V.24 and V.28, parallel the EIA RS-232C and provide a compatible international standard. RS-232C has been the most successful interfacing standard implemented to date.

A lengthy description of the RS-232C standard is contained in Appendix C. Appendix D contains a table of RS-232C functions, listed by pin number.

HP 82939 Description

The HP 82939 Serial I/O Interface allows the HP-85 calculator to communicate with serial asynchronous data communication devices. The HP 82939 is equipped with both RS-232C and 20 mA current loop drivers and receivers for the data transmitter and receiver. Data can be transferred at standard baud rates of 50 to 9,600. A universal asynchronous receiver/transmitter integrated circuit (UART) is used to manipulate data and provide the basic hardware protocol for asynchronous operation. The interface is available in cable configurations which allow the HP-85 to act as either a data terminal or the digital portion of a modem.

Plug-in ROMs

The HP 82939A interface requires the use of one of the following ROMs:

- I/O ROM (part number 00085-15002).
- Plotter/Printer ROM (part number 00085-15003).

The ROMs fit into a ROM drawer which slides into any of the four I/O slots on the HP Series 80 computer.

Specifications

Temperature: 0° C – 55° C (32° F – 131° F)

Humidity: 0 – 80%

Generally speaking, any environment in which an HP personal computer can operate will also be acceptable for the 82939 serial interface. If extreme environmental conditions exist, or if there is a question about specifications not listed here, consult your local HP sales and service office.

Cable Options

The 82939 interface must use one of the available option cables. The option number determines which cable is provided with the interface. Table 1-1 describes which equipment is included with the available options.

Table 1-1. Cable Options

Option	Connector	Purpose
000 (Standard)	25 Pin Female RS-232C	For connecting an HP-85 to data terminal equipment.
001	25 Pin Male RS-232C	For connecting an HP-85 to a modem or to other data communications equipment.
002	None	For connecting an HP-85 to 20 mA current loop equipment.

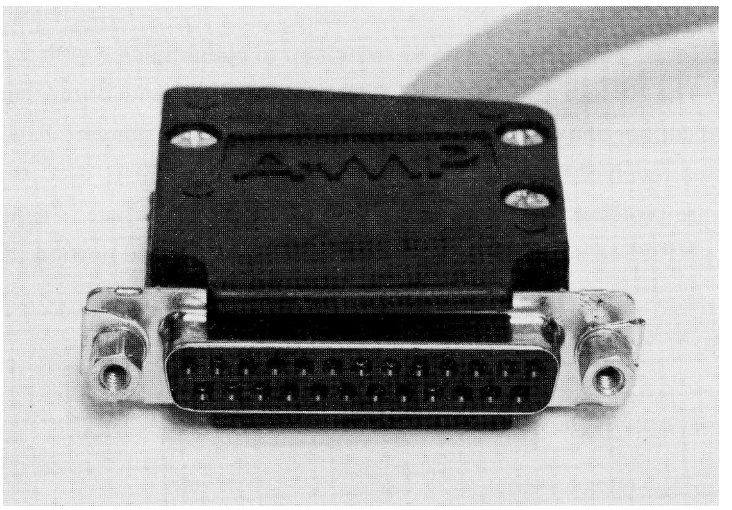
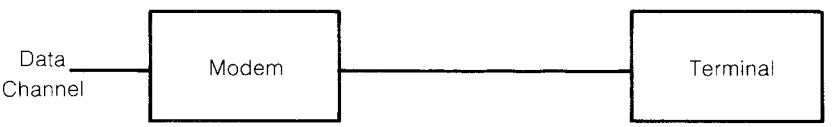
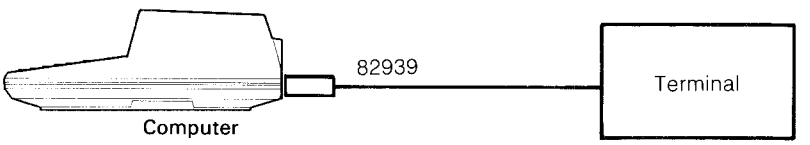


Figure 1-3. Standard Cable Connector

Using the standard interface cable, the HP-85 takes the place of a modem or computer communicating with a terminal.



Using Normal Data Communications



Using HP-85/82939 (Standard)

Figure 1-4. Using HP-85/82939 (Standard)

The 82939 option 001 interface cable is shipped with a 2-metre (6.5 ft) cable terminated with a standard male EIA 25-pin connector. The option 001 interface is connected between the HP-85 and a modem.

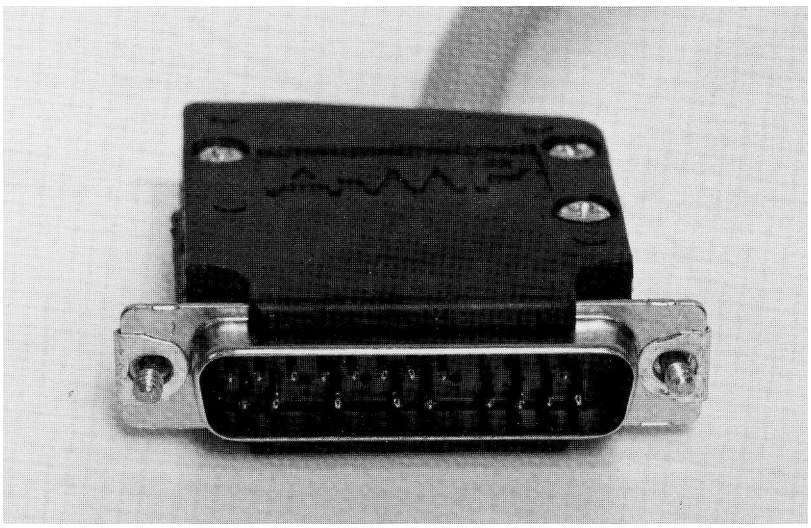
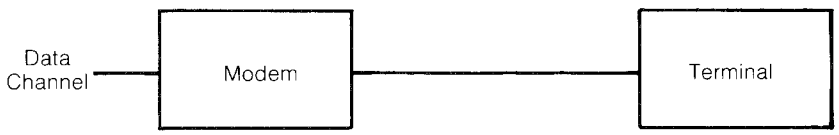


Figure 1-5. Option 001 Cable Connector

Using the option 001 interface cable, the HP-85 acts as a data terminal connected to a modem.



Using Normal Data Communications

Using HP-85/82939 (Option 001)

Figure 1-6. Using HP-85/82939 (Option 001)

Figure 1-7 shows a typical point-to-point installation using the 82939 interface. Note that one computer uses the standard connector, while the other is using option 001.

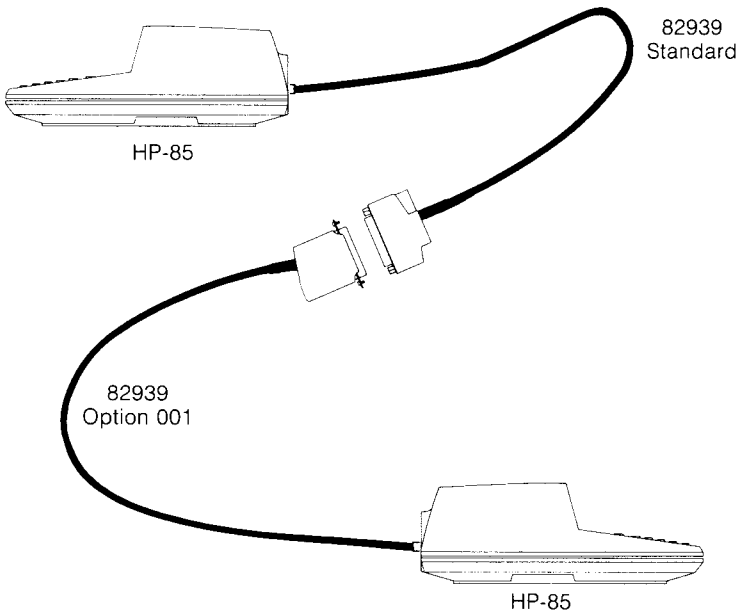


Figure 1-7. Point-to-Point System

Figure 1-8 shows a typical installation using modems to convey information over commercial telephone lines. Both computers in this example use the standard connector.

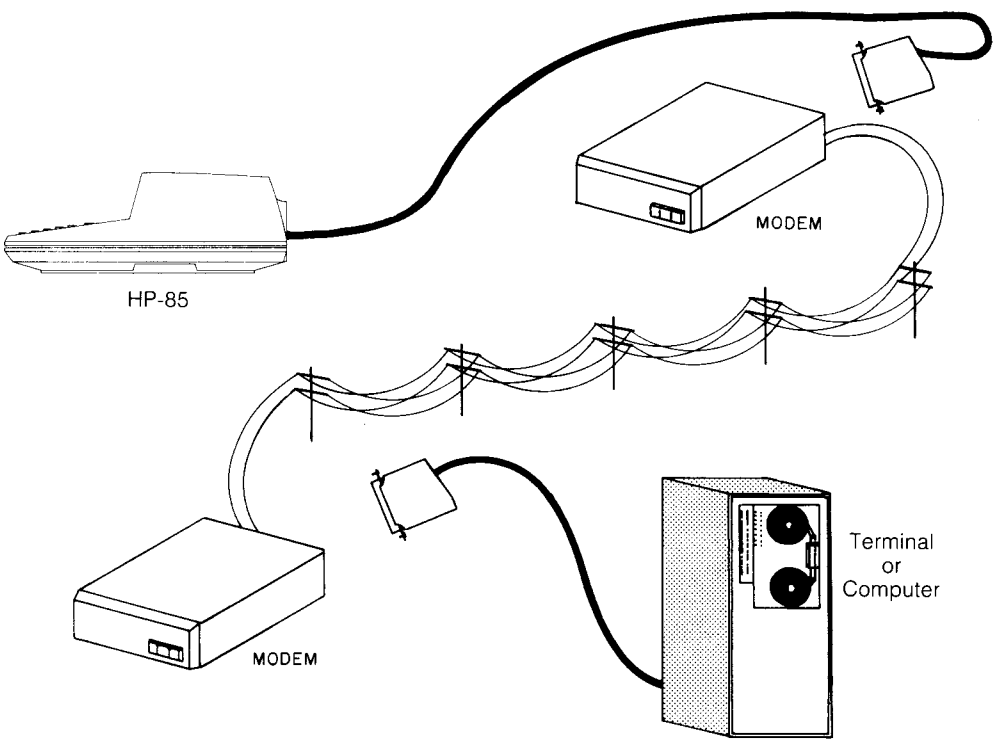


Figure 1-8. Typical Data Communications System With Modems

Here is a list of the signal lines and the corresponding connector pin numbers and wire colors used in the standard and option 001 cables.

Table 1-2. Cable Signals

82939 Standard Cable
(Female Connector Connects to Terminal)

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	Device to 82939
3	Received Data	82939 to Device
4	Request to Send	Device to 82939
5	Clear to Send	82939 to Device
6	Data Set Ready	82939 to Device
7	Signal Ground	N/A
8	Carrier Detect	82939 to Device
9 – 11	Unused	
12	Unassigned	
13 – 18	Unused	
19	Unassigned	
20	Data Terminal Ready	Device to 82939
21 – 22	Unused	
23	Data Rate Select	Device to 83939
24 – 25	Unused	

82939 Option 001 Cable
(Male Connector Connects to Modem)

Pin No.	Signal Name	Signal Direction
1	Protective Ground	N/A
2	Transmitted Data	82939 to Device
3	Received Data	Device to 83939
4	Request to Send	82939 to Device
5	Clear to Send	device to 82939
6	Data Set Ready	Device to 82939
7	Signal Ground	N/A
8	Carrier Detect	Device to 82939
9 – 11	Unused	
12	Unassigned	
13 – 18	Unused	
19	Unassigned	
20	Data Terminal Ready	82939 to Device
21 – 22	Unused	
23	Data Rate Select	82939 to Device
24 – 25	Unused	

82939 Option 002 Cable
(Unterminated Cable Connects to Current Loop Device)

Wire Color	Signal Name	Signal Direction
Shield	Protective Ground	N/A
Green	Logic Ground	N/A
Black	+ CL Received Data	Device to 82939
Red	– CL Received Data	82939 to Device
White	– CL Transmitted Data	82939 to Device

Section 2

Installation

Unpacking and Inspection

If the shipping carton is damaged, ask the carrier's agent to be present when the interface is unpacked. If the interface is damaged or fails to meet electrical specifications, immediately notify the carrier and the nearest HP sales and service office. Retain the shipping carton for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your interface without waiting for the claim against the carrier to be settled.

Conditions Set by User

Many conditions are determined by the position of switches set by the user. Table 2-1 contains a list of these conditions, the choices allowed by the switches and the factory settings of each.

Table 2-1. Conditions Set by User

Function	Choices	Factory Setting
Select Code	Three switches allow choice of eight codes.	10 (111)
Baud Rate	Four switches select one of 16 baud rates.	300 (0110)
Character Word Length	Two switches select among 5-, 6-, 7- or 8-bit word length.	7 (10)
Number of Stop Bits	One switch chooses one or two stop bits.	1 (0)
Parity Enable	One switch to enable parity.	Enable (1)
Parity Select	Select odd or even parity.	Odd (0)
Parity Stick	One switch to make parity bit always 0 or always 1, according to parity select switch.	No (0)
Autohandshake	One switch to recognize or ignore "Clear to Send" and "Carrier Detect".	Off (0)

Note that all of these switches except Select Code may be overridden by software, once the interface is in operation.

Since these switches are located inside the interface housing, changing any of them requires disassembly of the housing. If this is done, refer to the following disassembly procedure to gain access to the switches.

After the switches have been changed, their position can be determined without disassembling the interface by reading the appropriate status register (see Table 3-1).

Disassembly

Refer to Figure 2-1 to see how the interface parts fit together. Place the interface on a flat surface with the side having the seven screws facing upward and the cable coming out to the left. Then use the following steps to disassemble the interface.

1. Using a Pozidriv screwdriver, remove the screws and set them aside.
2. Hold the interface parts together and turn it over so that the seven screw holes are facing downward and the cable is still coming out to the left.
3. Hold the cable strain relief in place and remove the top half of the interface housing.

If you have followed the above steps, switch S1 should be oriented as shown in the following figures. If it isn't, orient it as illustrated before identifying the switch segments.

When you re-assemble the interface, reverse the above procedure, making sure the ground clip is in place. The ground clip should be under the circuit board when the component side is up.

Switch Settings

As previously noted, many interface functions are switch selectable, and preset at the factory. Switch blocks S1 and S2 are used for this purpose.

Once the interface is disassembled, any switch settings may be verified or changed by referring to the appropriate section of the following material.

They may have either slide or rocker switches. Both types are illustrated in the factory preset positions.

CAUTION

If you change any of the factory settings, make sure that you change the proper switch segments. Do not disturb the settings of adjoining switches. Use a pencil point or similar object for changing switch settings.

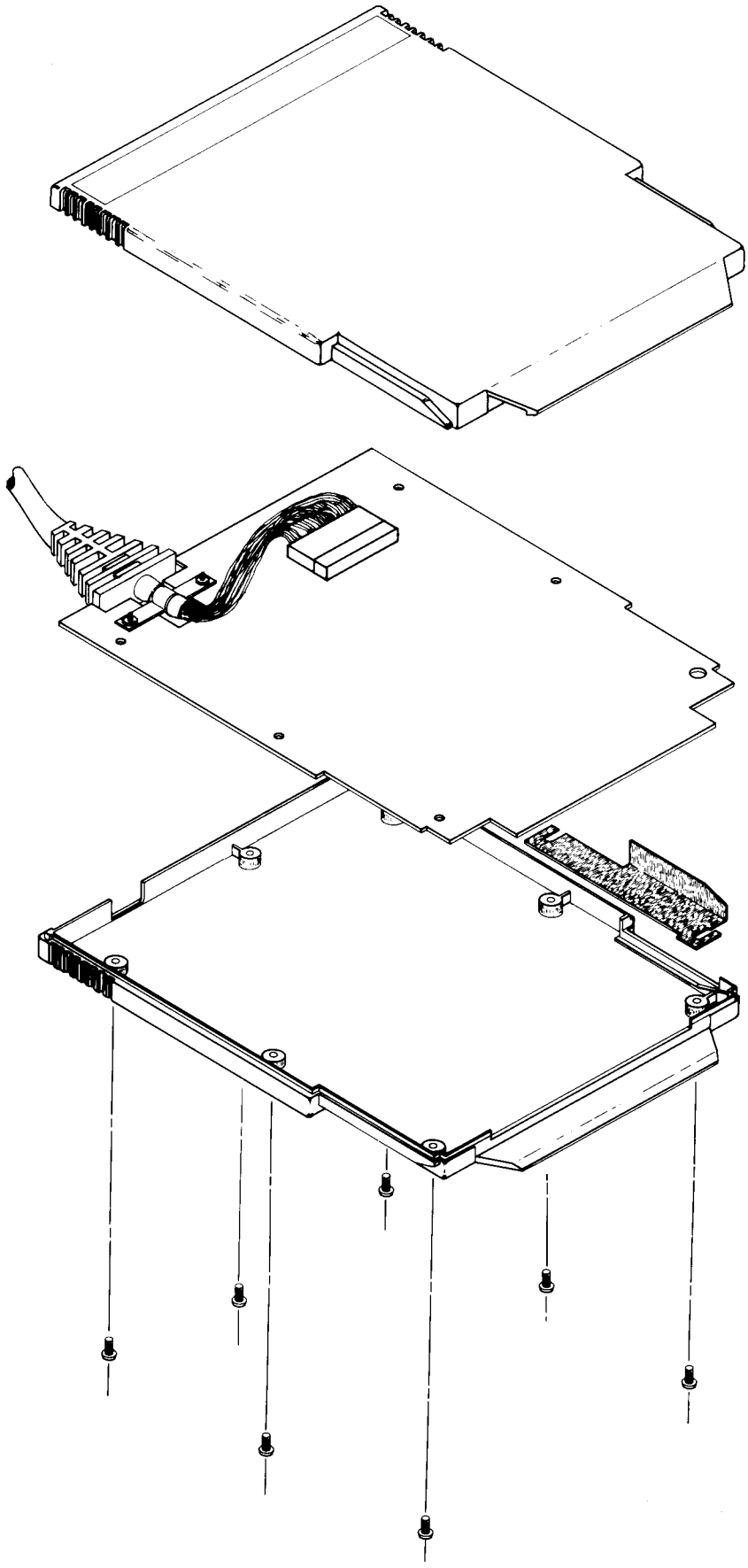
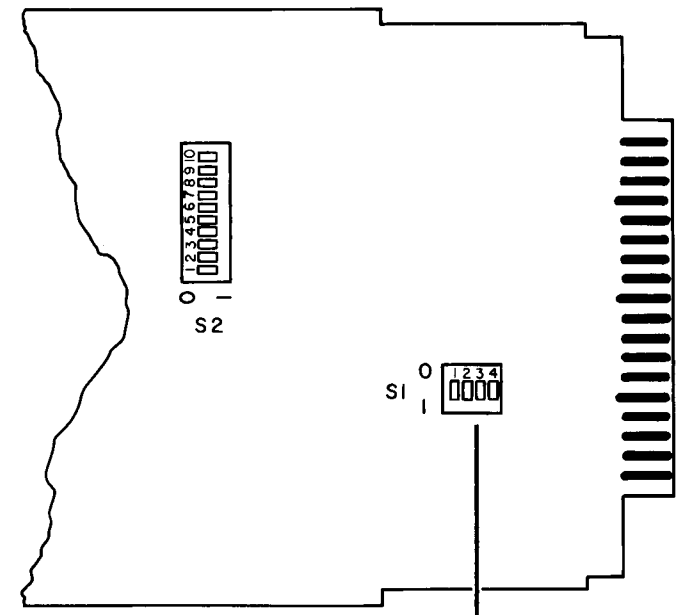


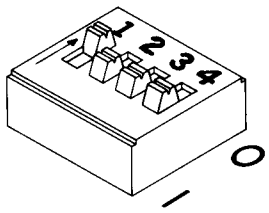
Figure 2-1. Disassembly



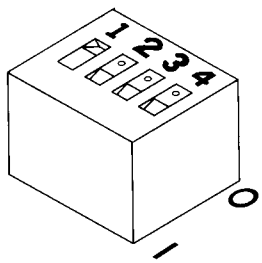
Switch 1

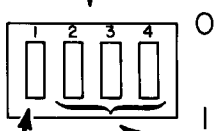
Segment 1:	AHS	Autohandshake
Segment 2:	SC2	Select code 2
Segment 3:	SC1	Select code 1
Segment 4:	SC0	Select code 0

Preset Positions



OR

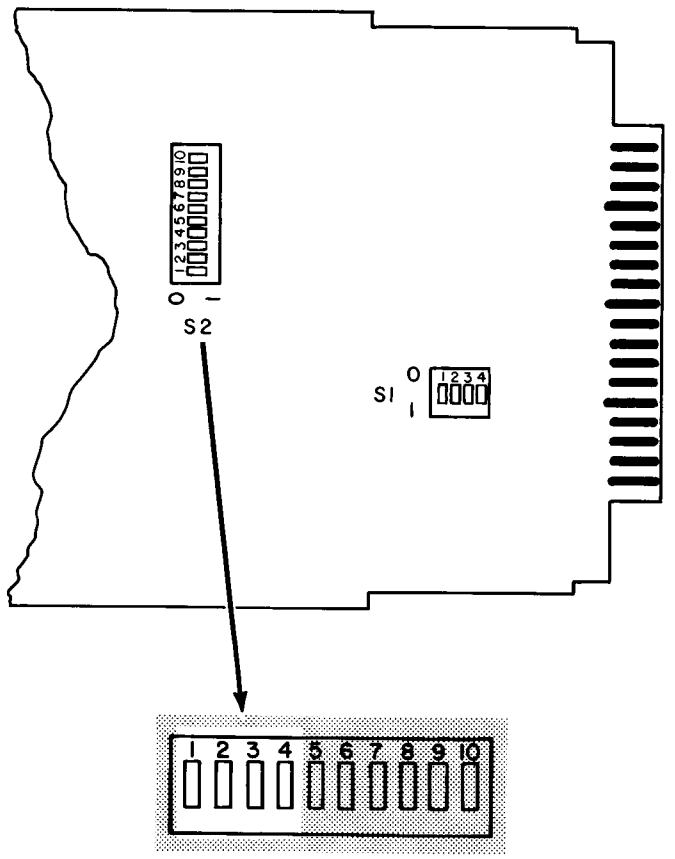




Autohandshake	S1(1)
PRESET → Ignore	0
Enable	1

Select Code Bit	S1(2)	S1(3)	S1(4)
3	0	0	0
4	0	0	1
5	0	1	0
6	0	1	1
7	1	0	0
8	1	0	1
9	1	1	0
PRESET → 10	1	1	1

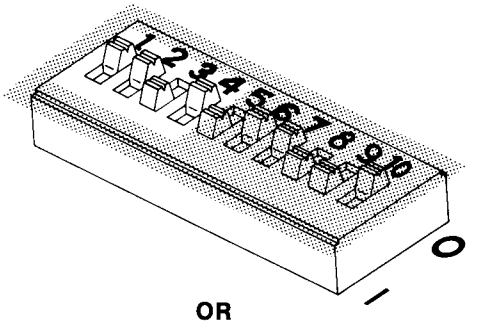
Figure 2-2. Auto Handshake and Select Code Switches



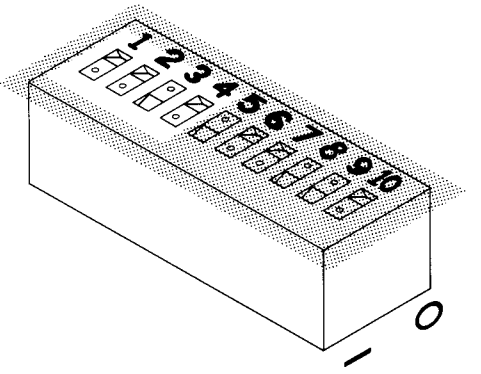
Switch 2

Segment 1:	SP	Parity transmit
Segment 2:	EPS	Select parity
Segment 3:	PEN	Parity enable
Segment 4:	STB	Number of stop bits

Preset Positions



OR



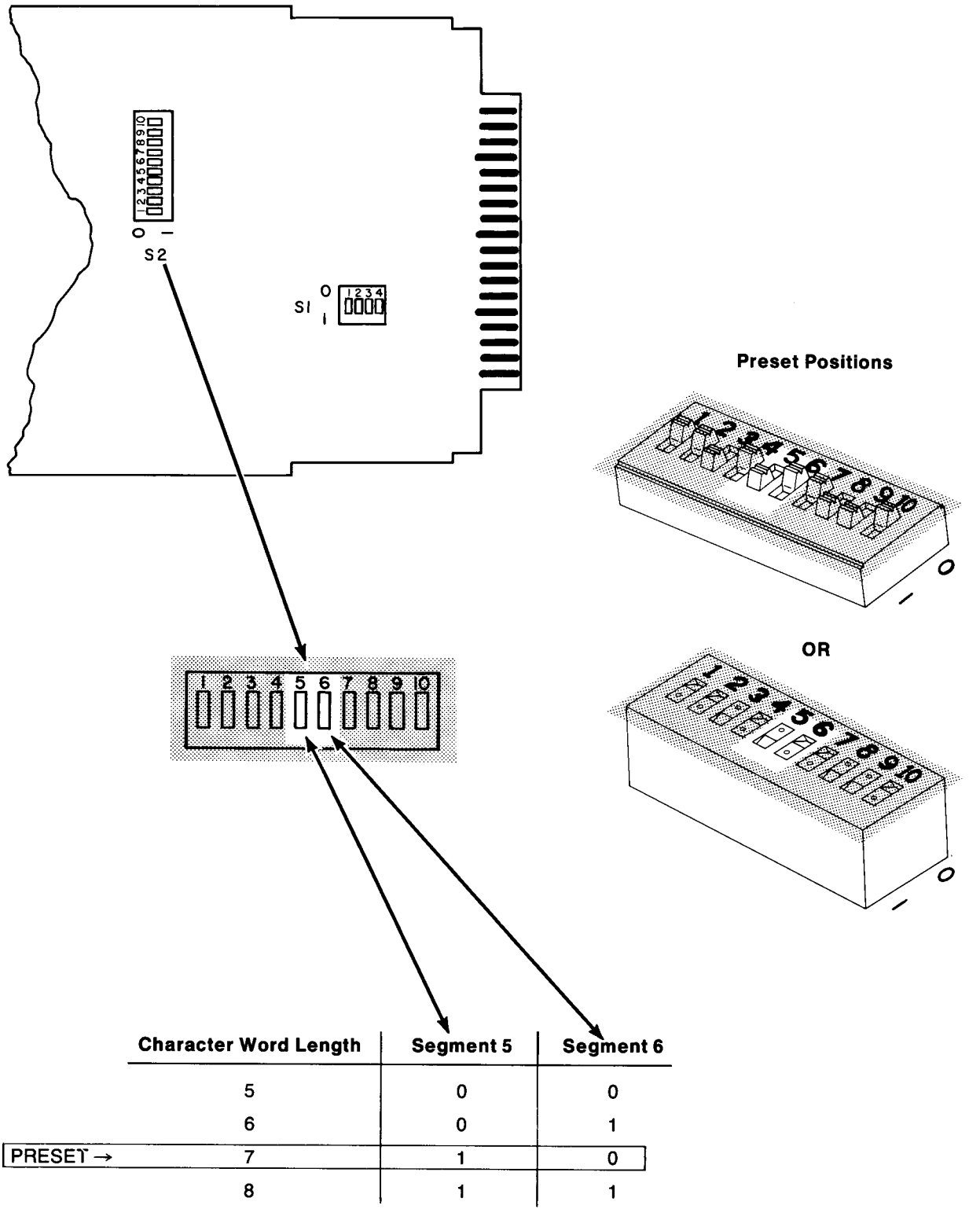
Parity Transmit	Segment 1
PRESET → No	0
Yes	1

Select Parity	Segment 2
PRESET → Odd	0
Even	1

Parity Enable	Segment 3
Disable	0
PRESET → Enable	1

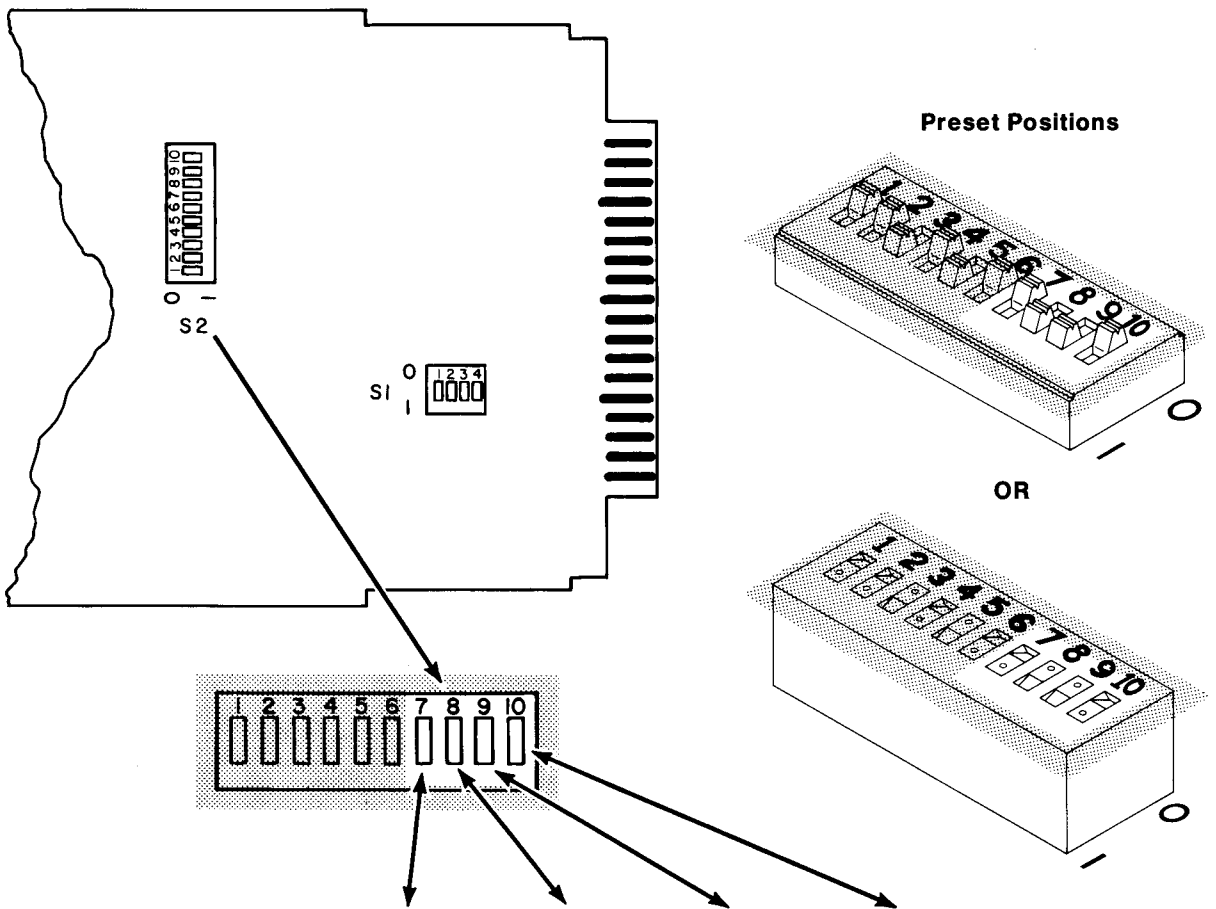
Number of Stop Bits	Segment 4
PRESET → 1	0
2	1

Figure 2-3. Parity and Stop Bit Switches



Character Word Length	Segment 5	Segment 6
5	0	0
6	0	1
PRESET → 7	1	0
8	1	1

Figure 2-4. Character Word Length Switches



Baud Rate	Segment 7	Segment 8	Segment 9	Segment 10
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
200	0	1	0	1
PRESET → 300	0	1	1	0
600	0	1	1	1
1,200	1	0	0	0
1,800	1	0	0	1
2,000	1	0	1	0
2,400	1	0	1	1
3,600	1	1	0	0
4,800	1	1	0	1
7,200	1	1	1	0
9,600	1	1	1	1

Figure 2-5. Baud Rate Switches

Connecting to the HP-85

CAUTION

Before connecting this interface (or any other interface), make sure the HP-85 is turned OFF. Installing with power on can damage both the interface and the mainframe. In addition, the mainframe goes through an initialization routine at power-on which checks for presence of the interface, and does not recognize the interface if installed after the initialization routine.

When connecting the 82939 interface to an HP-85, follow this procedure.

1. Set the select code switches. The select code is set to 10 at the factory.
2. Set the default condition switches.
3. Insert the interface end of the cable into any of the four I/O slots in the back of the mainframe (see Figure 2-6). Make sure the interface is firmly seated in the slot.
4. Connect the other end of the interface cable to an applicable data communications device.

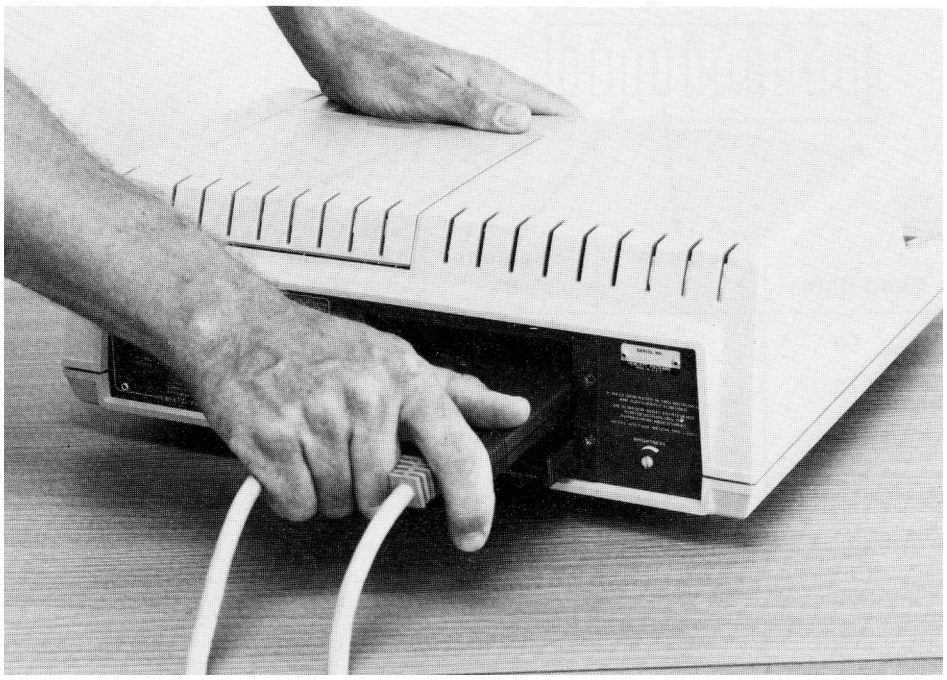
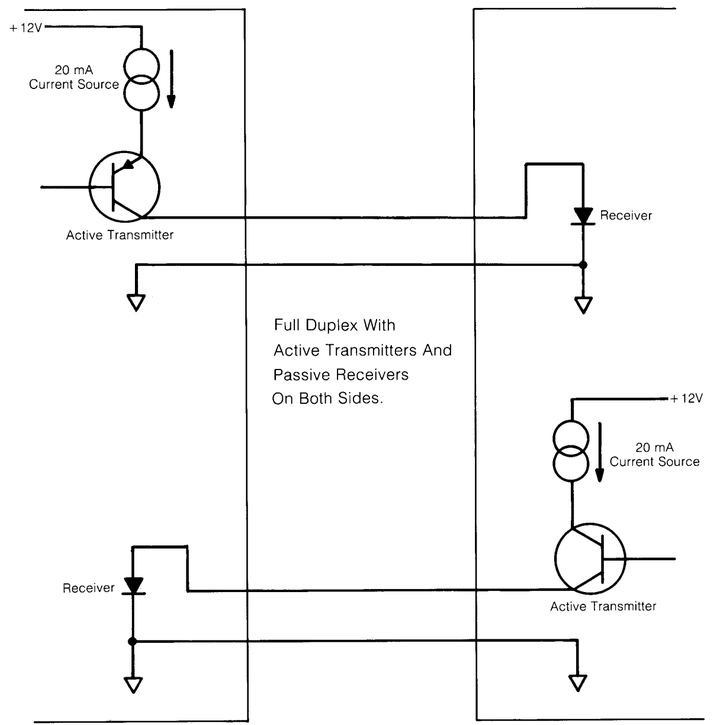


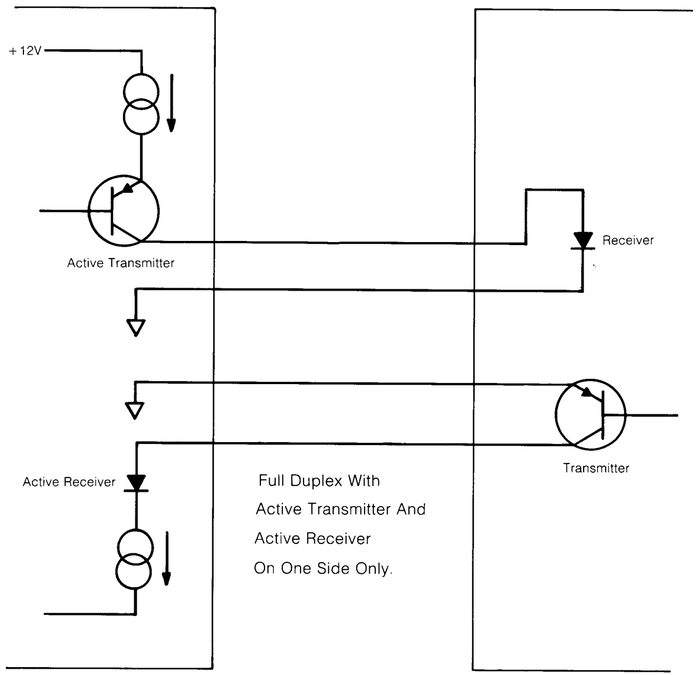
Figure 2-6. Installing the Interface Into the HP-85 Backplane

20 mA Current Loop

RS-232C supplies are ±12V. This gives a ±10V drive capability.

Each of the 20 mA current supplies can supply 20 mA at up to a 9.9V compliance (−20 mA into a 495 ohm load). The floating detector uses about 1.9V, and the floating switch uses about .2V. Thus, in full-duplex mode connected to a teletype, there is 9.7V compliance left to the teletype receiver/detector and 8V compliance left to the teletype transmitter/switch.





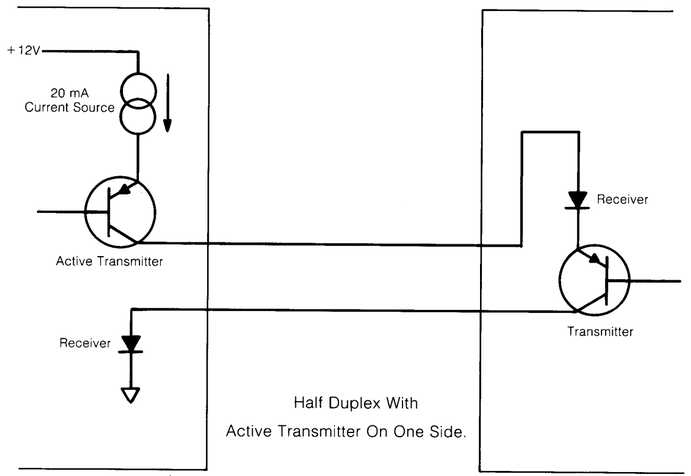


Figure 2-7. Recommended Current Loop Circuits

60 mA Current Loop

The passive switch and detector elements are capable of handling 60 mA current loop if the 20 mA current supplies are not used. 15 volts is the maximum off voltage allowed across the switch element.

20 mA Current Supplies

Q1 is a current sink, and Q2 is a current source. R1 and R2 form a voltage divider and apply a constant voltage to the base of Q1. Q1 places a constant 2V across R3. Since R3 is 100 ohms, a constant 20 mA flows through it. D1 provides temperature compensation for Q1. The current source circuit operates in an analogous manner. 1% resistors are used to limit the total variation of current to ±10% under all conditions.

Current Detector

A 6N138 opto-isolator (U7) is used as a current detector. The 150-ohm resistor shunting the input diode prevents the opto-isolator from turning on until at least 11 mA is flowing. Above 13 mA, R11 causes Q4 to conduct and draw the remaining current. The 0.1 μF capacitor between pins 5 and 8 prevents oscillations on the output of the opto-isolator.

Current Switch

A 6N136 opto-isolator (U9) is used as a current switch. When U9 is turned on, it turns Q3 off.

Functional Test

The following program listing may be entered and run to functionally test the interface. In most instances, running this test will indicate whether or not the interface is operational.

Use the following steps to enter and run the test from the HP-85 keyboard:

1. Make sure the interface and I/O ROM are installed. If necessary, refer to page 20 and install the interface and I/O ROM.
2. Peripherals may or may not be connected to the interface.
3. Turn the HP-85 power switch to the ON position.
4. Press the [SHIFT] key and, while this key is depressed, press the [AUTO I] key. This will cause the program lines to be numbered by ten in ascending order (10, 20, 30, etc.). Then press [END LINE].
5. Refer to the following program listing and enter the line by pressing these keys:

   [C] [L] [E] [A] [R] then press [END LINE]

   Continue this procedure until the entire program is entered, making sure to press [END LINE] as each numbered program line is entered.

```
 10 CLEAR
 20 DISP "82939A EXERCISER","ENT
    ER SELECT CODE..." @ PRINT "
    82939A EXERCISER"
 30 INPUT S
 40 DISP "ENTER # OF TIMES TO RU
    N TEST..."
 50 INPUT N
 60 RESET S
 70 GOSUB 150
 80 GOSUB 400
 90 GOSUB 460
100 GOSUB 680
110 N=N-1
120 IF N>0 THEN GOTO 60
130 DISP "TEST COMPLETE" @ PRINT
     "TEST COMPLETE"
140 END
150 DISP "TRANSLATOR AND PROCESS
    OR TEST"
160 N1=0 @ A4=0
170 WIO S,0;2
180 WIO S,1;113
190 WIO S,0;0
200 A5=1
210 IF RIO(S,0)=35 THEN 240
220 N1=N1+1 @ IF N1>2 THEN GOSUB
     730
230 GOTO 210
240 A5=0
250 A1=RIO(S,1)
260 IF A1#113 THEN GOSUB 880
270 FOR A2=0 TO 255
280 WIO S,1;A2
290 IF RIO(S,0)=35 THEN 360
300 N1=N1+1 @ IF N1>2 THEN GOSUB
     730
310 IF N1<=2 THEN 290
320 PRINT "CONTINUING WITH NEXT
    TEST"
330 A2=255
340 A3=RIO(S,1)
350 GOTO 380
360 A3=RIO(S,1)
370 IF A3#A2 THEN GOSUB 790
380 NEXT A2
390 RETURN
400 C=0
410 DISP "PORT 1 TEST"
420 B1=116
430 B3=10
440 GOSUB 530
450 RETURN
460 C=1
470 DISP "PORT 2 TEST"
480 B4=0
490 B1=117
500 B3=246
510 GOSUB 530
520 RETURN
530 WIO S,0;2
540 WIO S,1;B1
550 IF RIO(S,0)<128 THEN 590
560 N1=N1+1 @ IF N1>4 THEN GOSUB
     730
570 IF N1>4 THEN 590
580 GOTO 550
590 WIO S,0;0
600 IF RIO(S,0)=35 THEN 640
610 N1=N1+1 @ IF N1>4 THEN GOSUB
     730
620 IF N1>4 THEN 640
630 GOTO 600
640 B2=RIO(S,1)
650 IF RIO(S,0)#32 THEN GOSUB 90
    0
660 IF B2#B3 THEN GOSUB 920
670 RETURN
680 DISP "STATUS TEST"
690 STATUS S,0 ; D0,D1,D2,D3,D4,
    D5,D6,D7,D8,D9,C1,C2
700 IF D0#2 OR D1#0 OR D2#0 OR D
    3#0 OR D8#0 OR D9#137 OR C1#
    32 OR C2#0 THEN GOSUB 1120
710 IF D4#10 OR D5#0 OR D6#1 OR
    D7#128 THEN GOSUB 1150
720 RETURN
730 PRINT "HANDSHAKE FAILURE OR
    INTERFACE  NOT LOGGED IN"
740 IF A5=0 THEN RETURN
750 PRINT "CHECK THAT SWITCHES A
    RE SET TO  SELECT CODE";S
760 PRINT "NON RECOVERABLE ERROR
    -TEST ABORT" @ BEEP
770 RESET S
780 GOTO 110
790 PRINT "OUTPUT";A2;"TO OB  RE
    CEIVED";A3
800 A4=A4+1
810 IF A4>10 THEN 830
820 RETURN
830 PRINT "GREATER THAN 10 ERROR
    S";"CONTINUING WITH NEXT TES
    T"
840 A2=255
850 RETURN
860 PRINT "HANDSHAKE FAILURE-PRO
    BABLE";"PROCESSOR OR TRANSLA
    TOR FAILURE"
870 RETURN
880 PRINT "RECEIVED INCORRECT LO
    OPBACK";"RESPONSE-PROBABLE T
    RANSLATOR";"FAILURE"
890 RETURN
900 PRINT "HANDSHAKE FAILURE-PSR
     NOT";"CLEARED AFTER HANDSHA
    KE"
910 RETURN
920 IF C=1 THEN GOTO 1010
930 IF B2>127 THEN PRINT "PROCES
    SOR READS 8250 MR LINE";"PUL
    LED   PROCESSOR OR 8250 ERRO
    R"
940 IF BIT(B2,6) THEN PRINT "S1-
    1 OPEN"
950 B2=BINAND(B2,63)
960 IF B2=10 THEN GOTO 1000
970 PRINT "SWITCHES DID NOT READ
     AS FACTORY SETTINGS"
980 A$=DTB$(B2)
990 PRINT "S2-1 TO S2-6 READ AS
    "&A$[11,16]
1000 RETURN
1010 IF BIT(B2,6) THEN GOTO 1030
```

```
1020 PRINT "P26 READ LOW EXPECTE
     D HIGH"
1030 IF NOT BIT(B2,7) THEN PRINT
      "RLSD LINE READ IN WRONG S
     TATE"
1040 IF NOT BIT(B2,5) THEN PRINT
      "DSR LINE READ IN WRONG ST
     ATE"
1050 IF NOT BIT(B2,4) THEN PRINT
      "CTS LINE READ IN WRONG ST
     ATE"
1060 B2=BINAND(B2,15)
1070 IF b2=6 THEN GOTO 1110
1080 PRINT "SWITCHES DID NOT REA
     D AS FACTORY SETTINGS"
1090 B$=DTB$(B2)
1100 PRINT "S2-7 TO S2-10 READ A
     S "&B$[13,16]
1110 RETURN
1120 PRINT "STATUS ERROR-STATUS
     BYTE NOT AT RESET DEFAULT"
1130 PRINT "STATUS BYTES=";D0;D1
     ;D2;D3;D4;D5;D6;D7;D8;D9;C1
     ;C2
1140 RETURN
1150 IF D4=10 THEN GOTO 1200
1160 IF BIT(D4,6) THEN PRINT "BR
     EAK ERROR"
1170 IF NOT BIT(D4,6) THEN PRINT
      "STATUS READS";
1180 B2=BINAND(D4,63)
1190 GOSUB 950
1200 IF D5=0 THEN GOTO 1240
1210 IF BIT(D5,4) OR BIT(D5,5) T
     HEN PRINT "STATUS READS AUT
     OHANDSHAKE";"SWITCH OPEN"
1220 IF BIT(D5,4) OR BIT(D5,5) T
     HEN CONTROL S,5 ; 0
1230 IF NOT BIT(D5,4) OR NOT BIT
     (D5,5) THEN PRINT "STATUS E
     RROR IN BYTE 5  RCVD";D5;"E
     XPECTED 0"
1240 IF D6=1 THEN GOTO 1270
1250 PRINT "STATUS READS BAUD RA
     TE SWITCHES NOT AT FACTORY
     SETTINGS"
1260 PRINT "STATUS BYTE 6 READS"
     ;D6;"FACTORY SETTING=1"
1270 IF D7=128 THEN RETURN
1280 PRINT "STATUS READS BAUD RA
     TE SWITCHES NOT AT FACTORY
     SETTINGS"
1290 PRINT "STATUS BYTE 7 READS"
     ;D7;"FACTORY SETTING=128"
1300 RETURN
```

6. After the program is entered press (RUN). The printer should print:

```
82939A EXERCISER
```

   The screen should display:

```
82939A EXERCISER
ENTER SELECT CODE
?
```

7. Respond by entering the select code the interface is set to. For example, if select code 7 is set, press (7) and then (END LINE). If the wrong select code is entered, one or more error messages will appear on the screen after step 8 is performed. If this happens, press (RUN) and enter the select code again.

8. The screen should then display:

```
ENTER # OF TIMES TO RUN TEST
?
```

9. Enter the number of times you wish to run the short test. To run the test once, press (1) and then (END LINE); to run the test ten times, press (1) (0) and then (END LINE), etc. Running the test several times may be useful if you suspect an intermittent failure.

10. The screen should then display:

```
TRANSLATOR AND PROCESSOR TEST
```

    If this test passes, shortly thereafter the screen will display:

```
PORT 1 TEST
```

    The test names are displayed on the screen the number of times you have specified for the test to run unless there is a failure. If a test fails, an error message is printed for that test.

Re-Configuring the Cable

CAUTION

If it is necessary to re-configure the cable, please proceed with extreme caution. Improper configuration of the cable can result in seriously impaired operation or in permanent damage to the interface, the mainframe and the peripheral or terminal to which they are connected.

Individual modems may have features that are not compatible with the interface cable furnished with the 82939. These features may require re-configuring of the interface cable before connecting it to the modem. This is accomplished by re-wiring the 28-pin connector inside the interface housing.

Re-wiring the 28-Pin Connector

Re-wiring is accomplished by removing a pin from one position in the connector and replacing it in another position. Refer to the interface schematic diagram (Figure 3-4) for pin assignments.

The pin which is crimped onto each wire is held in place in the connector body by a locking tab (see Figure 2-8). Holes on the side of the connector provide access to the locking tabs.

To remove a wire, insert the end of a paper clip in the hole by the appropriate pin. Press in to release the locking tab, then pull the wire and its pin from the connector body.

To install a wire, insert it in the desired pin position with the locking tab to the outside edge of the connector. Once installed, pull gently on the wire to ensure that the locking tab is locking the pin in place.

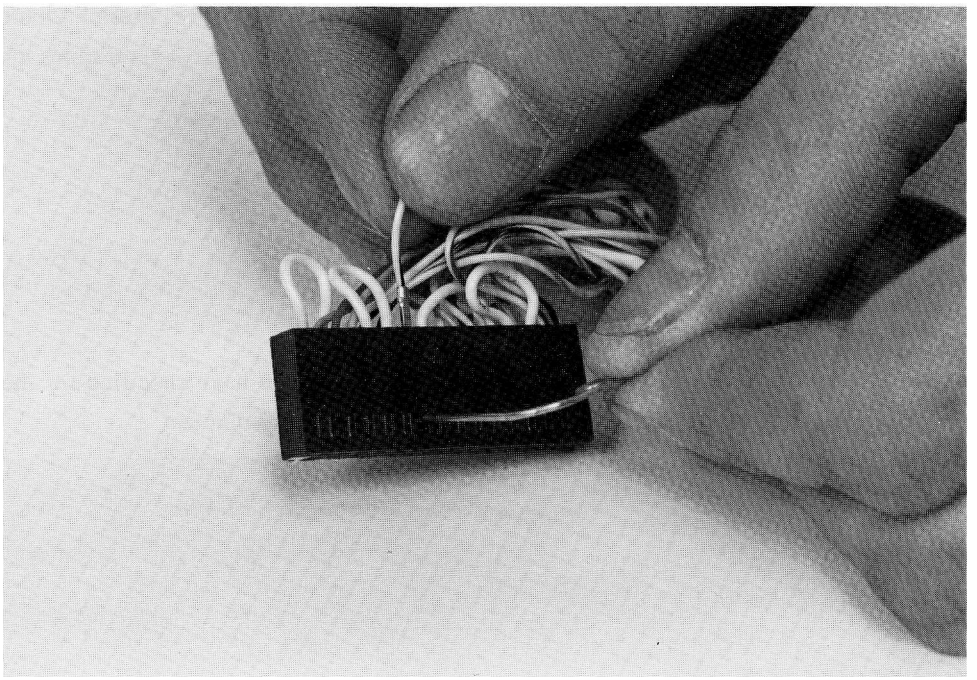
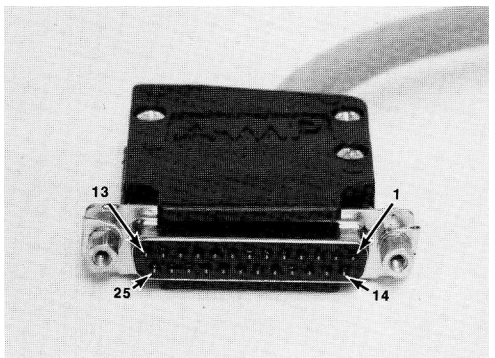
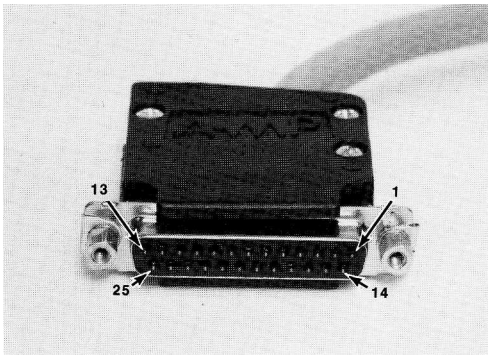


Figure 2-8. Removing a Wire From the Interface Connector

Table 2-2. RS-232 Connector Pin Assignments



Standard Cable Connector



Option 001 Cable Connector

Pin No.	Wire Color	Signal Name
1	Shield	Protective Ground
2	Red	Transmitted Data
3	Orange	Received Data
4	Yellow	Request to Send
5	Green	Clear to Send
6	Blue	Data Set Ready
7	Violet	Signal Ground
8	Gray	Received Line Signal Detector
12	Black/White	Unassigned
19	Brown/White	Unassigned
20	Black	Data Terminal Ready
23	Brown	Data Rate Select

Section 3

Theory of Operation

Introduction

This section describes the theory of operation of the 82939 hardware. Most of the interface functions are performed by a ROM program internal to a microcomputer. Therefore, the interface is almost entirely a software device. Refer to the operation and programming manual for the software theory of operation.

The 82939 consists of three major components: the translator, the microcomputer and the UART. The translator functions as an interface between the mainframe's internal bus structure and the 82939's internal bus structure; the UART converts parallel data to serial, and vice versa, for communication with the remote device; and the microcomputer controls and synchronizes the operation of both, on instructions from the mainframe and from its own internal ROM program.

The operation of these three components will be examined in greater detail, then data will be followed as it passes through the receiving and transmitting circuits to see how each component handles it.

Refer to the block diagrams as you read these discussions.

Translator Function

The translator functions as an interface, or translator, between the HP-85's internal bus structure and the 82939's internal bus structure. It contains two registers which can be written by the HP-85 CPU and read by the 82939 microcomputer (one for data and one for status), and two which can be written by the 82939 microcomputer and read by the HP-85 CPU (again one for data and one for status). It also contains control circuitry for manipulating these registers to produce the desired results. Figure 3-1 is a block diagram of the translator. All four registers are eight bits wide.

These registers can be described as follows:

Output Buffer (OB)

The output buffer is used by the HP-85 CPU to send data to the interface microcomputer. It is written by the CPU and read by the microcomputer. When the CPU writes to the OB, it sets the Output Buffer Full (OBF) flag. The microcomputer clears the OBF flag when it reads the OB.

Input Buffer (IB)

The input buffer is identical to the OB except that the data flows in the opposite direction. It is written by the microcomputer and read by the CPU. The microcomputer sets the Input Buffer Full (IBF) flag when it writes to the IB, and the CPU clears the IBF flag when it reads the IB.

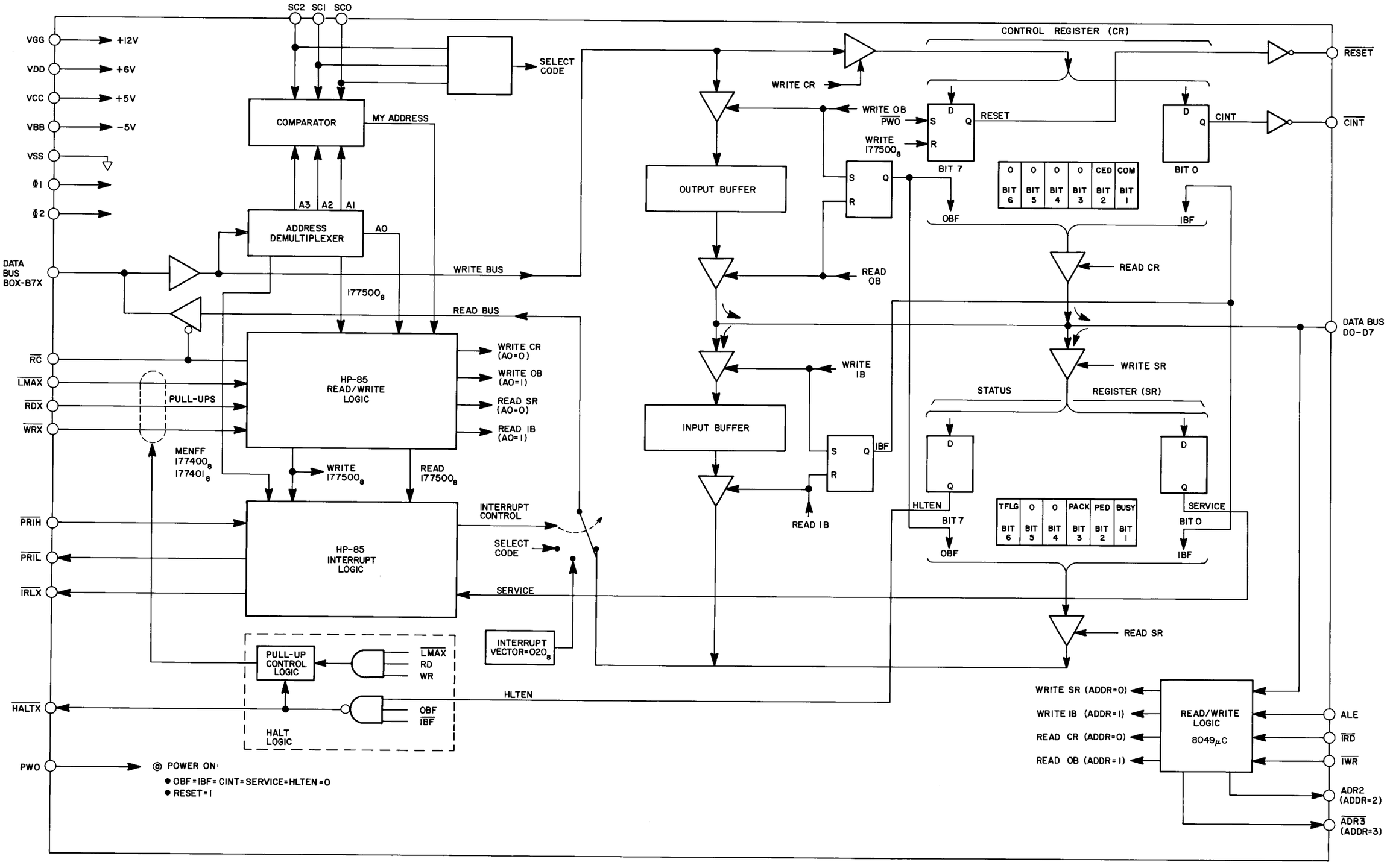


Figure 3-1. Translator Block Diagram

Control Register (CR)

The control register is used to send control information from the CPU to the microcomputer. The middle six bits (bits 1 to 6) are similar to the OB in that they are written by the CPU and read by the microcomputer. Bits 0 and 7 are two-function bits. When the CPU writes the CR, the middle six bits go straight through to be read by the microcomputer, but the outer two are diverted. Bit 0 becomes the INT signal, which is used to interrupt the microcomputer. Bit 7 becomes RESET, which is used to re-set the microprocessor. When the microcomputer reads the CR, it reads the IBF flag as bit 0 and the OBF flag as bit 7.

Status Register (SR)

The status register is similar to the CR except that status information is sent from the microcomputer to the CPU. The middle six bits are written by the microcomputer and read by the CPU. Bits 0 and 7 are two-function bits. When written by the microcomputer, bit 0 becomes SERVICE, which is used to interrupt the CPU. Bit 7 becomes HLTEN, which is used to halt the CPU. When the CPU reads the SR, it reads the IBF flag as bit 0 and the OBF flag as bit 7.

These four registers all share the same bus lines; that is, there is only one 8-bit bus connecting the HP-85 internal bus lines and the microcomputer. Control and status information and data all flow along this bus and are directed to the proper register by address logic, which will be described next.

When the mainframe wishes to communicate with a peripheral, it sends out a 4-bit code, A0 to A3. A0 determines whether control or status information or data will be transferred (A0 = 0 means control or status information, A0 = 1 means data), and A1 to A3 are the device address. A comparator circuit compares A1 to A3 with SC0 to SC2 (the select code set by the user) and if they are the same, it informs the HP-85 read/write logic via the My Address line. At the same time, the mainframe sends out a read or write instruction via the RD or WR line. These two pieces of information (A0 to A3 and RD or WR) completely determine which register is being implemented.

For example, if the mainframe sends out an address of 1101 and pulls the RD line, the following events will occur:

- 110 (A1, A2 and A3) will be sent to the comparator to be compared with SC0, SC1 and SC2. If they match, an enabling signal will be sent to the read/write logic via the My Address line.
- A0 will be sent to the read/write logic. Since it is a 1, either the output buffer will be written or the input buffer will be read.

The signal on RD tells the read/write logic that a read will occur. This narrows the choice down to reading the input buffer. The read/write logic will then activate the Read IB line, and the contents of the input buffer will be placed on the read bus and then on the data bus for transfer to the mainframe data bus.

The procedure used by the interface microcomputer is similar, except there is no My Address line (it is not needed, since the microcomputer can only address its own interface). An 8-bit code is sent out with the LSB determining whether data or status information will be transferred (LSB = 0 means status, LSB = 1 means data). The microcomputer also sends out a read or write instruction via the RD or WR lines.

The translator also contains logic for dealing with interrupts and halts.

The translator contains a number of latches, two of which, the Output Buffer Full flag and the Input Buffer Full flag, are of sufficient complexity and importance to require further explanation. When the CPU writes the output buffer, it sets the OBF flag, along with bit 7 of the CR and SR. When the microcomputer reads the OB, it re-sets the OBF flag, along with bit 7 of the CR and SR. The IBF flag operates in a similar manner (see Figure 3-1).

The translator operates on supply voltages of +5V, +6V and +12V, all of which it receives from the mainframe.

Microcomputer Function

The controlling entity of the 82939 interface is an 8049 single-chip microcomputer. A major portion of this microcomputer is a ROM which contains a microcode which determines the entire behavior of the interface. This microcode is not changeable by the user, however, many variables can be changed, either by switches (see Section 2) or by software (see operation and programming manual). The microcomputer also contains a 5.5296 MHz clock for internal timing, which is divided by three and passed to the UART for internal timing. The microcomputer has one 8-bit-wide data port which functions for both input and output.

Internal to the microcomputer are 12, 8-bit status registers and 22, 8-bit control registers. The status registers contain information indicating the current state of the microcomputer. Table 3-1 shows the location of this information. The control registers are written to whenever a change in the microcomputer state is desired. Table 3-2 lists the functions of the control registers.

UART Function

The UART is the device which does the actual serial-to-parallel conversion. Under control of the microcomputer, it converts incoming serial data streams into parallel data for transmission to the mainframe. It also converts parallel data into serial data streams suitable for RS-232C transmission.

The UART can be programmed by the microcomputer to cause an interrupt on various conditions.

Data Flow Through the 82939 Interface

Having looked at the operation of the major components of the interface, we will now trace the path which data takes as it passes through the interface. Refer to Figure 3-2 while reading this description.

Control Register Number	Bit Number 7	6	5	4	3	2	1	0	Default Value (Decimal)	Register Function
CR12	Input termination character								0	Input termination character #1
CR13	Input termination character								0	Input termination character #2
CR14	Input termination character								0	Input termination character #3
CR15	Input termination character								0	Input termination character #4
CR16	Auto-RTS enable	EOL transmit disable	Six bit EOL character count						2	Output EOL sequence
CR17	EOL character								13 (CR)	EOL character #1
CR18	EOL character								10 (LF)	EOL character #2
CR19	EOL character								0	EOL character #3
CR20	EOL character								0	EOL character #4
CR21	EOL character								0	EOL character #5
CR22	EOL character								0	EOL character #6
CR23	EOL character								0	EOL character #7

Table 3-2. Control Register Contents

Control Register Number	Bit Number 7	6	5	4	3	2	1	0	Default Value (Decimal)	Register Function
CR1	Break received	Framing error	Parity error	Receive data available	DCD (RTS)	Auto-disconnect	DSR (DRS)	CTS (DTR)	0	Interrupt mask
CR2	—	—	—	—	—	DRS (DSR)	RTS (DCD)	DTR (CTS)	0	Modem control lines
CR3					Baud rate number				Variable	Baud rate select
CR4	—	Set break	Force parity	Odd/even parity	Enable parity	Stop bits	Character length		Variable	Line characteristics
CR5	—	—	Receive handshake	Transmit handshake	DCD (RTS)	—	DSR (DRS)	CTS (DTR)	Variable	Modem features
CR6	Most significant byte								Variable	Baud rate
CR7	Least significant byte								Variable	divisor latches
CR8	Parity/framing error replacement character								0	Error replacement character
CR9	Enable transmitter	Strip received rubouts	Strip received nulls	Change char if error	Set bit 7 of char if error	Reset receive queue	Auto-echo enable	Enable receiver	137 (10001001)	Transmitter/ receiver control
CR11	Transmit ON	Transmit OFF	—	Terminate if CR15	Terminate if CR14	Terminate if CR13	Terminate if CR12	—	0	Input data control

Table 3-1. Status Register Contents

Status Register Number	Bit Number 7	6	5	4	3	2	1	0	Default Value (Decimal)	Register Function
SR0	0	0	0	0	0	0	1	0	2	Interface identification
SR1	Break received	Framing error	Parity error	Receive data available	DCD (RTS)	Auto-disconnect	DSR (DRS)	CTS (DTR)	0	Interrupt cause
SR2	—	—	—	—	—	DRS (DSR)	RTS (DCD)	DTR (CTS)	0	Modem control lines
SR3	—	—	—	—	DCD (RTS)	Cable type	DSR (DRS)	CTS (DTR)	Variable	Modem status lines
SR4		Set break	Force parity	Odd/even parity	Enable parity	Stop bits	Character length		Variable	Line characteristics
SR5	—	—	Receive handshake	Transmit handshake	DCD (RTS)	—	DSR (DRS)	CTS (DTR)	Variable	Modem features
SR6	Most significant byte								Variable	Baud rate
SR7	Least significant byte								Variable	divisor latches
SR8		Parity/framing error replacement character							0	Error replacement character
SR9	Enable transmitter	Strip received rubouts	Strip received nulls	Change char if error	Set bit 7 of char if error	Reset receive queue	Auto-echo enable	Enable receiver	137 (10001001)	Transmitter/ receiver control
SR10	—	—	Transmit register empty	Break received	Framing error	Parity error	—	Received data available	0	Line status
SR11	End of output data list	End of input data list	Transfer count expired	CR15 character received	CR14 character received	CR13 character received	CR12 character received	DELIM character received	0	I/O Termination cause

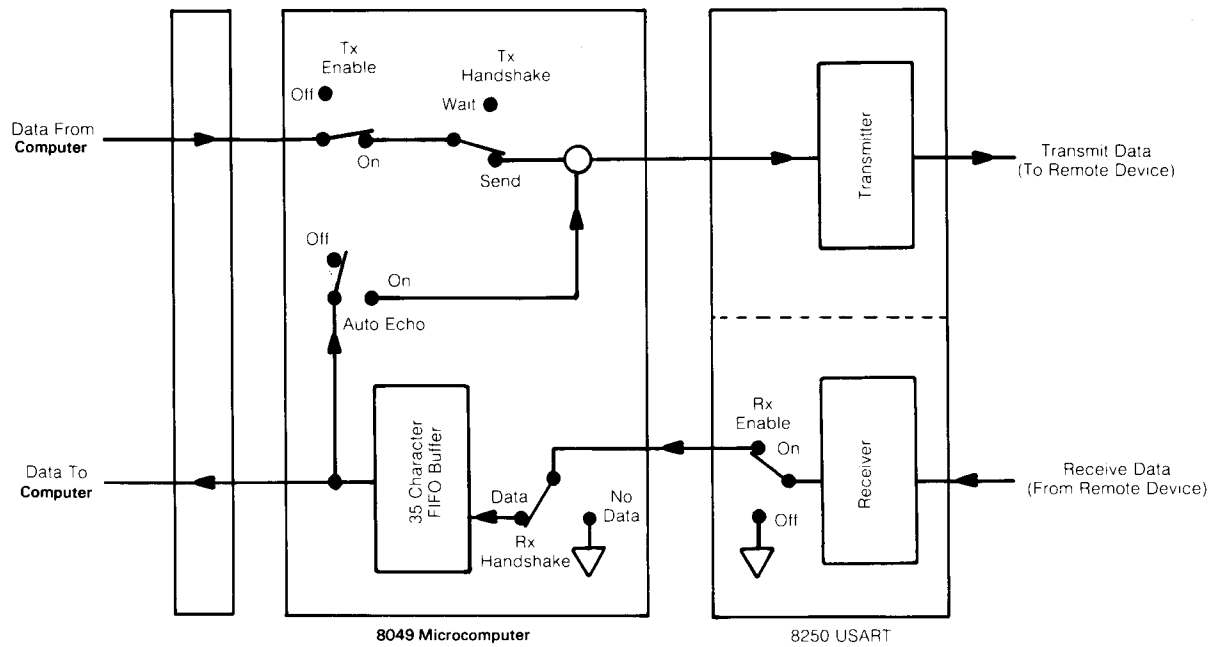


Figure 3-2. Data Flow Diagram

As data is received from a remote device, the receiver checks it for errors and converts it to parallel form. If the user has enabled the receiver via the receiver control register (control register 9, bit 0), the UART will interrupt the microcomputer to indicate that it has a data byte ready. If the user has not enabled the receiver, the data byte will be discarded.

When interrupted for received data, the microcomputer checks the receive autohandshake bit (control and status register 5, bit 5) and the data carrier detect (modem status register 3, bit 0) modem status line to determine if the received data is valid. If the user has specified the receive handshake feature and DCD is "OFF", the received data will be discarded. Otherwise, the data will be pushed into the queue buffer. If the data was received with a parity or framing error, this information will also be pushed into the queue buffer.

A received BREAK follows essentially the same path as received data. If a BREAK is received, an indicator will be pushed into the queue buffer if the receiver is enabled and the autohandshake criteria are met.

All received data and status are passed through the queue buffer, as described here, to keep correct time sequence.

Note: Data and status will be saved in the buffer whether or not there is an input data statement active in the HP-85.

The background idle loop in the interface microcomputer pulls data and status information from the queue buffer and takes appropriate action. This idle loop handles auto echo, data transfer, status and interrupts. If the auto echo feature is enabled, the receive data is sent back to the UART for re-transmission. Since data will not be sent to the HP-85 mainframe until it has been re-transmitted, the auto echo feature may affect performance.

Received data is input to the HP-85 from the queue buffer using either the ENTER or TRANSFER I/O statements. The termination conditions, such as count and character match, are checked as the data is transferred to the mainframe.

Receive status information, such as BREAK or data errors, can be read via the line status register (#10) and, depending on the state of the interrupt mask (control register 1), may cause a user interrupt.

Due to the nature of the queue buffer, if a data byte is in the queue, status information which follows it will not be seen until this data has been sent to the mainframe. For example, if an input is not active, a BREAK will not be reported if a data byte was received before the BREAK. (The idle loop will not look ahead beyond the received character to perceive the BREAK.)

This is the procedure which the 82939 interface uses for receiving data. The data transmit path will be presented next.

When the UART transmit buffer is empty, the microcomputer checks the transmit autohandshake bit (control register 5, bit 4) and the Clear to Send signal (modem status register 3, bit 0) to determine if the remote device is ready to accept data. If the user has enabled the transmit autohandshake feature and CTS is "OFF", no data will be sent. Otherwise, the microcomputer will look for data to transmit. Characters to be echoed get the highest priority for transmission. If auto echo is enabled, the queue buffer will be scanned for echo data to be sent to the UART transmitter. If there is no echo data, data from the HP-85 mainframe will be sent if there is an OUTPUT or TRANSFER statement active.

BASIC Statements

The 82939 interface is controlled by means of a command set derived from BASIC, which is sent to it via the HP-85 mainframe. Table 3-3 lists the statements which interact with the interface, along with the function of each statement.

Table 3-3. Summary of Basic Statements

Statement	Function
ABORT IO (isc)	Abort TRANSFERs in progress and drop all modem lines.
ASSERT (isc); (exp)	Interrupting write to modem control register. (Immediate – does not wait for Tx character.)
CONTROL (isc), XX*; (list)	See CONTROL summary (Table 3-2).
ENABLE INTR (isc); (exp)	Enable interrupts with (exp) as mask.
ENTER (isc); (list) (isc) USING (string); (list) (isc) USING (line#); (list)	Read Rx characters in default format. Read Rx characters in (string) format. Read Rx characters with format of (line#).
HALT (isc)	Abort TRANSFERs in progress and leave modem lines unchanged.
OUTPUT (isc); (list) (isc) USING (string); (list) (isc) USING (line#); (list)	Transmit data in default format. Transmit data with (string) format. Transmit data with format of (line#).
REQUEST (isc); (exp)	Sends a BREAK of (exp) character-time duration ((exp) character-time spacing line followed by a 5 character-time marking idle line).
RESET (isc)	RESET card: disconnect modem, run self-test, initialize card to defaults.
RESUME (isc)	Enable transmitter.
SEND (isc); DATA (list) [END]	Output data as bytes. Execute EOL sequence after data.
STATUS (isc), XX*; (list)	See STATUS summary (Table 3-1).
TRANSFER (isc) TO (buffer) (buffer) TO (isc) INTR [COUNT (exp)] [DELIM (exp)]	Read receive data into buffer. Send transmit data from buffer. Interrupt transfers. Byte count to terminate input transfer. Input termination character.

* XX represents the register number.

Error Messages

The 82939 generates error messages when operation of the card violates certain conditions. Table 3-4 contains a list of these error messages.

Table 3-4. Summary of Error Messages

System Errors (common to all I/O cards)

Error Number	Error
110	Hardware self-test failed (RAM, ROM, ALU, UART)
111	Illegal operation

Card Dependent Errors (unique to RS-232 card)

Error Number	Error
113*	UART receiver overrun – data lost
114*	Rx queue buffer overrun – data lost
115*	Automatic disconnect forced

* Aborts TRANSFERs in progress.

HP-85 I/O Backplane Lines

The I/O lines in Table 3-5 appear at each of the four I/O slots on the HP-85. They connect to the interface when it is inserted into any of the slots. Figure 3-3 shows how the I/O slot connector pins are numbered. Each I/O slot is numbered in the same manner.

Table 3-5. HP/85 I/O Backplane Lines

Line	Pin No.	Meaning	Direction HP-85	Direction Interface
Φ21	1	Non-Overlapping Clock (+12V) (not used)		→
Φ2	2	Non-Overlapping Clock (+12V)		→
Φ1	3	Non-Overlapping Clock (+12V)		→
Φ12	4	Non-Overlapping Clock (+12V) (not used)		→
V_{GG}	5	+12V		→
$\overline{\text{LMAX}}$	6	Load Memory Address		→
$\overline{\text{IRLX}}$	7	Interrupt Request		←
$\overline{\text{RDX}}$	8	Read		→
$\overline{\text{RC}}$	9	Read Control		←
$\overline{\text{WRX}}$	10	Write		→
V_{CC}	11	+5V		→
B4X	12	I/O Line	↔	↔
B5X	13	I/O Line	↔	↔
B6X	14	I/O Line	↔	↔
B7X	15	I/O Line	↔	↔
—	16	Open		
$\overline{\text{PRIH}}$	17	Priority High		→
DIS	18	Disable. +6V Signal Voltage. This is used to keep $\overline{\text{PRIH}}$ and $\overline{\text{PRIL}}$ from shorting together when an interface is plugged into an I/O slot.		
SPKR	$\overline{1}$	Speaker Output (not used)		→
—	$\overline{2}$	Open		
—	$\overline{3}$	Open		
L. GND	$\overline{4}$	Logic Ground		→
L. GND	$\overline{5}$	Logic Ground		→
L. GND	$\overline{6}$	Logic Ground		→
$\overline{\text{HALTX}}$	$\overline{7}$	Halt		←
V_{BB}	$\overline{8}$	−5V		→
—	$\overline{9}$	−12V (not used)		→
PWO	$\overline{10}$	Power On		→
V_{CC}	$\overline{11}$	+5V		→
B0X	$\overline{12}$	I/O Line	↔	↔
B1X	$\overline{13}$	I/O Line	↔	↔
B2X	$\overline{14}$	I/O Line	↔	↔
B3X	$\overline{15}$	I/O Line	↔	↔
V_{DD}	$\overline{16}$	+6V		→
—	$\overline{17}$	Open		
$\overline{\text{PRIL}}$	$\overline{18}$	Priority Low		←

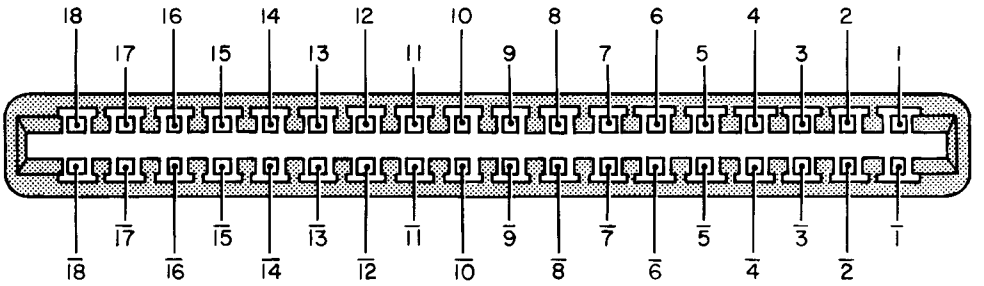


Figure 3-3. HP-85 I/O Slot Connector Pinout

Table 3-6. Replaceable Parts List

Reference Designator	CD	hp Part No.	TQ	Description
A1	8	82939-60901	1	PC Assembly
	9	82939-60902	1	Case, Complete, Standard
	0	82939-60903	1	Case, Complete, Option 1
	1	82939-60904	1	Case, Complete, Option 2
	0	8120-3248	1	Cable Assembly, Standard
	1	8120-3247	1	Cable Assembly, Option 1
	2	8120-3191	1	Cable Assembly, Option 2
C1	6	0180-0228	2	C-F: 22μF, 15V
C2	5	0160-0576	10	C-F: .1μF, 50V
C3	6	0180-0228	—	C-F: 22μF, 15V
C4 – C6	5	0160-0576	—	C-F: .1μF, 50V
C7 – C8	1	0180-0116	2	C-F: 6.8μF, 35V
C9	4	0160-4767	1	C-F: 20pF, 200V
C10 – C15	5	0160-0576	—	C-F: .1μF, 50V
C16 – C19	4	0160-3694	4	C-F: 330pF, 100V
CR1 – CR4	1	1901-1098	4	Diode: Switching
MP1	9	0340-0883	4	Transistor Insulator
Q1	7	1854-0477	2	Transistor: NPN, 2N2222A
Q2 – Q3	9	1853-0281	2	Transistor: PNP, 2N2907A
Q4	7	1854-0477	—	Transistor: NPN, 2N2222A
R1	0	0698-0085	2	R-F: 2610Ω, 1%, .125W
R2	9	0757-0442	2	R-F: 10kΩ, 1%, .125W
R3	0	0757-0401	2	R-F: 100Ω, 1%, .125W
R4	0	0698-0085	—	R-F: 2610Ω, 1%, .125W
R5	9	0757-0442	—	R-F: 10kΩ, 1%, .125W
R6	0	0757-0401	—	R-F: 100Ω, 1%, .125W
R7	1	0683-1035	1	R-F: 10kΩ, 5%, .25W
R8	6	0683-2715	1	R-F: 270Ω, 5%, .25W
R9	9	0683-1025	1	R-F: 1kΩ, 5%, .25W
R10	3	0683-1045	1	R-F: 100kΩ, 5%, .25W
R11	8	0683-4705	1	R-F: 47Ω, 5%, .25W
R12	2	0683-1515	1	R-F: 150Ω, 5%, .25W
R13, R14	7	1810-0205	2	Resistor Network, 4.7kΩ
S1	8	3101-0489	1	Switch, 4 Segment SPST
S2	2	3101-0491	1	Switch, 10 Segment SPST
U1	3	1MB5-0101	1	IC: Translator
U2	3	1820-2438	1	IC: MCU, 11 MHz
U3	8	1820-1112	1	IC: SN74LS74N
U4	0	1820-2443	1	IC: 8250
U5	7	1820-1492	1	IC: SN74LS368AN
U6	8	1820-0990	1	IC: MC1489AL
U7	6	1990-0494	1	Opto-Isolator
U8	5	1820-0509	1	IC: MC1488L
U9	6	1990-0444	1	Opto-Isolator
U10	7	1820-1195	1	IC: SN74LS175N
Y1	0	0410-1221	1	XTAL: 5.5296 MHz
	9	0590-0199	2	Hex Nut with Lock Washer
	0	2200-0143	7	Screws: 4-40 Machine
	9	0363-0174	1	Contact, Ground
	7	1400-1062	1	Clamp: Cable
	8	1400-1063	1	Clamp: Cable

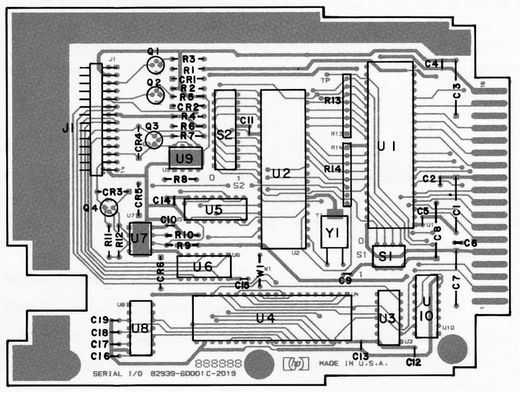
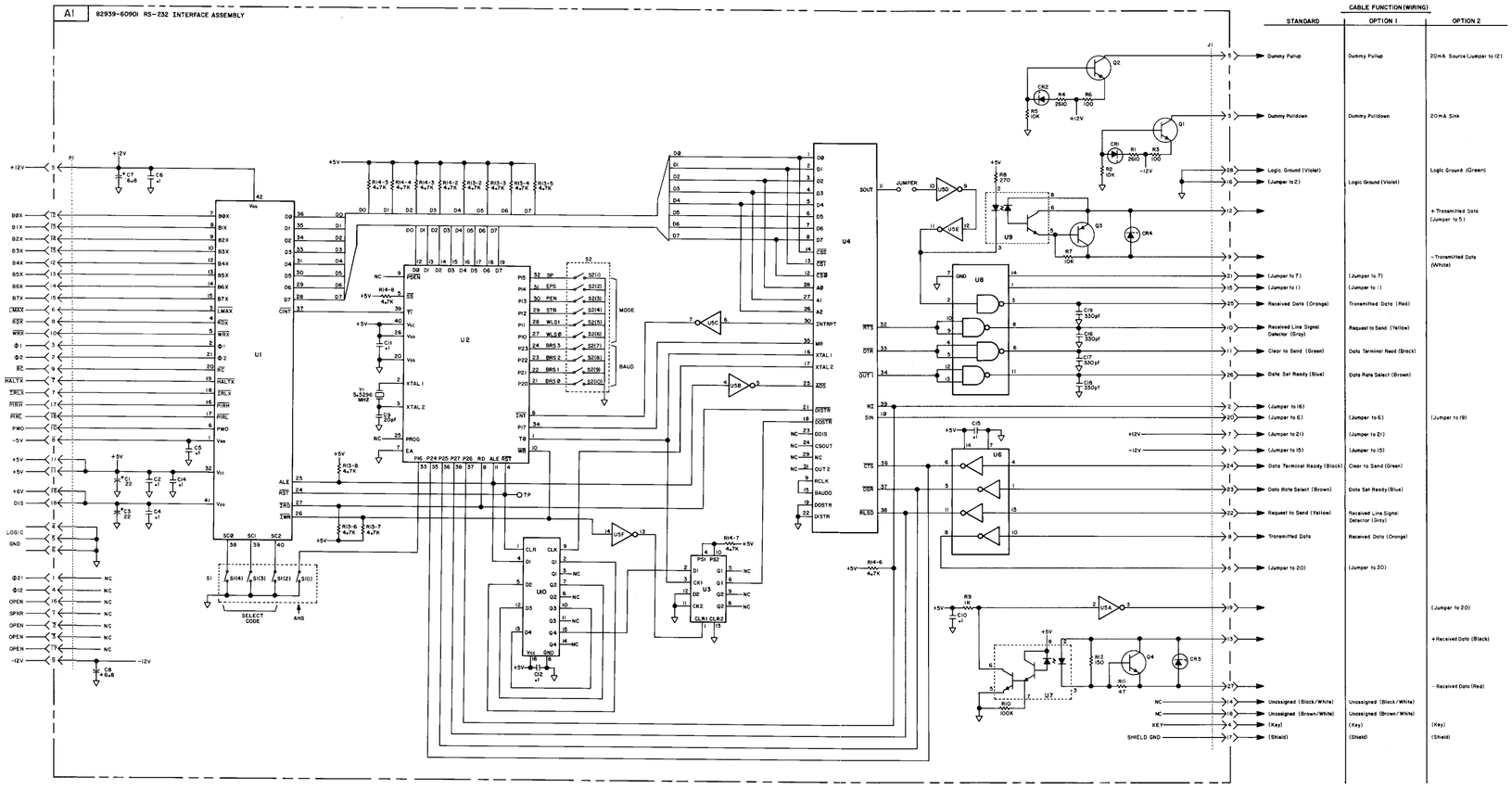


Figure 3-4. RS-232 Interface Schematic Diagram



Appendix A

RS-232C

RS-232C Compatible

What is the meaning of "RS-232C Compatible"? Or, of more importance, what doesn't it mean?

To answer the latter question first, it does not mean that every piece of equipment bearing that label will work perfectly with every other piece of equipment so labelled. What it does mean is that the equipment does not exceed any of the specifications or characteristics set down in the standard known as EIA RS-232C. But within the scope of RS-232C there is enough latitude to permit minor incompatibilities from one device to another, and these minor incompatibilities can cause unpleasant surprises for the unwary.

What is RS-232C?

In 1963, the Electronic Industry Association (EIA) established a standard to govern the Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Interchange. The latest revision of this standard has been in effect since 1969 and is known colloquially as RS-232C. It specifies:

- Mechanical characteristics of the interface,
- Electrical characteristics of the interface,
- A number of interchange circuits with descriptions of their functions,
- The relationship of interchange circuits to standard interface types.

The Comite Consultatif International Telephonique et Telegraphique (CCITT) has established standards that correspond to RS-232C. While these standards, CCITT V.24 and CCITT V.28, are very similar to RS-232C, they are not identical. Because it does not make use of all the circuits defined in both RS-232C and CCITT V.24, the 82939 Data Communications Interface conforms to both RS-232C and CCITT V.24 without any modification of the interface. The circuits which are utilized vary with different applications and with different modems. The drivers and receivers used in the 82939 conform to voltage and other electrical specifications of both CCITT V.28 and RS-232C.

Mechanical Characteristics

The standard gives definitions to 22 pins and designates three pins as unassigned, but does not specify a 25-pin connector. Although a particular 25-pin connector is not defined, the industry has accepted the connector shown in Figure A-1 as a de facto standard. The male connector is used with data terminal equipment (the desktop computer), and the female connector is used with data communications equipment (the modem).

The length of the cable used by data terminal equipment to connect to data communications equipment should not be longer than 15.24 metres (50 feet). This is assuming that the load capacitance at the interface point is the worst case value of 2,500 picofarads. Longer cables are often used, especially in point-to-point configurations when the user knows that the total load capacitance will not exceed the 2,500 pf maximum.

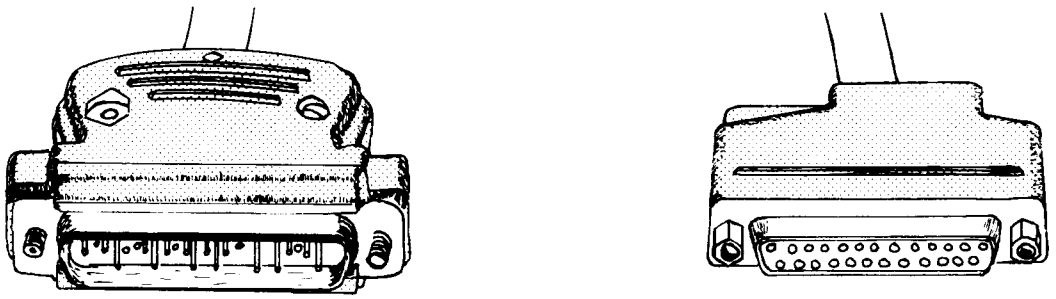


Figure A-1. 25-Pin Connector

Electrical Characteristics

A number of electrical parameters and limitations are defined by RS-232C for each interchange circuit. They refer to the equivalent interchange circuit shown in Figure A-2. All voltage measurements are made at the interface point and with reference to signal ground.

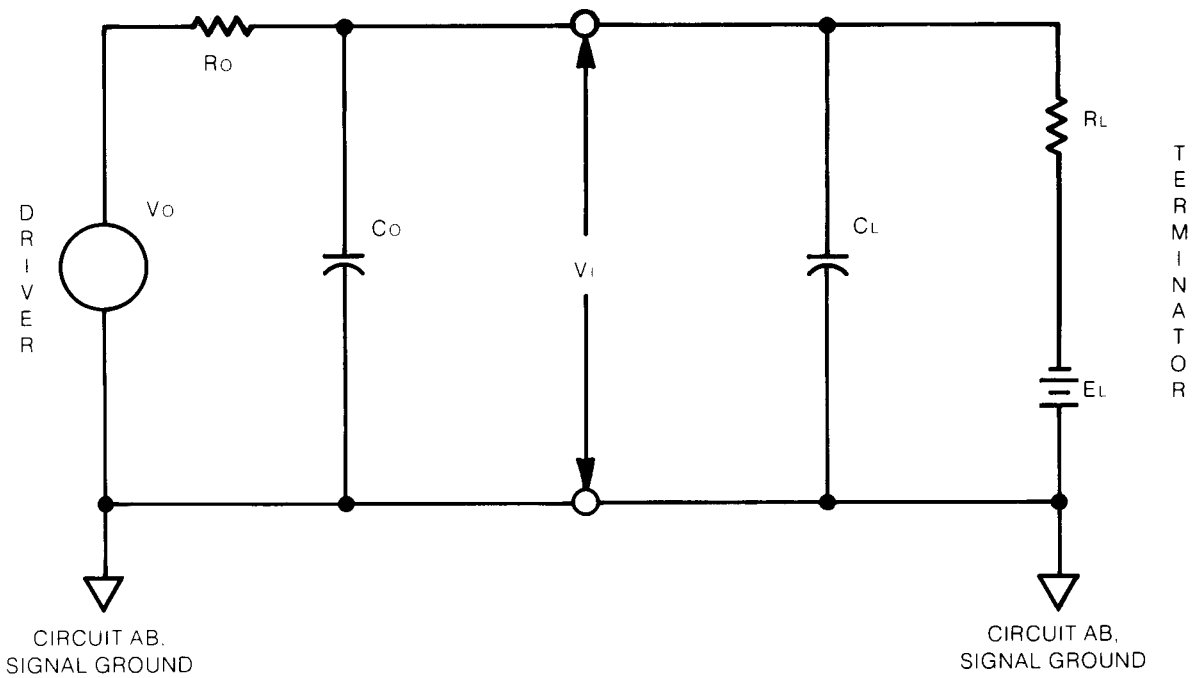


Figure A-2. Interchange Equivalent Circuit

- Open circuit voltage from the driver shall not be greater than ±25 volts.
- The open circuit voltage of the terminator shall not exceed ±2 volts.
- The total capacitance of the terminator shall not exceed 2,500 picofarads.
- The driver output voltage must be between 5 and 15 volts when the total terminator input resistance is between 3,000Ω and 7,000Ω.
- The output impedance of the driver circuit, when the driver power is off, shall not exceed 300Ω.
- The rate of change of the driver output voltage (slew rate) shall not exceed 30 volts per microsecond.

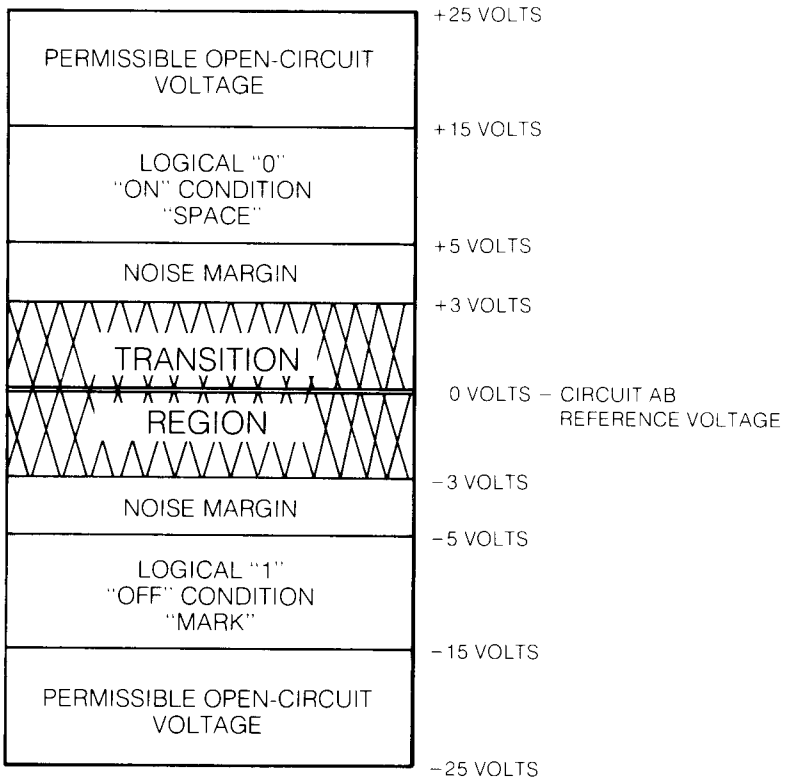


Figure A-3. Circuit Voltage Levels

In addition, several rules define the logic state indicated by voltage levels on the circuit.

- A logical "1" (MARK) is indicated when the voltage at the interface point is more negative than −3 volts.
- A logical "0" (SPACE) is indicated when the voltage at the interface point is more positive than +3 volts.
- To indicate a "1" signal condition (MARK), the driver shall assert a voltage between −5 volts and −15 volts.
- To indicate a "0" signal condition (SPACE), the driver shall assert a voltage between +5 volts and +15 volts.

Note that these standards allow for a 2-volt noise margin between the minimum driver voltage of 5 volts and the maximum undefined voltage of 3 volts. Other specifications that govern the transition region:

- All interchange signals entering the transition region shall proceed to the opposite valid signal state. It shall not re-enter the transition region until the next significant change in signal state.
- While in the transition region, the direction of the voltage change must not reverse.
- The time required for a control signal to cross the transition region shall not exceed one millisecond.
- The time required for a data or timing signal to cross the transition region shall not exceed one millisecond or four percent of the nominal signal period, whichever is the lesser.

Appendix B

RS-232C Function Table

This table contains the RS-232C functions, listed by pin number in the connector. Those functions marked with an asterisk are implemented in the 82939 Interface.

Pin 1	***Protective Ground.** Electrical equipment frame and ac power ground.
Pin 2	***Transmitted Data.** Data originated by the terminal to be transmitted via the sending modem.
Pin 3	***Received Data.** Data from the receiving modem in response to analog signals transmitted from the sending modem.
Pin 4	***Request to Send.** Indicates to the sending modem that the terminal is ready to transmit data.
Pin 5	***Clear to Send.** Indicates to the terminal that its modem is ready to transmit data.
Pin 6	***Data Set Ready.** Indicates to the terminal that its modem is not in a test mode and that modem power is ON.
Pin 7	***Signal Ground.** Establishes common reference between the modem and the terminal.
Pin 8	***Received Line Signal Detector.** Indicates to the terminal that its modem is receiving carrier signals from the sending modem.
Pin 9	Reserved for test.
Pin 10	Reserved for test.
Pin 11	Unassigned.
Pin 12	**Secondary Received Line Signal Detector.** Indicates to the terminal that its modem is receiving secondary carrier signals from the sending modem.
Pin 13	**Secondary Clear to Send.** Indicates to the terminal that its modem is ready to transmit signals via the secondary channel.
Pin 14	**Secondary Transmitted Data.** Data from the terminal to be transmitted by the sending modem's channel.
Pin 15	**Transmitter Signal Element Timing.** Signal from the modem to the transmitting terminal to provide signal element timing information.

* Implemented in the 82939 Interface Card.

Pin 16 **Secondary Received Data.** Data from the modem's secondary channel in response to analog signals transmitted from the sending modem.

Pin 17 **Receiver Signal Element Timing.** Signal to the receiving terminal to provide signal element timing information.

Pin 18 Unassigned.

Pin 19 **Secondary Request to Send.** Indicates to the modem that the sending terminal is ready to transmit data via the secondary channel.

Pin 20 ***Data Terminal Ready.** Indicates to the modem that the associated terminal is ready to receive and transmit data.

Pin 21 **Signal Quality Detector.** Signal from the modem telling whether a defined error rate in the received data has been exceeded.

Pin 22 **Ring Indicator.** Signal from the modem indicating that a ringing signal is being received over the line.

Pin 23 ***Data Signal Rate Selector.** Selects one of two signaling rates in modems having two rates.

Pin 24 **Transmit Signal Element Timing.** Transmit clock provided by the terminal.

Pin 25 Unassigned.

* Implemented in the 82939 Interface Card.

Appendix C

ASCII Character Set

ASCII Char.	EQUIVALENT FORMS			
	Binary	Oct	Hex	Dec
NULL	00000000	000	00	0
SOH	00000001	001	01	1
STX	00000010	002	02	2
ETX	00000011	003	03	3
EOT	00000100	004	04	4
ENQ	00000101	005	05	5
ACK	00000110	006	06	6
BELL	00000111	007	07	7
BS	00001000	010	08	8
HT	00001001	011	09	9
LF	00001010	012	0A	10
VT	00001011	013	0B	11
FF	00001100	014	0C	12
CR	00001101	015	0D	13
SO	00001110	016	0E	14
SI	00001111	017	0F	15
DLE	00010000	020	10	16
DC1	00010001	021	11	17
DC2	00010010	022	12	18
DC3	00010011	023	13	19
DC4	00010100	024	14	20
NAK	00010101	025	15	21
SYNC	00010110	026	16	22
ETB	00010111	027	17	23
CAN	00011000	030	18	24
EM	00011001	031	19	25
SUB	00011010	032	1A	26
ESC	00011011	033	1B	27
FS	00011100	034	1C	28
GS	00011101	035	1D	29
RS	00011110	036	1E	30
US	00011111	037	1F	31

ASCII Char.	EQUIVALENT FORMS			
	Binary	Oct	Hex	Dec
space	00100000	040	20	32
!	00100001	041	21	33
"	00100010	042	22	34
#	00100011	043	23	35
$	00100100	044	24	36
%	00100101	045	25	37
&	00100110	046	26	38
'	00100111	047	27	39
(	00101000	050	28	40
)	00101001	051	29	41
*	00101010	052	2A	42
+	00101011	053	2B	43
,	00101100	054	2C	44
-	00101101	055	2D	45
.	00101110	056	2E	46
/	00101111	057	2F	47
0	00110000	060	30	48
1	00110001	061	31	49
2	00110010	062	32	50
3	00110011	063	33	51
4	00110100	064	34	52
5	00110101	065	35	53
6	00110110	066	36	54
7	00110111	067	37	55
8	00111000	070	38	56
9	00111001	071	39	57
:	00111010	072	3A	58
;	00111011	073	3B	59
<	00111100	074	3C	60
=	00111101	075	3D	61
>	00111110	076	3E	62
?	00111111	077	3F	63

ASCII Char.	EQUIVALENT FORMS			
	Binary	Oct	Hex	Dec
@	01000000	100	40	64
A	01000001	101	41	65
B	01000010	102	42	66
C	01000011	103	43	67
D	01000100	104	44	68
E	01000101	105	45	69
F	01000110	106	46	70
G	01000111	107	47	71
H	01001000	110	48	72
I	01001001	111	49	73
J	01001010	112	4A	74
K	01001011	113	4B	75
L	01001100	114	4C	76
M	01001101	115	4D	77
N	01001110	116	4E	78
O	01001111	117	4F	79
P	01010000	120	50	80
Q	01010001	121	51	81
R	01010010	122	52	82
S	01010011	123	53	83
T	01010100	124	54	84
U	01010101	125	55	85
V	01010110	126	56	86
W	01010111	127	57	87
X	01011000	130	58	88
Y	01011001	131	59	89
Z	01011010	132	5A	90
[	01011011	133	5B	91
\	01011100	134	5C	92
]	01011101	135	5D	93
^	01011110	136	5E	94
_	01011111	137	5F	95

ASCII Char.	EQUIVALENT FORMS			
	Binary	Oct	Hex	Dec
`	01100000	140	60	96
a	01100001	141	61	97
b	01100010	142	62	98
c	01100011	143	63	99
d	01100100	144	64	100
e	01100101	145	65	101
f	01100110	146	66	102
g	01100111	147	67	103
h	01101000	150	68	104
i	01101001	151	69	105
j	01101010	152	6A	106
k	01101011	153	6B	107
l	01101100	154	6C	108
m	01101101	155	6D	109
n	01101110	156	6E	110
o	01101111	157	6F	111
p	01110000	160	70	112
q	01110001	161	71	113
r	01110010	162	72	114
s	01110011	163	73	115
t	01110100	164	74	116
u	01110101	165	75	117
v	01110110	166	76	118
w	01110111	167	77	119
x	01111000	170	78	120
y	01111001	171	79	121
z	01111010	172	7A	122
{	01111011	173	7B	123
|	01111100	174	7C	124
}	01111101	175	7D	125
~	01111110	176	7E	126
DEL	01111111	177	7F	127

1000 N.E. Circle Blvd., Corvallis, OR 97330

82939-90001 Rev. B

Printed in U.S.A.